Analysis of Active Pixel Sensor Readout Circuit

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***Abstract*—This brief provides a detailed analysis of active pixel sensor, pixel and column circuit. Surprisingly, we find that shorter readout times can be achieved by reducing the bias current and hence reducing energy consumption. We investigate the effect of nonidealities on the readout operation. We find that when the follower transistor channel-length modulation is taken into consideration, delay is reduced, which implies that shorter length transistors can be used in the pixel. We show that readout time decreases linearly with technology scaling.**

***Index Terms*—Active pixel sensor (APS), CMOS image sensor, high-speed imaging, readout electronics.**

I. Introduction

An important advantage of CMOS active pixel sensor (APS) architecture [1] is its high frame-rate capability. Several high-speed APS implementations have been reported. For example, in [2], Krymski *et al.* describe a 1024 × 1024 APS with column level analog-to-digital converter (ADC) achieving frame rate of 500 frames/s. In [3], Stevanovic *et al.* describe a 256 × 256 APS with 64 analog outputs achieving frame rate of 1000 frames/s. Recently, high-speed CMOS APS based digital cameras have become commercially available [4]. The high frame-rate capability of CMOS APS combined with the ability to integrate processing with the sensor on the same chip also enables the implementation of several still and video imaging applications, such as dynamic range extension, motion-blur prevention, and high accuracy optical flow estimation [5], [6].

Although APS is currently the most popular CMOS image-sensor architecture and has been extensively reported on, to the best of our knowledge, no detailed analysis of its readout circuit has been published, especially when implemented in deep submicron technologies. A better understanding of the APS readout circuit operation can help further increase its frame rate and reduce its power consumption.

In this brief, we provide a detailed analysis of the standard APS pixel and column readout circuit. Our analysis considers such nonidealities as the access transistor resistance, channel-length modulation, and nonsquare-law saturation current. The analysis is first performed assuming a standard 0.35-μm CMOS technology. Contrary to conventional wisdom, we find that shorter readout times can be achieved by reducing the bias current and hence reducing energy consumption. We find that when the follower transistor channel-length modulation is taken into consideration, delay is reduced, which implies that shorter length transistors can be used allowing for a smaller pixel size or a higher fill factor. The analysis is then extended down to 0.1 μm. We find that delay improves linearly with technology scaling.

The rest of the brief is organized as follows. In Section II, we briefly describe the APS circuit operation. In Section III, we analyze the APS circuit assuming a 0.35-μm CMOS technology. In Section IV, we analyze the effect of the nonidealities on circuit delay. In the last section, we discuss the effect of technology scaling down to 0.1 μm on readout time.

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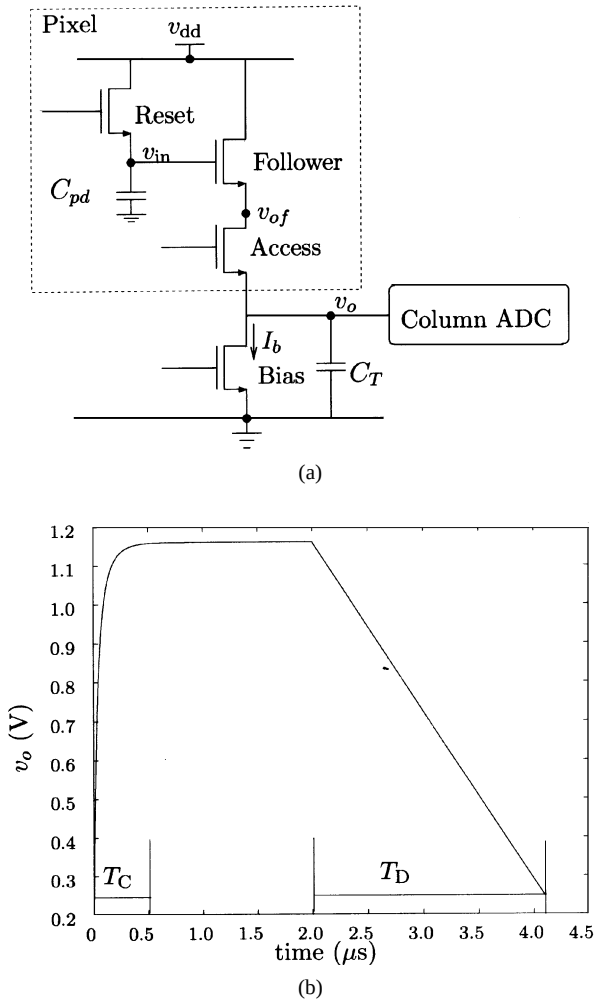


Fig. 1. (a) APS circuit schematic. (b) HSPICE output waveform showing charging and discharging operations for a typical 0.35-μm CMOS technology (t_C is charging time, while t_D is discharging time).

II. APS Circuit Operation

We consider the basic three-transistor APS pixel and column APS circuit depicted in Fig. 1(a). The capacitor C_{pd} shown in the figure represents the equivalent photodiode capacitance. The bias transistor and capacitor C_T are shared among pixels in the same column. In standard APS operation, e.g., [1], the bit line is not reset after reading each row. Instead, it is charged through the follower transistor or discharged through the column bias transistor depending on the bit-line voltage at the end of the previous row readout [see Fig. 1(b)]. Since bit-line voltage changes linearly with time during discharging compared to exponentially during charging, discharging time limits row readout time and can be very slow. One can speed up the discharging operation by using a higher bias current, but this leads to higher power consumption. To reduce the readout time to the charging time, the bit line may be reset to a low-voltage value after each row readout by pulsing the gate of the current source. For a given readout time requirement, this method achieves lower power consumption than using the standard operation.

For the rest of the brief, we focus on analyzing the APS readout circuit during charging. For completeness, we include a brief analysis of the the circuit during discharging in the Appendix.

III. Analysis of Readout Time

After photocurrent integration, readout is performed by turning on the access transistor. Ideally, the access transistor resistance would be zero, leading to $v_o = v_{of}$. Assuming a level-1 MOS transistor model for both the bias and follower transistors, (i.e., no channel-length modulation), Kirchhoff's current law at the output node gives

$$I_b + C_T \frac{dv_0}{dt} = K_n (v_{in} - v_{TF} - v_0)^2.$$

This differential equation can be readily solved analytically by separation of variables and the output voltage $v_o(t)$ is given by

$$v_o(t) = v_{in} - v_{TF} - \rho \left(\frac{1 + \frac{\alpha-\rho}{\alpha+\rho} e^{\frac{-2\rho K_n}{C_T} t}}{1 - \frac{\alpha-\rho}{\alpha+\rho} e^{\frac{-2\rho K_n}{C_T} t}} \right)$$

where $K_n = (1/2)\mu_n C_{ox}(W/L)$ is the follower transistor transconductance, v_{TF} is its threshold voltage, and $\rho = \sqrt{(I_b/K_n)}$, and $\alpha = v_{in} - v_{TF} - v_o(0)$.

In most APS implementations aimed at high frame-rate operation, each column, or group of columns, share an ADC (e.g., [2]). The *readout time* T_R is defined as the time from the access transistor turning on to the output voltage v_o reaching to within half a bit of its steady state value. For worst case delay, we set the input voltage v_{in} to its maximum possible value and assume that the output voltage before switching is at its lowest possible value, $v_o(0)$. Under these conditions, the readout time is given by

$$T_R = \frac{C_T}{2\sqrt{K_n I_b}} \ln \frac{(\beta+\rho)(\alpha-\rho)}{(\beta-\rho)(\alpha+\rho)}$$

where

$$\beta = v_{in} - v_{TF} - v_o(T_s)$$
$$v_o(T_s) = \left(1 - \frac{1}{2^{n+1}}\right)(v_o(\infty) - v_o(0)) + v_o(0)$$
$$v_o(\infty) = v_{in} - v_{TF} - \sqrt{\frac{I_b}{K_n}}.$$

Fig. 2(a) plots T_R versus bias current I_b assuming typical 0.35-μm CMOS technology parameters and $C_T = 3.7$ pf, $k_n = 1.88$ μA/V^2, follower and bias transistor ratios $(W/L) = (4/2)$, and $(W/L) = (16/32)$, respectively, $v_o(0) = 0.2$ V, $v_{in} = 2.2$ V, and ADC resolution of 8 bits. Note that decreasing bias current leads to shorter readout time, since more current is available to charge the output node.

Reducing bias current also leads to an increase in output voltage swing, S, which is given by

$$S = v_o(\infty) - v_o(0) = v_{in} - v_{TF} - \sqrt{\frac{I_b}{K_n}} - v_o(0).$$

As bias current is reduced from 1.9 to 0.1 μA, voltage swing increases from 1 to 1.08 V.

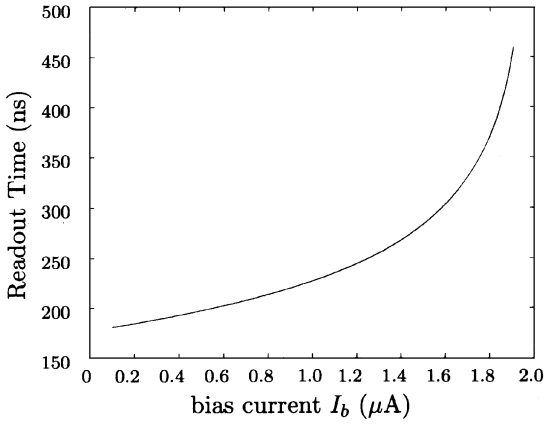
The energy consumed by the APS circuit during readout can be calculated by integrating the power consumed during readout, which gives

$$E = C_T v_{\rm dd} \left(\frac{\rho}{2} \ln \left(\frac{(\beta+\rho)(\alpha-\rho)}{(\beta-\rho)(\alpha+\rho)} \right) + v_o(0) - v_o(T_R) \right).$$

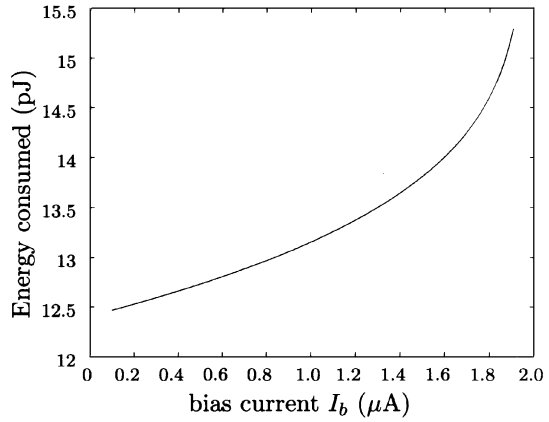
As bias current is reduced from 1.9 to 0.1 μA, the energy consumed drops by 20% as shown in Fig. 2(b), while readout time is reduced by as much as 50% as shown in Fig. 2(a). Thus, contrary to coventional wisdom, delay can be reduced while consuming less energy.

IV. Effect of Transistor Nonidealities

In this section, we investigate the effect of circuit nonidealities, namely, nonzero access transistor resistance R_a, current source



(a)



(b)

Fig. 2. (a) APS readout time versus bias current. (b) Energy consumed during readout versus bias current.

channel-length modulation λ_i, follower transistor channel-length modulation λ_f, and the nonsquare drain to source saturation current exponent γ. With these nonidealities included, the circuit equations become

$$I_f = \frac{v_{of} - v_o}{R_a}$$
$$I_f = I_b(1 + \lambda_i v_o) + C_T \frac{dv_o}{dt}, \text{ and}$$
$$I_f = K_n (v_{in} - v_{TF} - v_{of})^{\gamma} (1 + \lambda_f (v_{dd} - v_o)).$$

To better understand the effect of each nonideality on readout time, we vary one parameter at a time while setting the other parameters to their ideal values. First we set $\gamma = 2$. In this case, the above equations can be numerically solved by evaluating the integral

$$T_R = \int_{\alpha}^{\beta} -C_T \frac{1 + 2RK_n x}{D(x)} dx \tag{1}$$

where

$$D(x) = K_n \lambda_f x^3 + K_n (1 + \lambda_f (v_{\rm dd} - v_{\rm in} + v_{\rm TF}) + I_b \lambda_i R) x^2 + I_b \lambda_i x - I_b (1 + \lambda_i (v_{in} - V_{TF})).$$

First we consider the effect of the nonzero access transistor resistance R_a on readout time. In this case, the integral (1) has a closed-form solution, given by

$$T_R = \frac{C_T}{2\sqrt{K_n * I_b}} \ln \left(\frac{(\beta+\rho)(\alpha-\rho)}{(\beta-\rho)(\alpha+\rho)} \right) + R_a C_T \ln \left(\frac{\alpha^2 - \rho^2}{\beta^2 - \rho^2} \right).$$

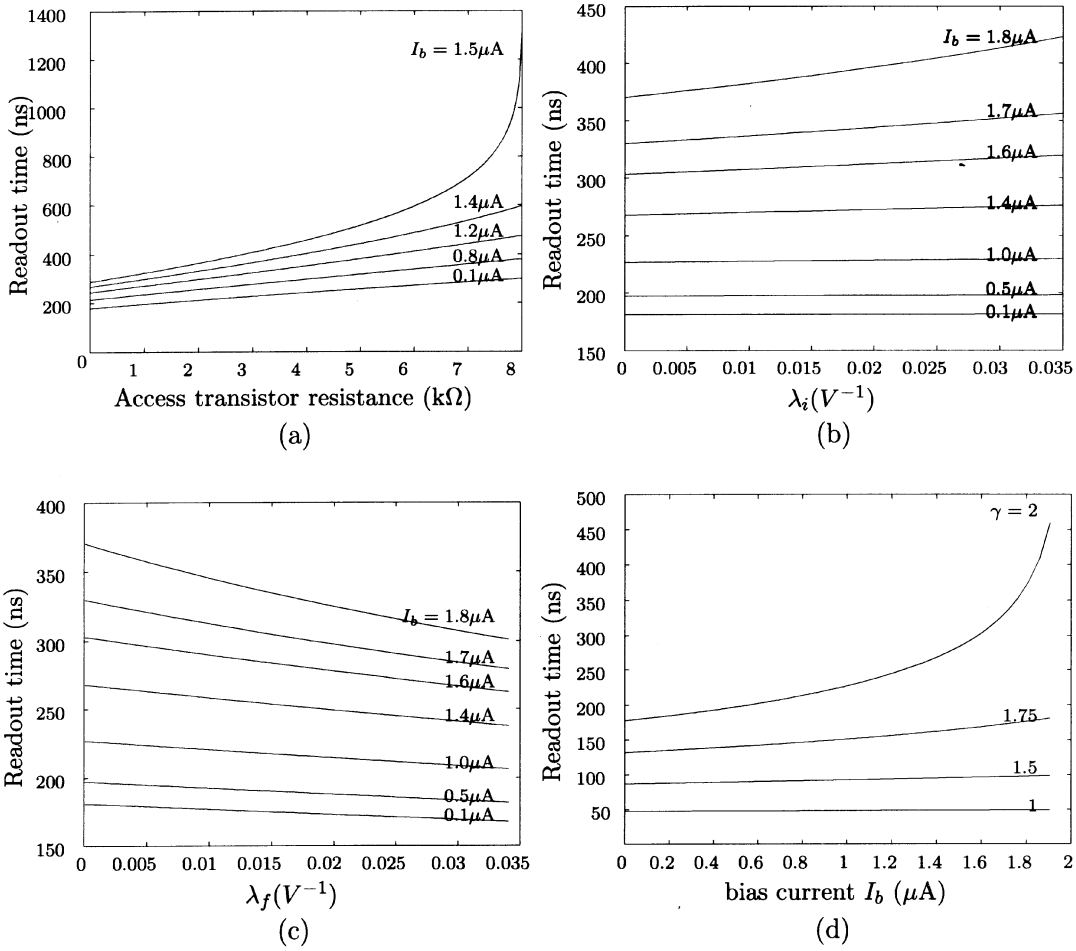


Fig. 3. (a) Readout time versus access transistor resistance. (b) Readout time versus current source lambda. (c) Readout time versus follower transistor lambda. (d) Readout time versus bias current for different γ.

Note that decreasing the access-transistor resistance, which can be done by increasing its width, reduces readout time. This, however, is not desirable, since it leads to larger pixel size or a smaller fill factor. Fortunately, this effect can be mitigated using lower bias current as described in Section III.

Now, we consider the current-source-transistor-channel-length modulation. We set R_a and λ_f to zero in the Intergral l, and we obtain the analytical solution

$$T_R = \frac{C_T}{2K_n\rho}\ln\left(\frac{(\beta+\rho)(\alpha-\rho)}{(\beta-\rho)(\alpha+\rho)}\right)$$

where

$$\beta = \frac{\lambda_i I_b}{2K_n} + v_{in} - v_{TF} - v_{o\max}$$

$$\alpha = \frac{\lambda_i I_b}{2K_n} + v_{in} - v_{TF} - v_{o\min} \quad \text{and}$$

$$\rho = \sqrt{\frac{I_b\left(1+\lambda_i(v_{in}-v_{TF})\right)}{K_n} - \left(\frac{\lambda_i I_b}{2K_n}\right)^2}.$$

Readout time is plotted in Fig. 3(b). Note that it increases when the effect of the channel length is taken into consideration, due to the reduction in the current available to charge the output node. Since channel-length modulation is inversely proportional to the the transistor-gate length, λ can be decreased by increasing the transistor-channel length. Therefore, increasing the current source transistor gate length reduces readout time. This can be done with no effect on pixel size or fill factor, since the current source is part of the column level circuits.

Next, we consider the effect of the follower transistor channel-length modulation. The result is plotted in Fig. 3(c). As shown in the figure, readout time decreases as λ_f increases, due to the increase in the current available to charge the output node (for a given bias current). Therefore, readout time can be decreased by making the follower transistor channel length as small as possible.

Fig. 3(b) and (c) also shows that reducing bias current not only reduces readout time but also diminishes the effect of channel-length modulation.

As technology scales, the square-law-drain-saturation-current relation becomes less accurate. A more accurate model for the follower current is given by

$$I_f = K_n(v_{in} - v_{TF} - v_0)^\gamma, \qquad \text{for } 1 < \gamma < 2.$$

In this case, neglecting other nonidealities, the readout time can be readily calculated to be

$$T_R = \frac{C_T}{K_n}\sum_{j=1}^{\infty}\left(\frac{I_b}{K_n}\right)^{j-1}\frac{1}{(j\gamma+1)}\left(\frac{1}{\beta^{(j\gamma+1)}} - \frac{1}{\alpha^{(j\gamma+1)}}\right).$$

This is plotted in Fig. 3(d). As technology scales, readout time decreases and the effect of the bias current becomes less pronounced.

Fig. 4 plots readout time versus bias current using results of the integral (1) and HSPICE simulations, assuming the same parameters and conditions as in Section III, $\lambda_i = \lambda_f = 0.01\ \mathrm{V}^{-1}$, and $R_a = 2\ k\Omega$. Note that the HSPICE simulations results are in good agreement with the analytical results.

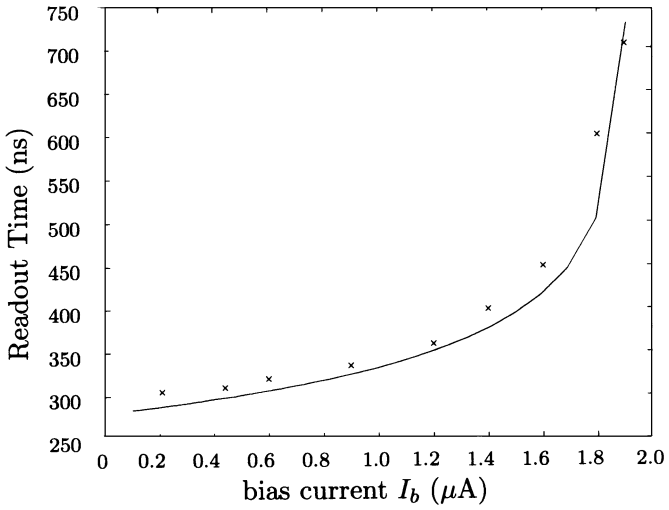


Fig. 4. Readout time versus bias current ($\times$ HSPICE simulation,-analytical).

TABLE I
SCALED TECHNOLOGY PARAMETER VALUES

Technology (μm)	0.35	0.25	0.18	0.13	0.1
Threshold Voltage (V)	0.6	0.5	0.4	0.3	0.25
Supply Voltage (V)	3.3	2.5	1.8	1.5	1.2
Oxide Thickness ($A°$)	12	6	5	2.7	1.9

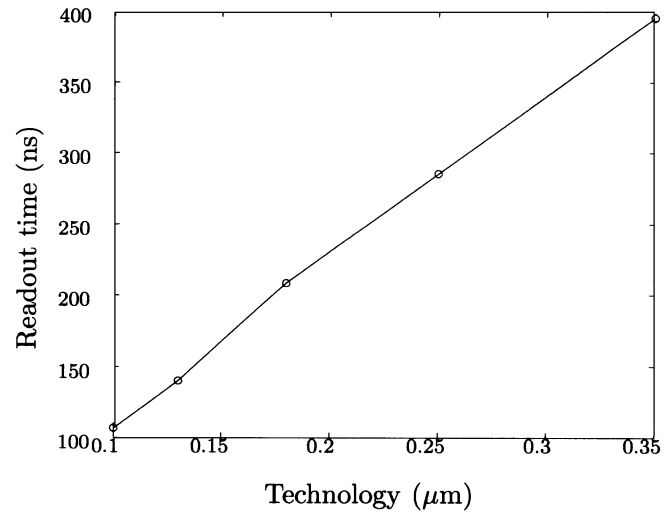


Fig. 5. Readout time versus minimum feature size.

V. TECHNOLOGY SCALING

To investigate the effect of technology scaling on readout time, we assume the device and circuit parameters in Table I, which are derived from the 1999 edition of the ITRS projections. Fig. 5 plots the readout time for technologies down to 0.1 μm. Note that readout time decreases almost linearly with minimum feature size.

VI. CONCLUSION

We presented a detailed analysis of the APS pixel and column circuit. We showed that shorter readout times can be achieved by reducing the bias current and hence reducing energy consumption. We then investigated the effect of nonidealities on the readout operation and found that when the follower transistor channel-length modulation is taken into consideration, delay is reduced. As expected, we found that delay improves linearly with technology scaling.

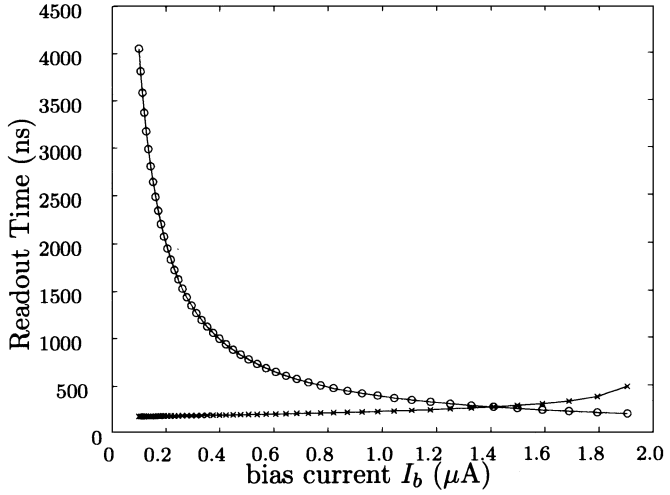


Fig. 6. APS readout time ($\times$ charging, o discharging).

APPENDIX

In the brief, we focused on the analysis of the APS readout circuit during charging. In this Appendix, we briefly analyze the circuit during discharging, which is determines the readout time in standard APS operation. For ideal operation and worst case analysis, the discharge time is given by 2

$$T_R = \frac{C_T}{I_b}\left(v_o(T_R) - v_o(0)\right). \tag{2}$$

Assuming a typical 0.35-μm CMOS technology, and the same circuit parameters as in Sections III and IV, the readout time through the discharge operation can be up to 30 times longer than the charging time for smaller bias current. To speed up the discharging time, higher bias currents can used but at the expense of higher power consumption as illustrated in Fig. 6.

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