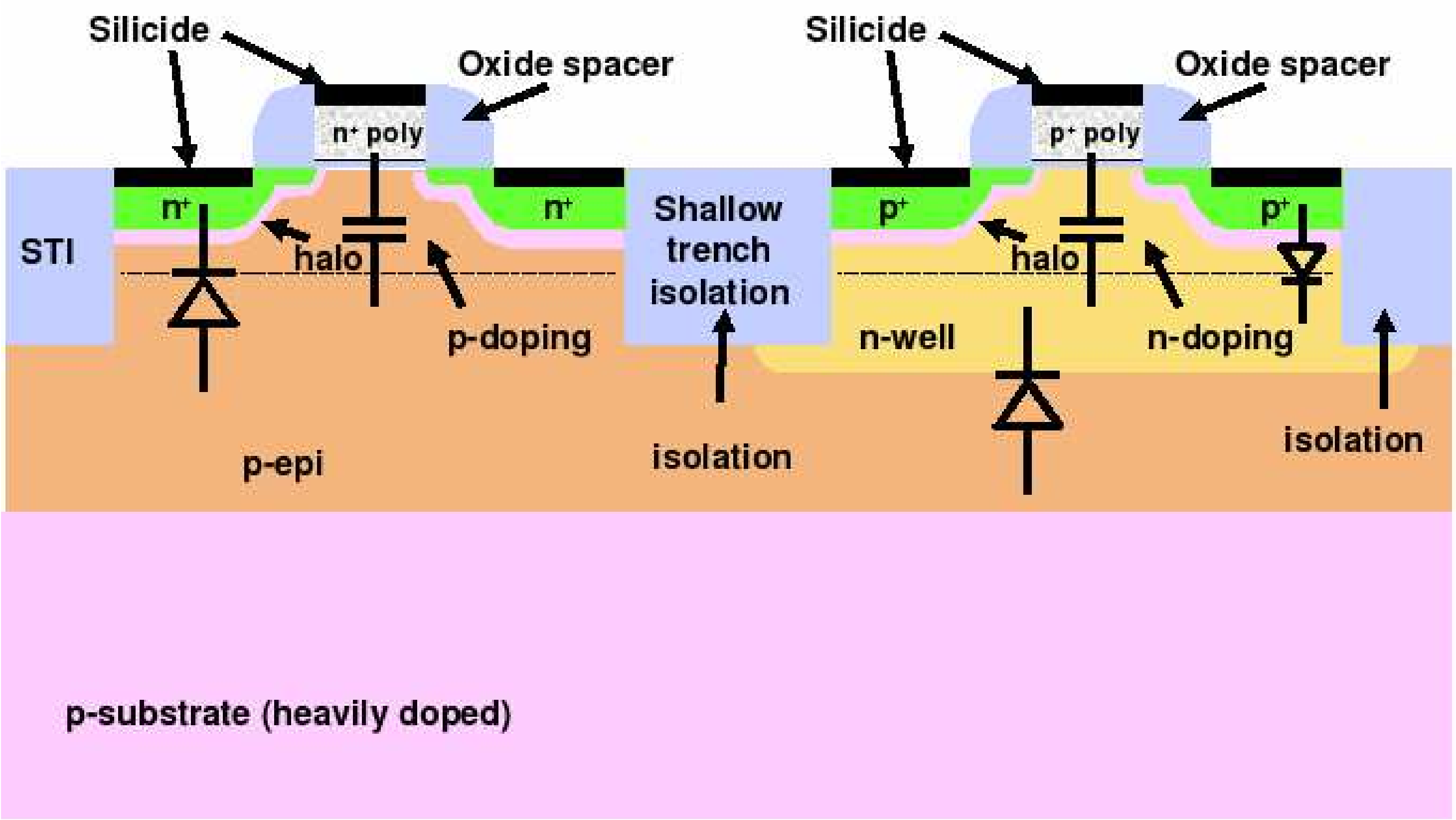
Lecture Notes 5

CMOS Image Sensor Device and Fabrication

- CMOS image sensor fabrication technologies
- Pixel design and layout
- Imaging performance enhancement techniques
- Technology scaling, industry trends
- Microlens
- Color filter array

Modern CMOS Device Structure



Imaging Is Different from Digital Logic

Features	**Digital Logic**	**Imaging**
Silicide	Improves contact resistance	Absorbs light – low photosensitivity Increased junction leakage
STI	Enables tighter design rules	Leads to larger dark current due to defects from stress
Shallow junction	Reduces short-channel effect	Reduces quantum efficiency for medium to long wavelength light
Lower power supply voltage	Reduces power consumption, enables device scaling	Reduces headroom for signal swing
Lower threshold voltage	Improves drive current	Increases subthreshold leakage
Thin gate oxide	Enables device scaling to shorter channel length	Increases gate leakage
Multiple levels of interconnect	Improves wire-ability	Increases distance from microlens or color filter to photodetector

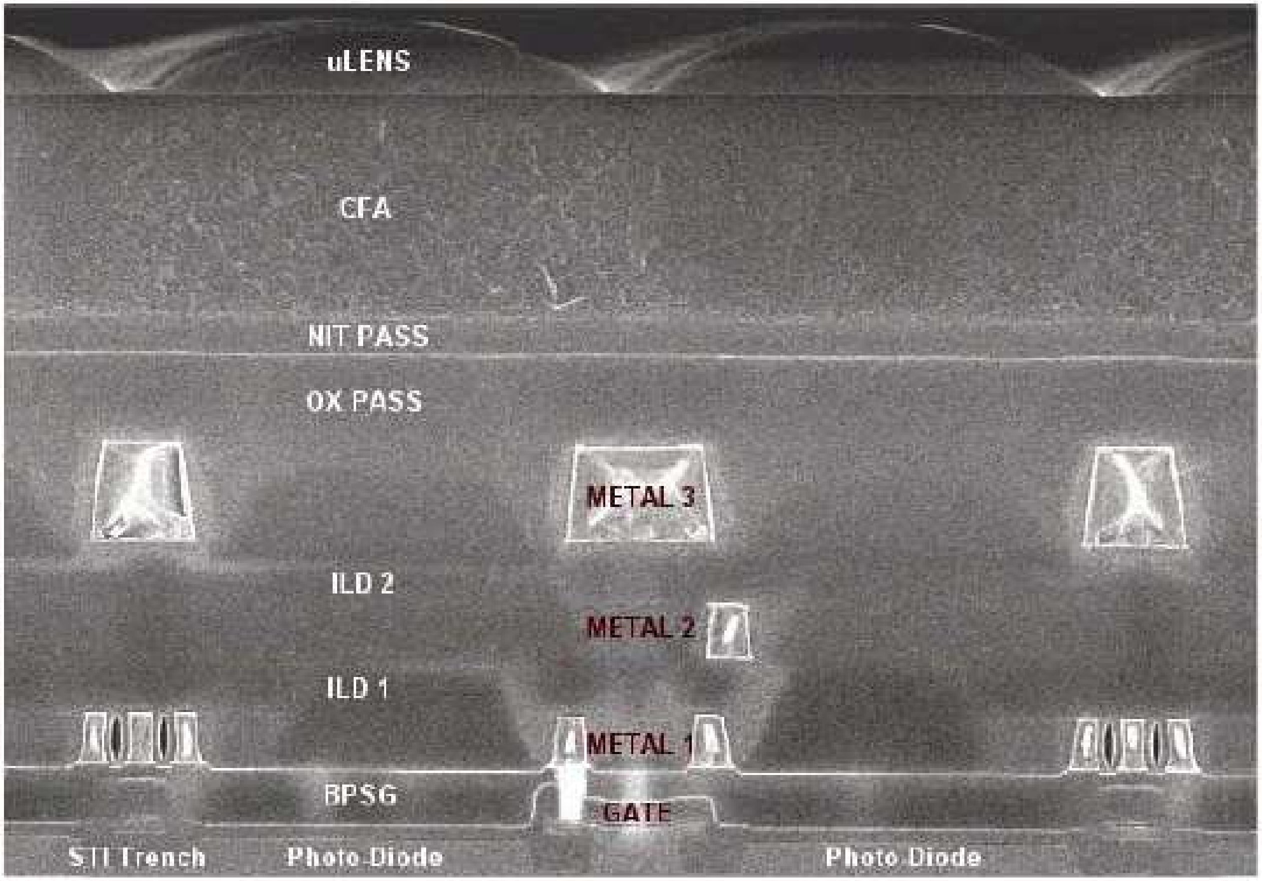
Baseline Modifications of CMOS for Imaging

Modifications are generally needed only in the pixel area

- Modifications to improve optical performance:
  - Non-silicided source/drain for photodiode and PolySi gate for photogate
  - Deeper n-well to p-substrate diode for improved quantum efficiency
  - Epi substrate thickness optimization for quantum efficiency, spectral tailoring and crosstalk optimization
  - Customized dielectric layers to reduce reflection from material with mis-matched refractive index
  - Reduced metal light shield height, tight (vertical and horizontal) light shield

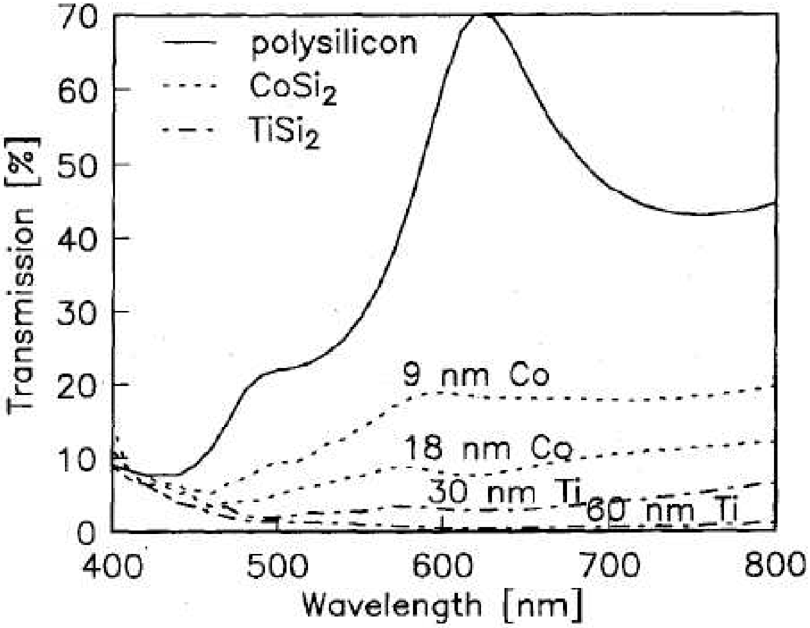
- Modifications to reduce dark current:
  - Avoid landed contacts, minimize gate edge, isolation edge
  - Gentle STI process and defect repair/avoidance around STI
- Modifications to in-pixel transistors:
  - Thicker gate oxide to handle higher pixel (analog) power supply
  - Adjust v_T to maximize signal swing and minimize leakage
  - Longer than minimum gate length to reduce hot-carrier induced photon emission and impact ionization

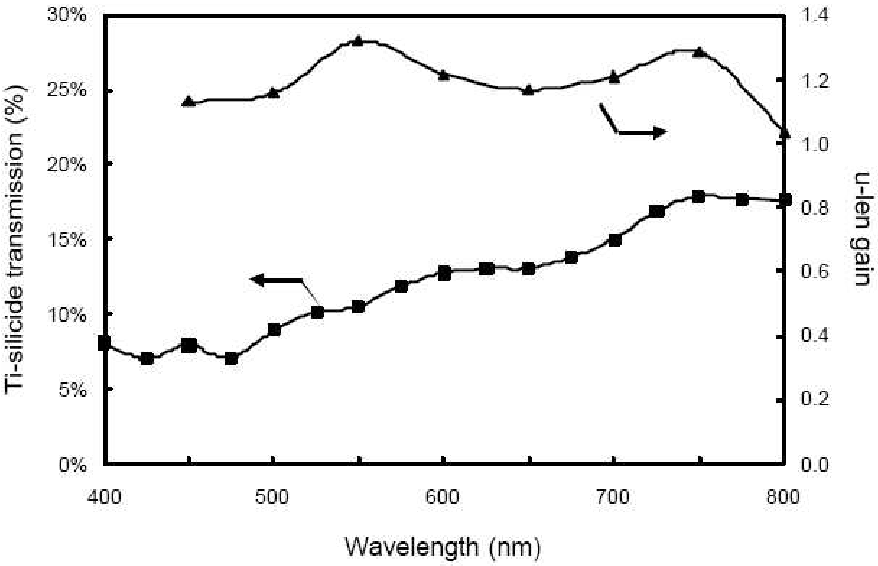
Example CMOS Image Sensor Cross-Section



H. Rhodes et al., "CMOS imager technology shrinks and image performance," IEEE Workshop on Microelectronics and Electron Devices, pp.7-18 (2004)

Silicide Transmittance



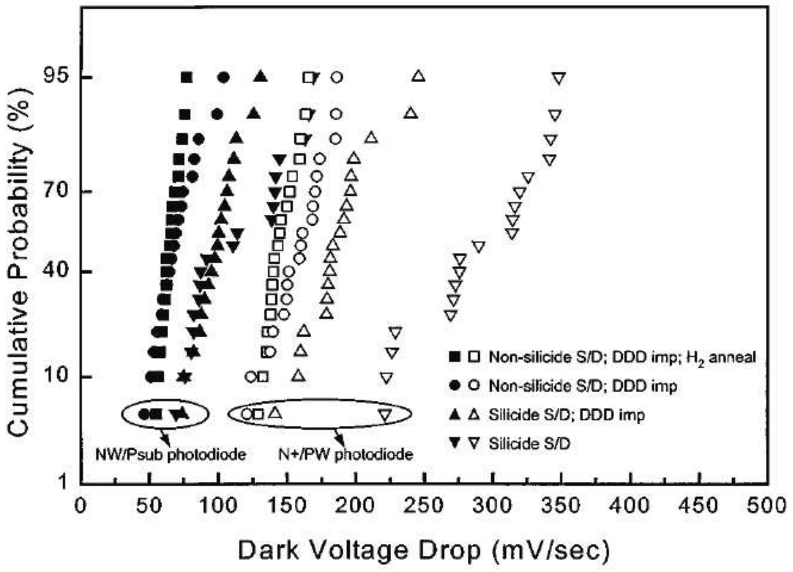


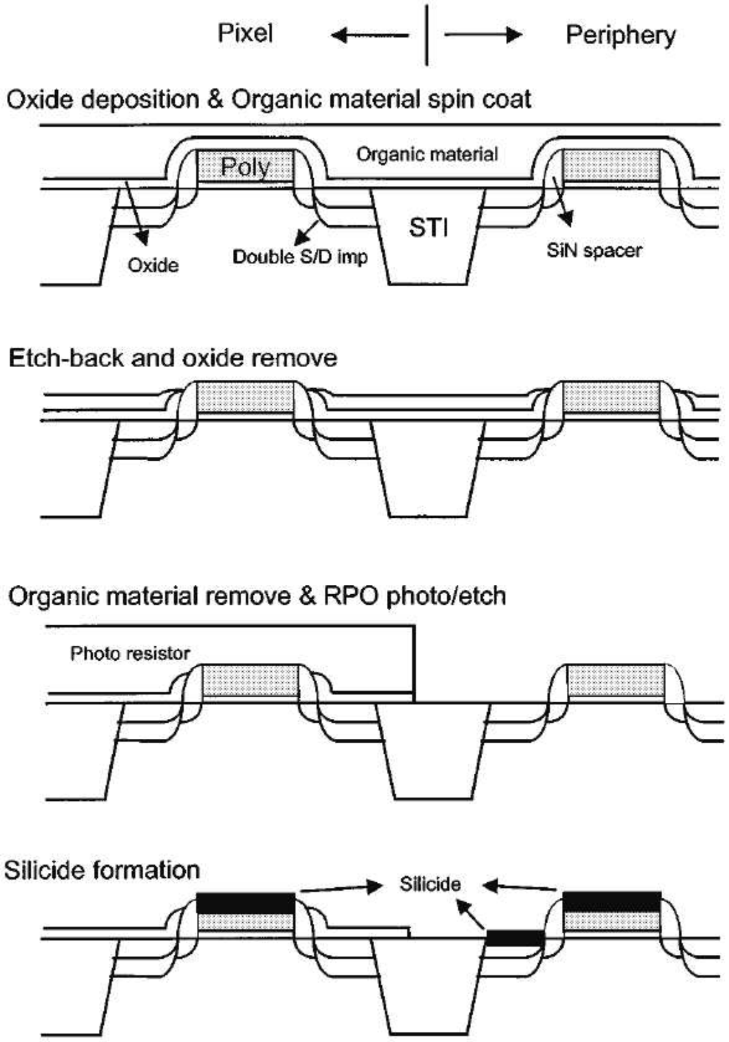
S.G. Wuu et al., “High performance 0.25 μm CMOS color imager technology with non-silicide source/drain pixel,” IEDM Tech. Dig., pp. 705-708 (2000)

H.-S. P. Wong, “Technology and Device Scaling Considerations for CMOS Imagers,” pp. 2131-2146 (1996)

Non-Silicided Source/Drain

- Silicide consumes silicon, causes stress and larger leakage (corner leakage)
- N-well to p-substrate diode has less leakage

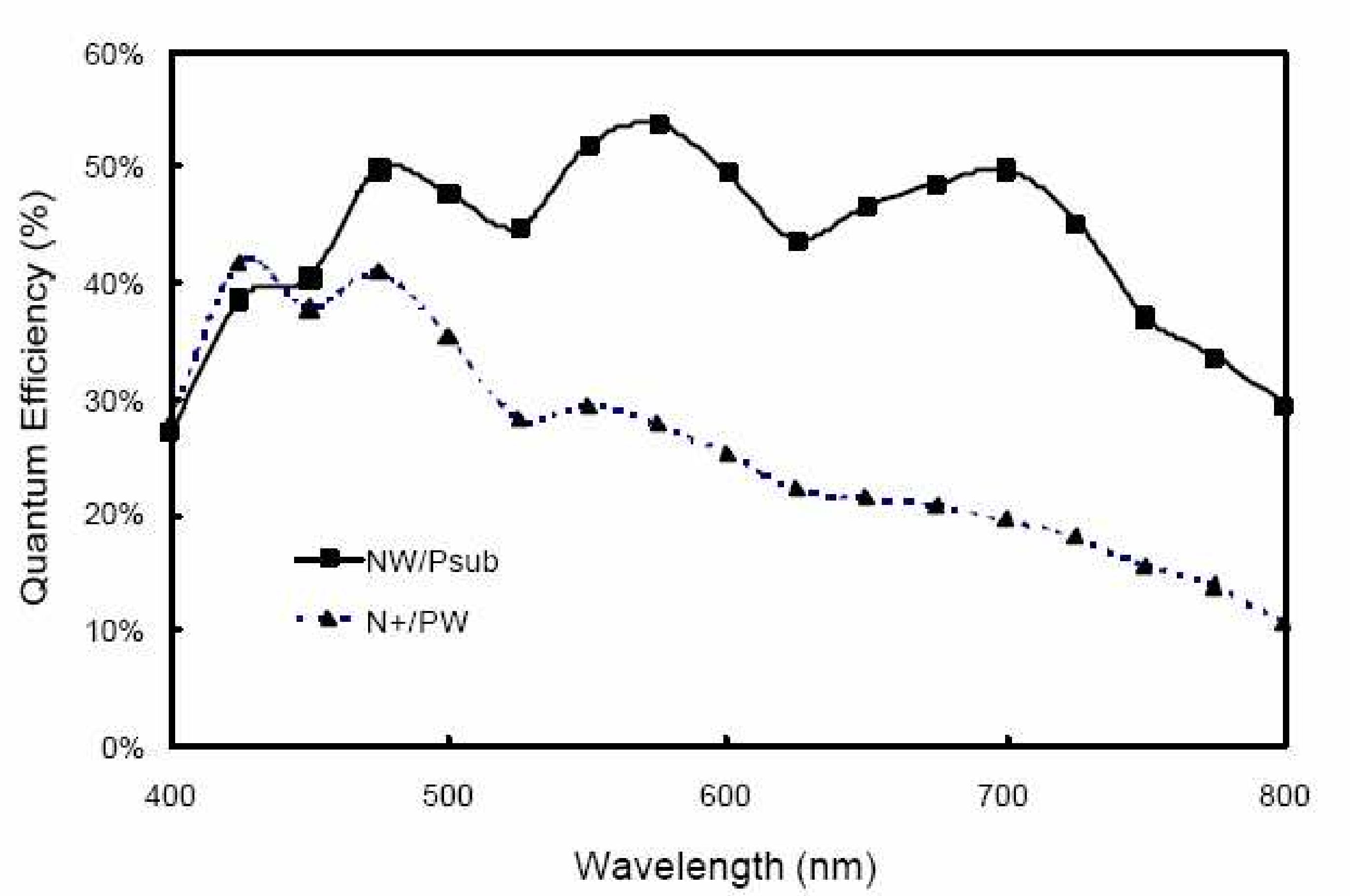




D.-N. Yaung et al., "Nonsilicide source/drain pixel for 0.25 μm CMOS image sensor," IEEE Electron Device Letters., pp. 71-73 (2001)

N-Well to P-Substrate Photodiode

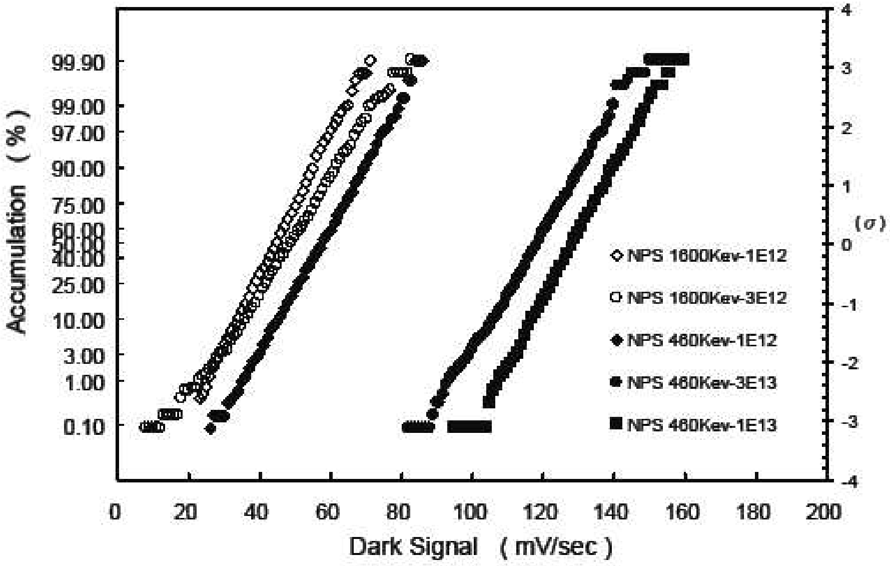
- Higher quantum efficiency due to deeper junction

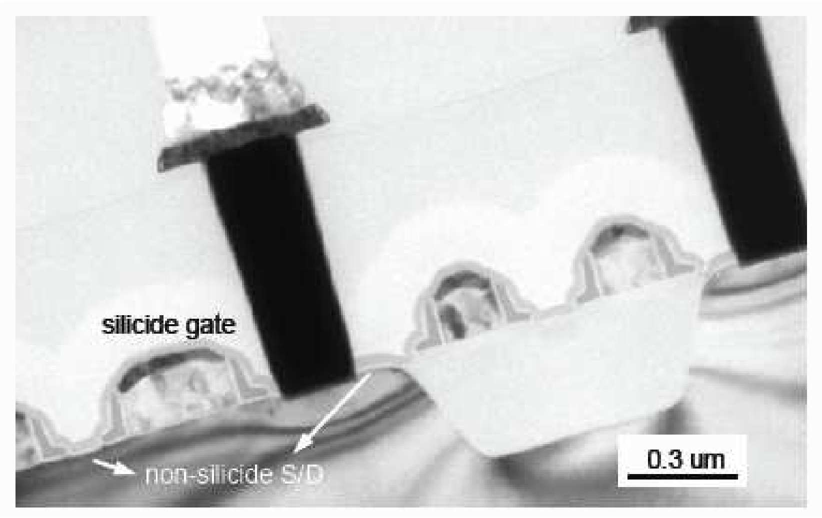


S.G. Wuu et al., "High performance 0.25 μm CMOS color imager technology with non-silicide source/drain pixel," IEDM Tech. Dig., pp. 705-708 (2000)

N-Well to P-Substrate Photodiode Under STI

- Deep (2.5 μm) n-well (MeV) implant, light dose
- Light collection region under STI

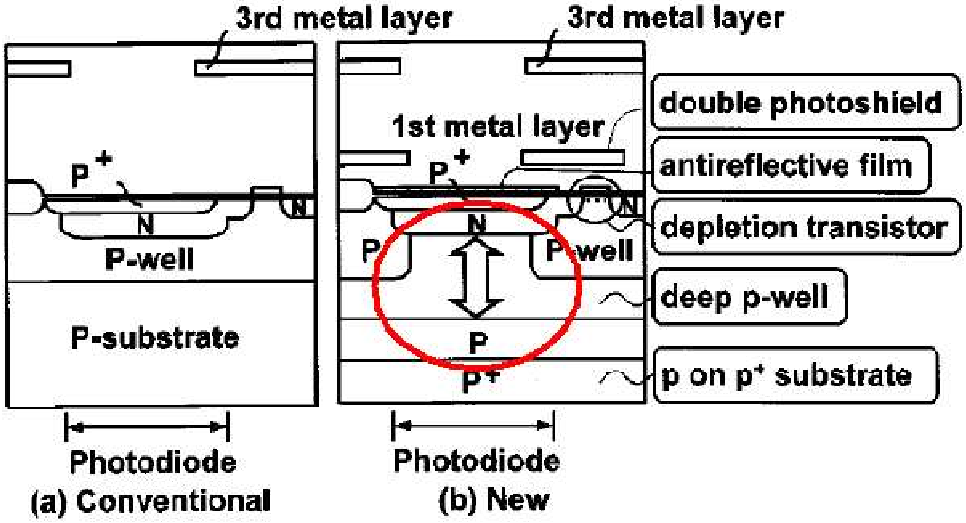




S.G. Wuu et al., "A high performance active pixel sensor with 0.18 μm CMOS color imager technology," IEDM Tech. Dig., pp. 555-558 (2001)

Epi Substrate Thickness Tailoring

- P+-substrate (more costly) cuts down on carrier diffusion due to red and infra-red light because diffusion length in heavily doped semiconductor is short
- Typical p-epi on p+-substrate is $< 2\ \mu$m, not deep enough for good green/red light absorption
- Epi-layer too thick causes crosstalk



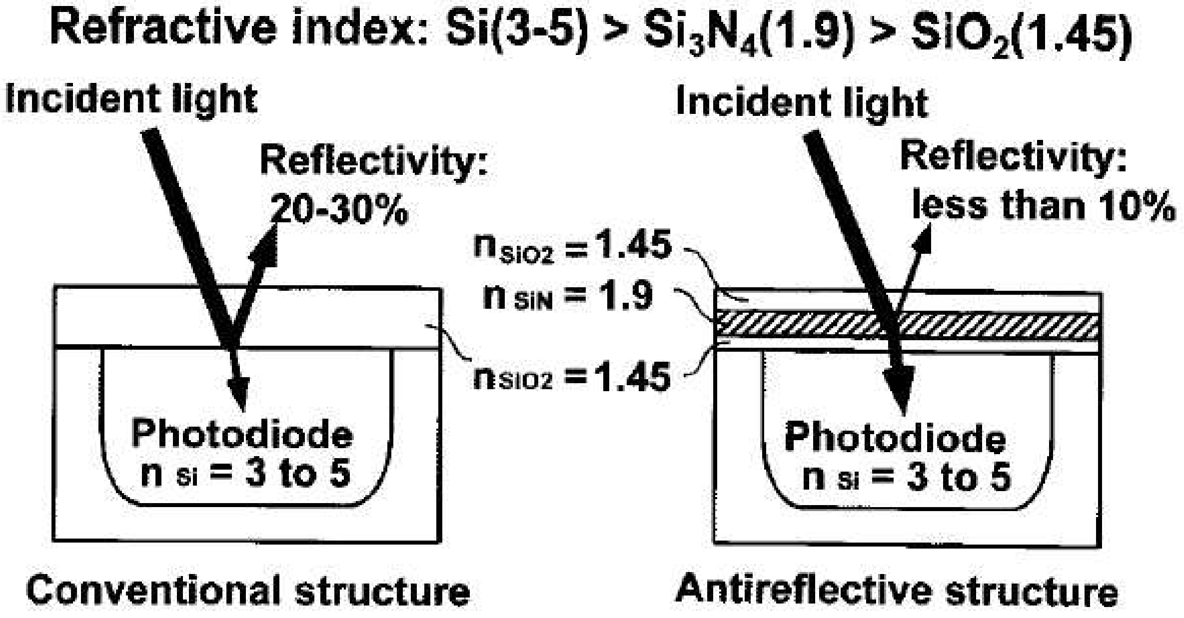
(a) Conventional

(b) New

M. Furumiya et al., "High sensitivity and no-crosstalk pixel technology for embedded CMOS image sensor," IEEE Trans. Electron Devices, pp. 2221-2227 (2001)

Customized Back-End Dielectrics

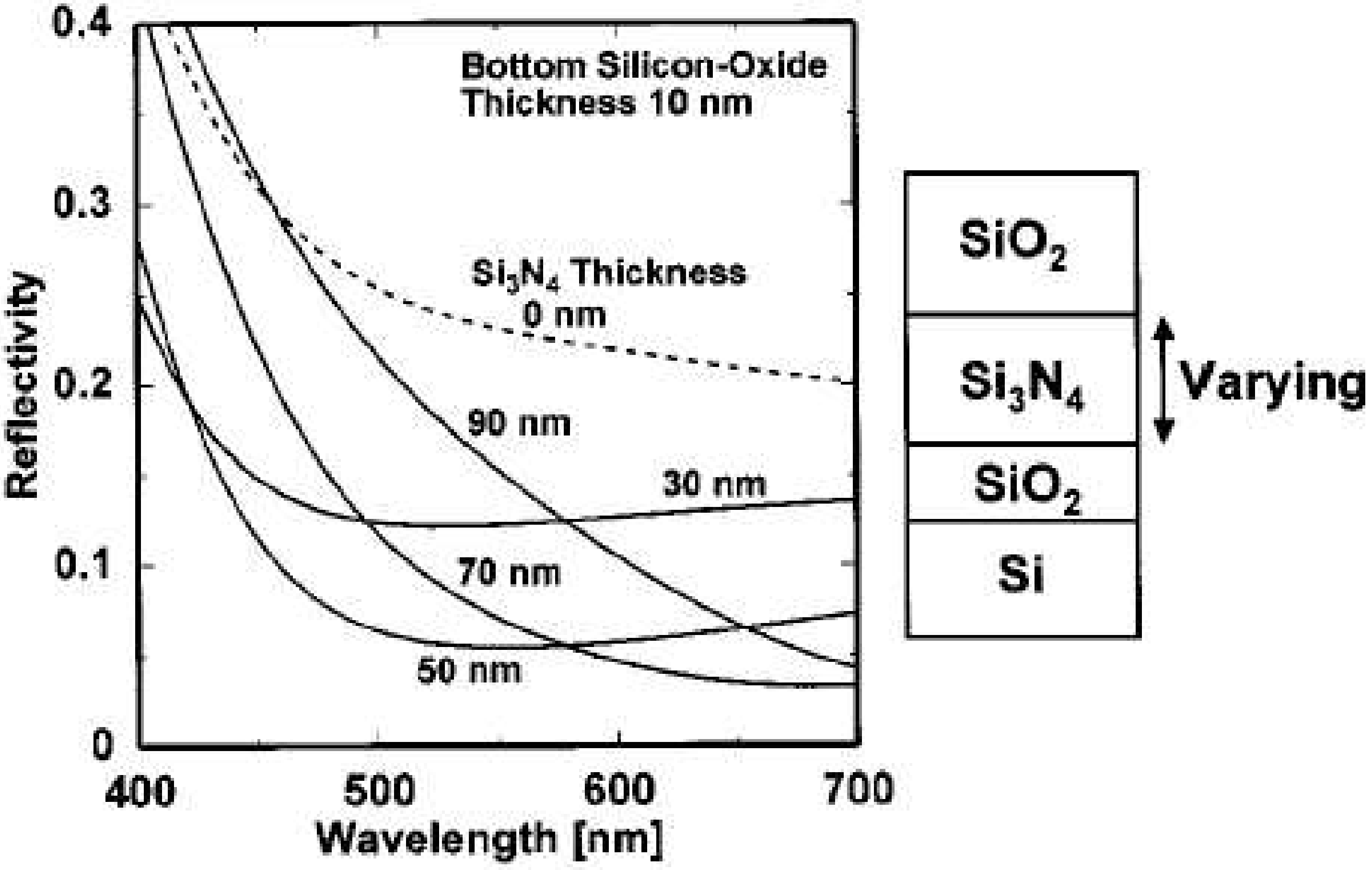
- Grade the refractive index, match refractive index at boundaries as far as possible
- Dielectrics: Si_3N_4, PECVD oxide, silicon-rich oxide, SiO_2, PECVD nitride
  - Make sure dielectrics are not light absorbing



M. Furumiya et al., "High sensitivity and no-crosstalk pixel technology for embedded CMOS image sensor," IEEE Trans. Electron Devices, pp. 2221-2227 (2001)

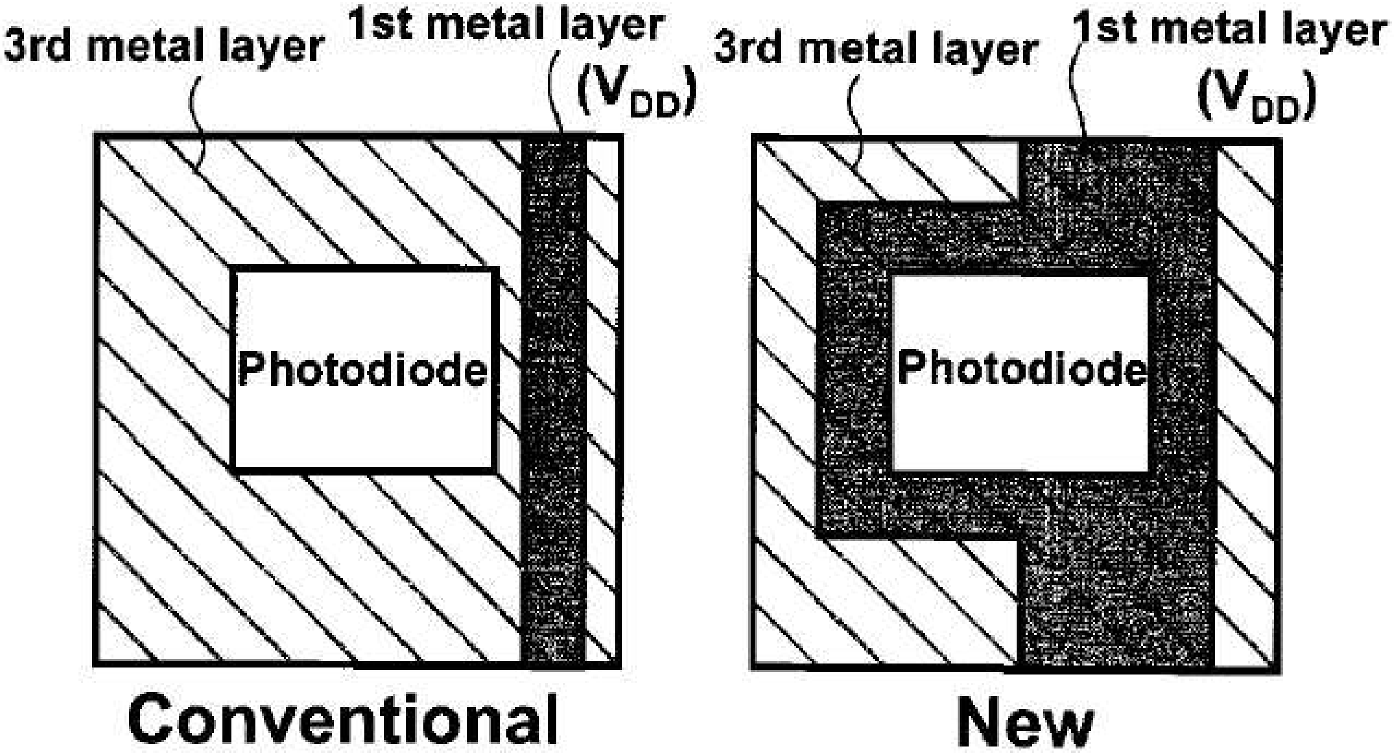
Dielectric Thickness Optimization

- Wavelength dependent due to multiple reflections



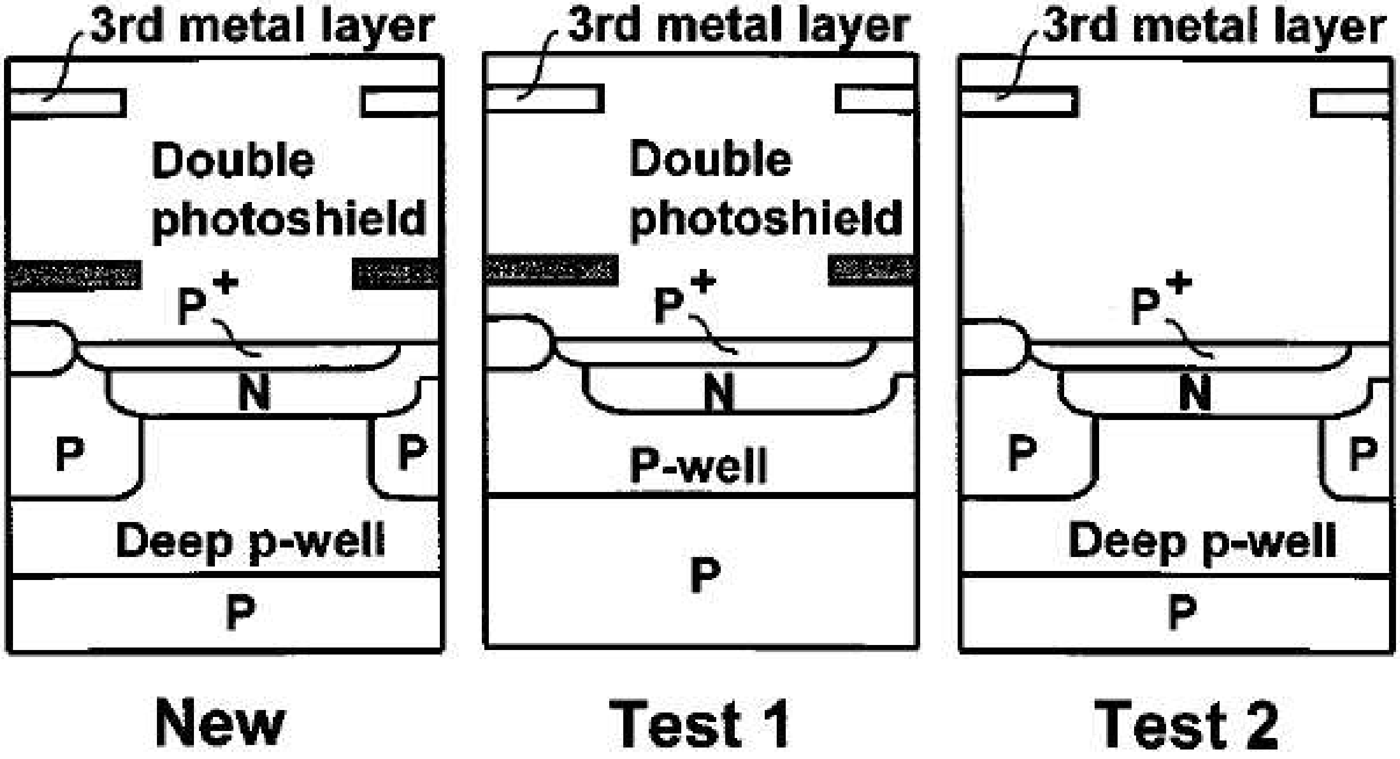
M. Furumiya et al., "High sensitivity and no-crosstalk pixel technology for embedded CMOS image sensor," IEEE Trans. Electron Devices, pp. 2221-2227 (2001)

Tight Metal Light Shield



M. Furumiya et al., "High sensitivity and no-crosstalk pixel technology for embedded CMOS image sensor," IEEE Trans. Electron Devices, pp. 2221-2227 (2001)

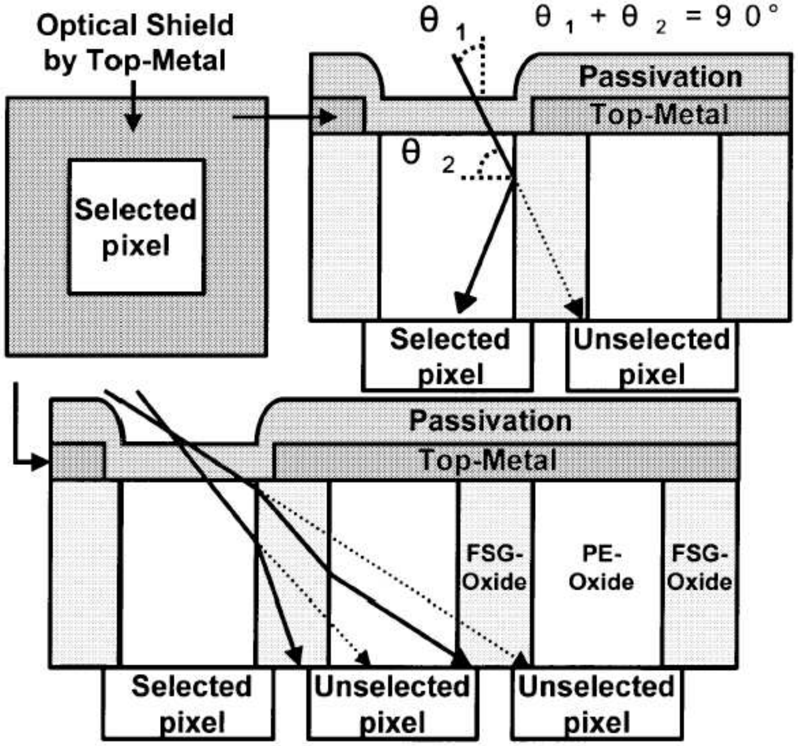
Lower The Metal Light Shield Height



M. Furumiya et al., “High sensitivity and no-crosstalk pixel technology for embedded CMOS image sensor,” IEEE Trans. Electron Devices, pp. 2221-2227 (2001)

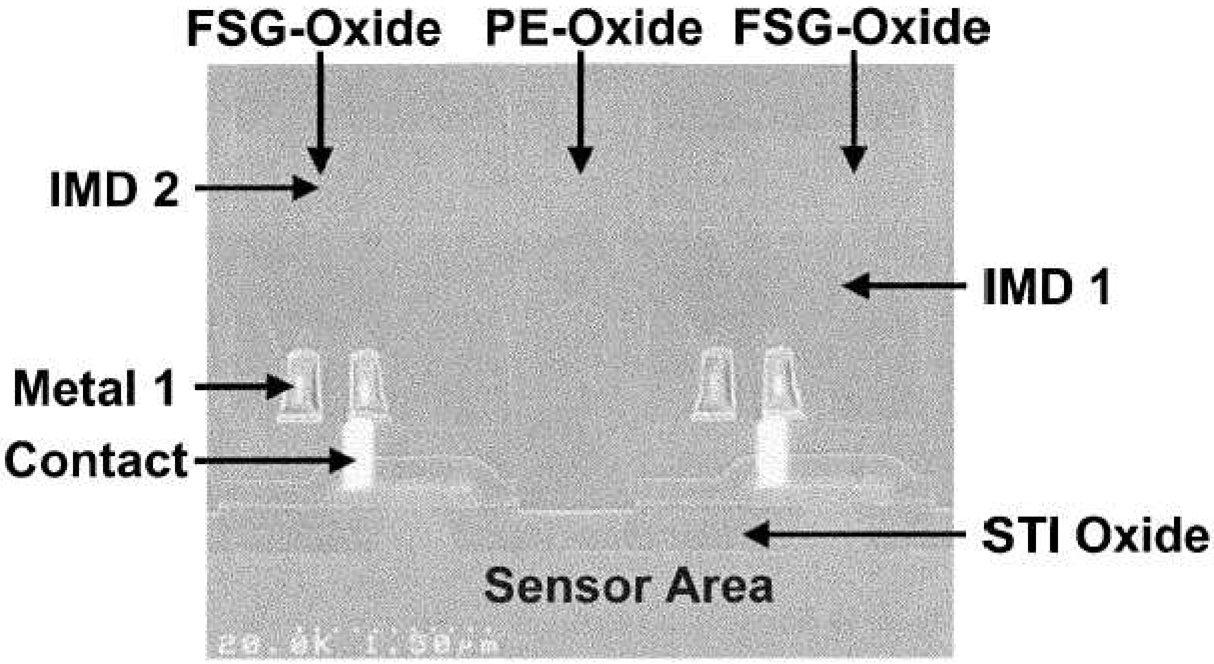
Optical Path Optimization at the Backend

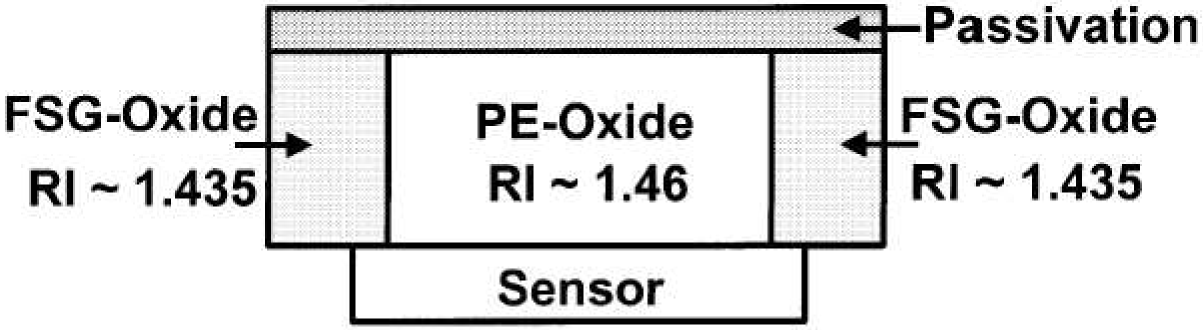
- Utilize different dielectric refractive index to achieve total internal reflection
- Snell's law: $n_1 \sin\theta_1 = n_2 \sin\theta_2$



T.H. Hsu et al., "Light guide for pixel crosstalk improvement in deep submicron CMOS image sensor," IEEE Electron Device Letters, pp. 22-24 (2004)

Optical Path Optimization at the Backend





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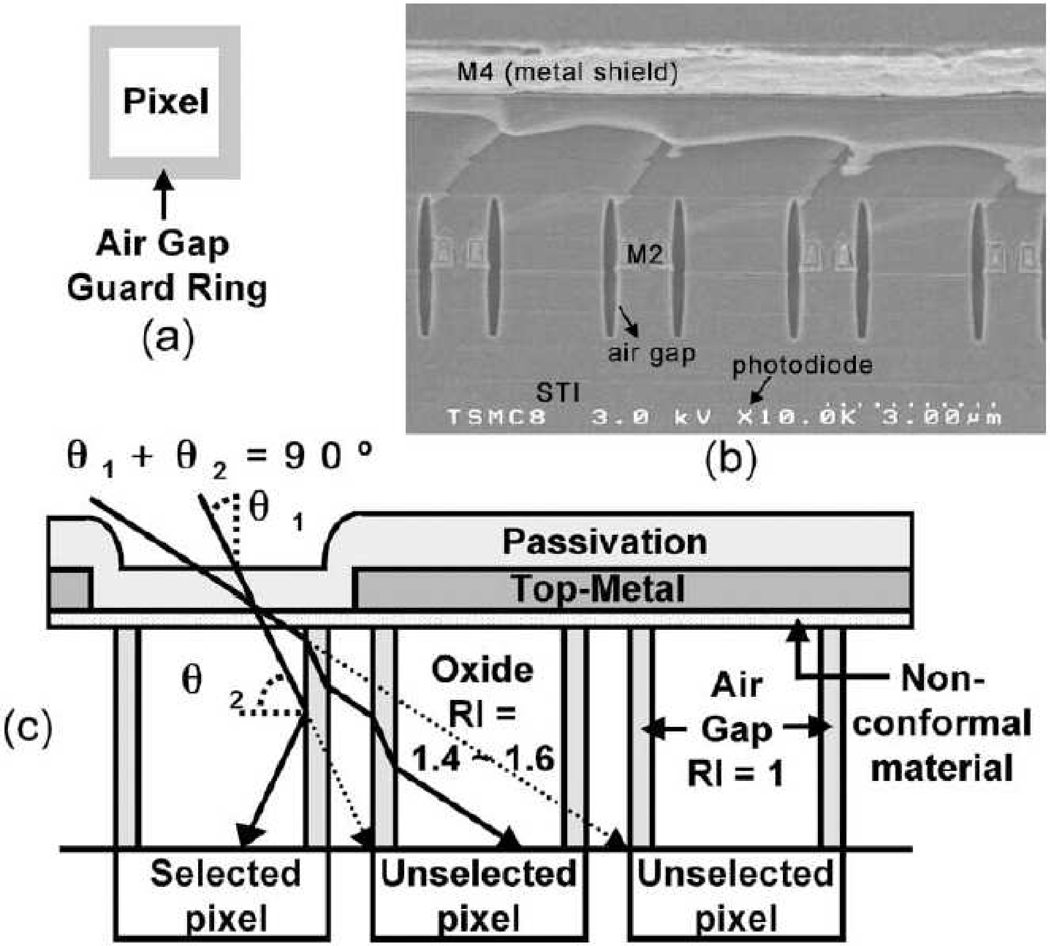
Air Gap Guard Ring

- An extension of the total internal reflection concept

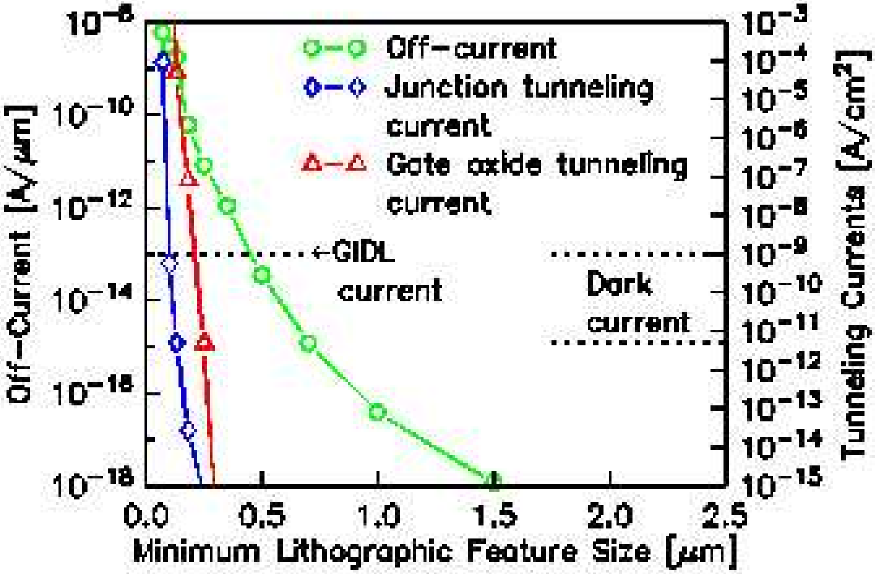


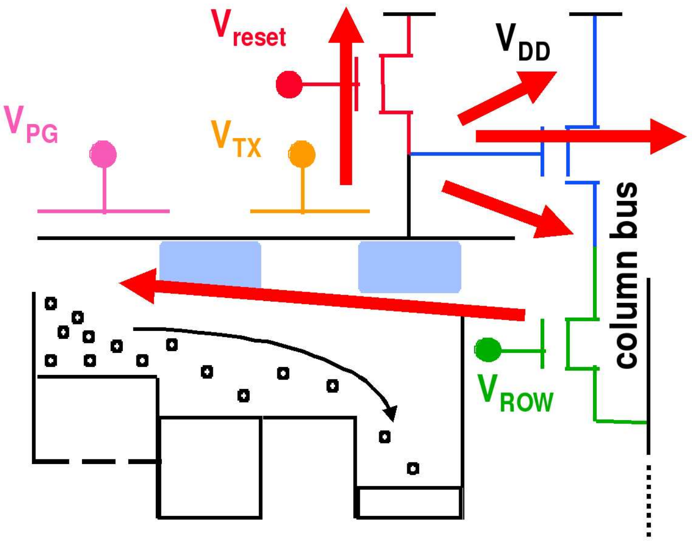
T.H. Hsu et al., "Dramatic reduction of optical crosstalk in deep-submicrometer CMOS imager with air gap guard ring," IEEE Electron Device Letters, pp. 375-377 (2004)

Leakage Current

- Charge leakage from high impedance node during signal integration or readout
- Sources:
  - Diffusion current (proportional to n_i^2)
  - Generation current in space charge region (proportional to n_i)
  - PN junction tunneling current (band to band tunneling)
  - Off-current – subthreshold conduction due to low v_T
  - Gate current – important at $<$ 130 nm node
  - Hot-carrier effects – present for transistors operated in the saturation region
  - Defect generated leakage – process stress (strained silicon, STI, silicide, contact etch)

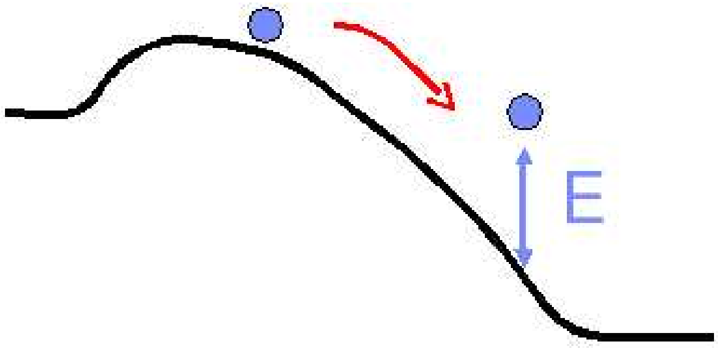
Leakage Current





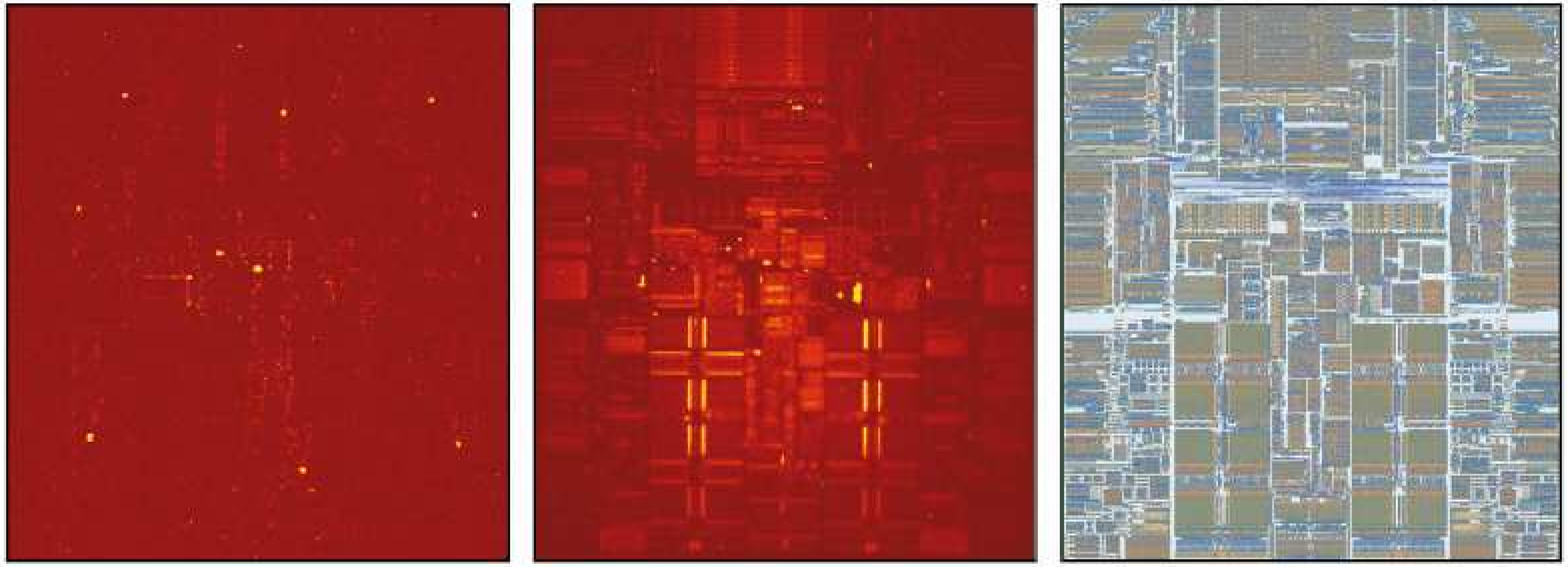
H.-S. P. Wong, “Technology and Device Scaling Considerations for CMOS Imagers,” pp. 2131-2146 (1996)

Hot Carriers



- Carriers gain energy as they travel along the channel
- Why are carriers called “hot” carriers?
  - The energy of the carriers can be described by a carrier distribution characterized by a “temperature” that is higher than the lattice temperature, hence the term “hot” carriers
- Two main effects caused by hot-carriers
  - Impact ionization, generates electron-hole pairs
  - Photon emission

Device In Saturation Region Will Emit Light



(a) (b) (c)

Figure 15

Time-integrated images of switching-induced light emission from a CMOS microprocessor chip under different excitation conditions (a) and (b). Image (c) is a computer rendering of the chip layout.

J. C. Tsang, J. A. Kash, D. P. Vallett, IBM J. Research and Development, vol. 44, p. 583 (2000)

Hot-Carrier Induced Photon Emission

- Intra-band (conduction band) transition – only for nFETs
- Photons generated in the infra-red wavelengths
- Photons travel quite far in the silicon substrate
- PN junction guard ring is not effective in isolating pixel from photons
    - PN junction guard ring is useful to block electrons from impact ionization

Optimized STI Process

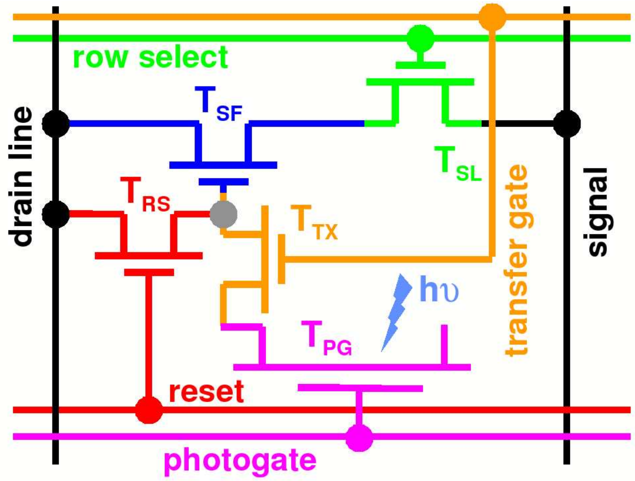
- Gentle STI etch
- Reduce STI dielectric stress (engineer the liner) induced defects (stacking faults)
- Implant p+ doped region around STI to push electrons away from STI surface

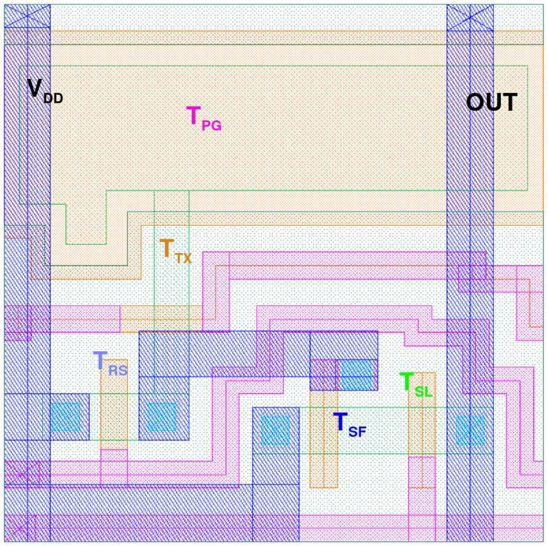
Transistor Design

- Pixel transistors
  - High v_{DD} to provide signal swing headroom
  - Thick oxide to handle higher v_{DD} and reduce gate leakage
  - Boosted Reset Gate voltage for hard reset
  - Avoid hot-carrier generation using longer than minimum devices
  - v_T adjustments
    - Higher v_T for reset transistor
    - Lower v_T for source follower transistor
- Peripheral transistors
  - Standard CMOS logic transistors to reduce power consumption and attain high circuit speed
- Similar strategy as DRAM
  - Separate "array" transistors, and "support circuit" transistors

Pixel Layout and Pixel Size

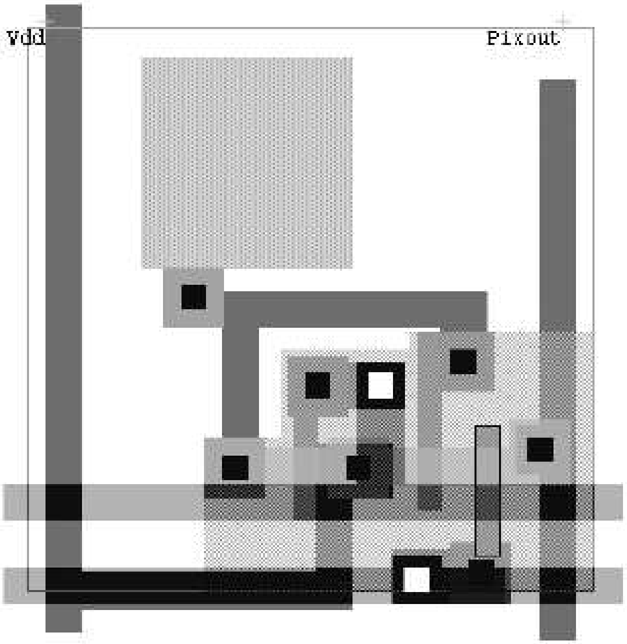
- Pixel size mostly determined by
  - Contact size
  - Poly-gate to contact spacing
  - Metal to metal spacing
- 20F for 4T cell
- 13-16F for 3T cell

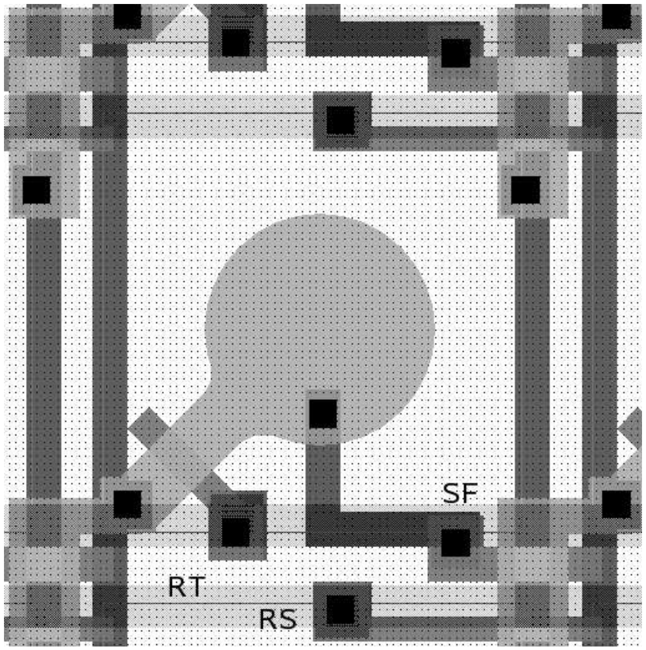




Pixel Layout Examples – 3T Photodiode

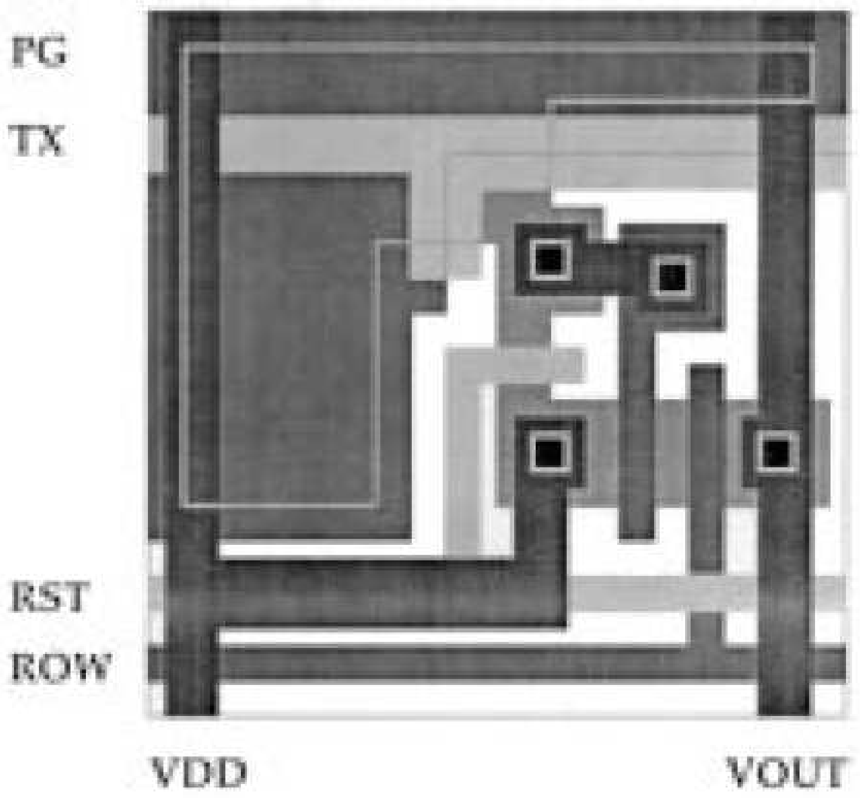
- Maximum photodiode area may not give the best imaging performance
  - Leakage, conversion gain





A. I. Krymski, N. E. Bock, N. Tu, D. Van Blerkom, and E. R. Fossum, “A high-speed, 240-frames/s, 4.1-Mpixel CMOS sensor,” IEEE Trans. Electron Devices, Vol. 50, pp. 130-135, January 2003
I. Shcherback, O. Yadid-Pecht, “Photoresponse analysis and pixel shape optimization for CMOS active pixel sensors,” IEEE Trans. Electron Devices, pp. 12-18 (2003)

Pixel Layout Examples – 4T-Photogate

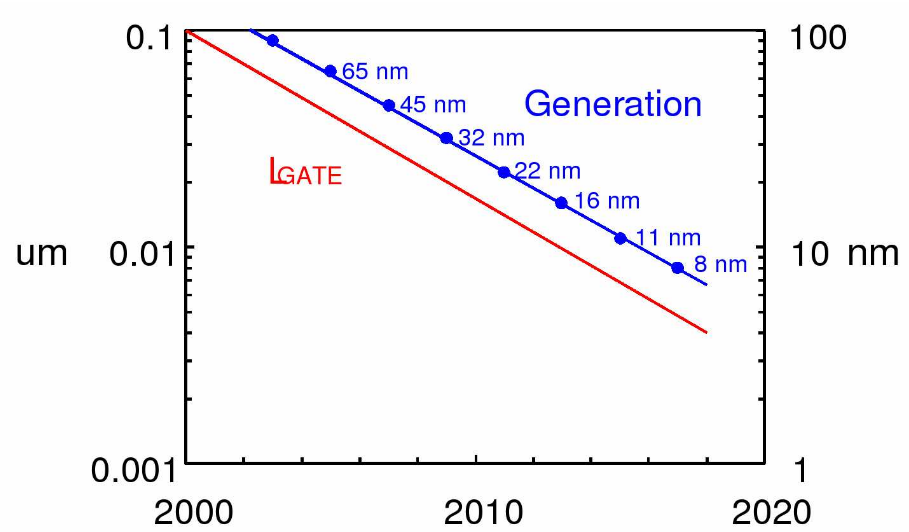


S. K. Mendis, S. E. Kemeny, R. C. Gee, B. Pain, C. O. Staller, Q. Kim, and E. R. Fossum, "CMOS active pixel image sensors for highly integrated imaging systems," IEEE Journal of Solid-State Circuits, vol. 32, pp. 187-197, February 1997

Technology Scaling

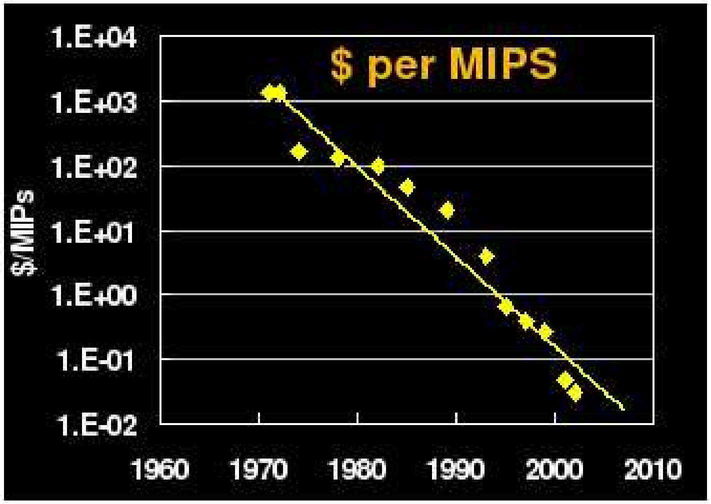
- Today's advanced CMOS image sensors are fabricated in 0.18 μm CMOS
- Most advanced logic technology is 90 nm (will be 65 nm in 2006)
- Can CMOS image sensor use nanometer scale CMOS technologies?

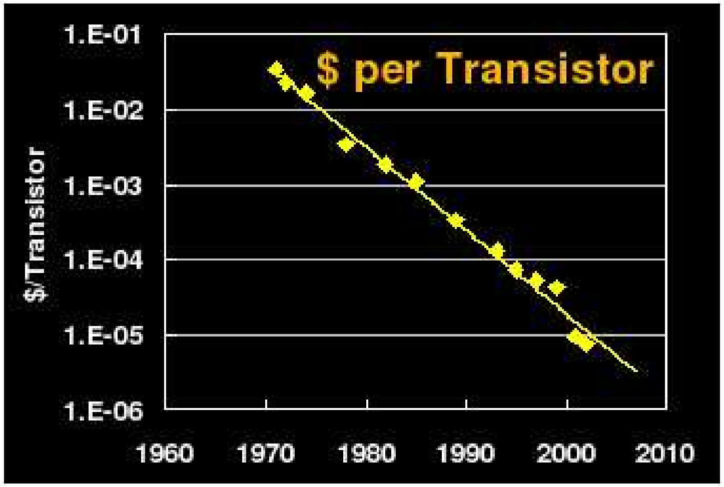
Technology Trends



Source: M. Bohr, Intel (2003)

Source: G. Moore, Intel (2003)

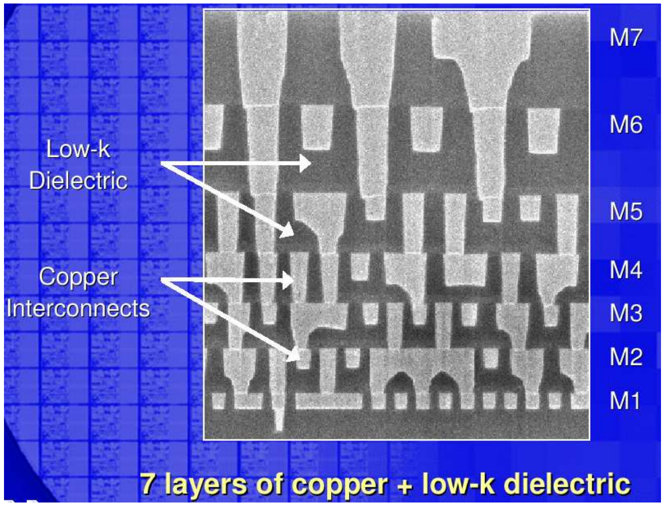




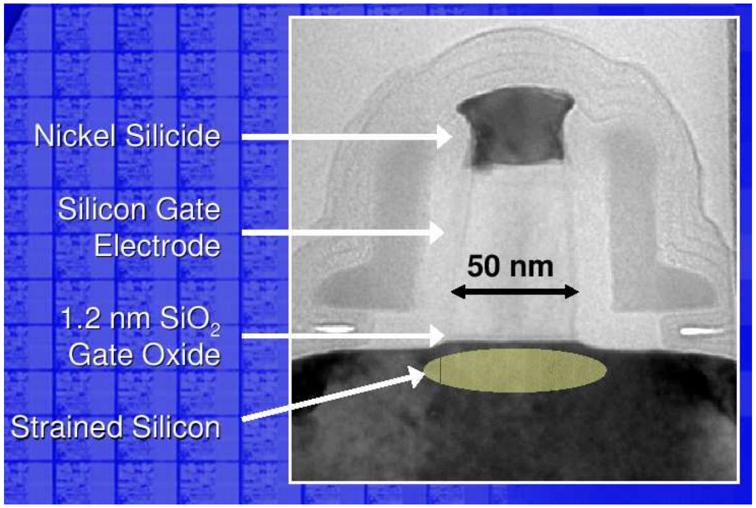
Source: P. Gelsinger, Intel (2003)

State-of-the-Art Technology

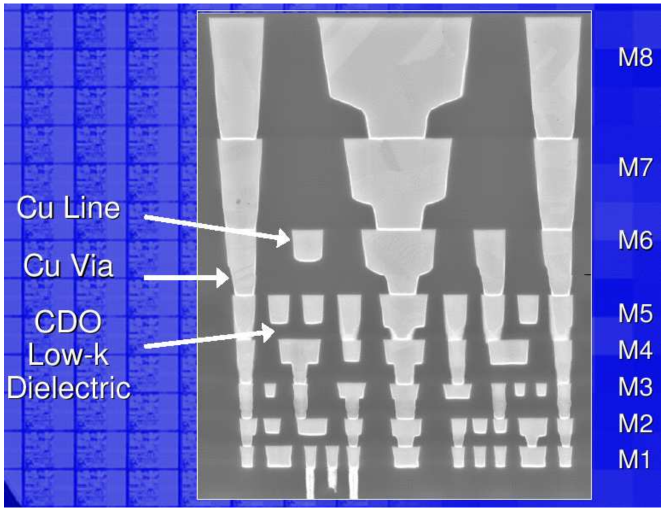
90 nm

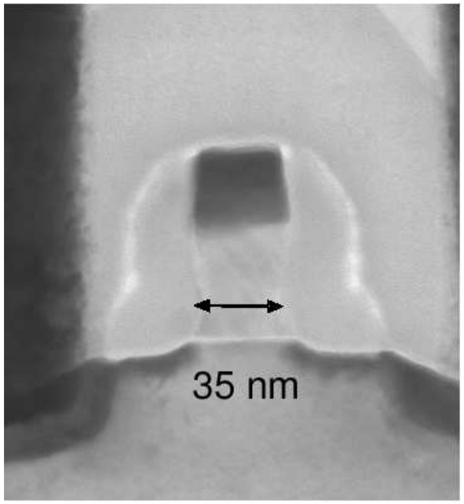


7 layers of copper + low-k dielectric



65 nm





Source: M. Bohr, Intel (2004)

Benefits of Scaling

- More devices per unit area
- Higher gate leakage
- Higher subthreshold leakage
- Lower power supply voltage

Scaling Examples

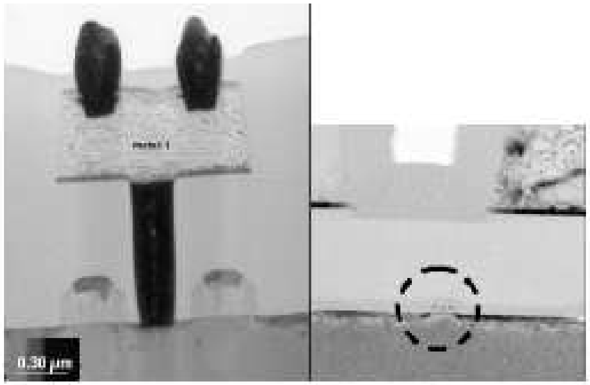
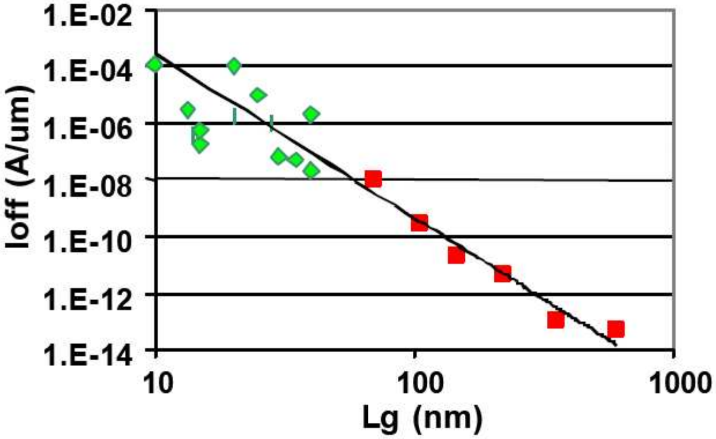
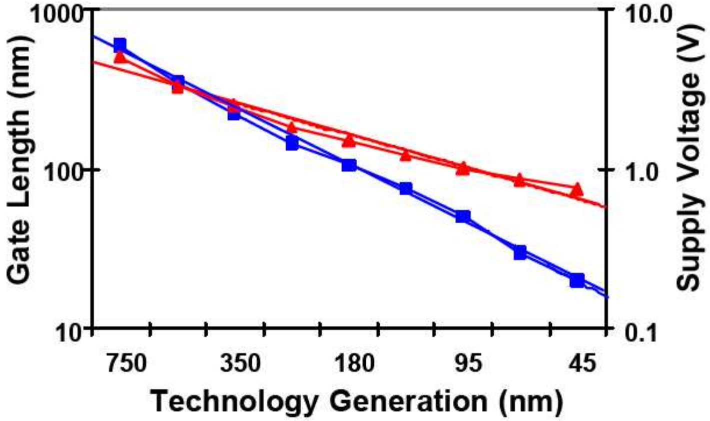
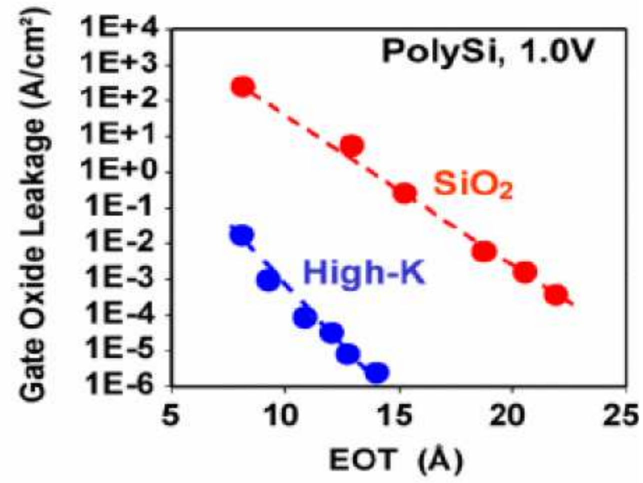


Figure 12: 0.18um technology node transistors (left), with 10nm transistor (circled on right) on the same scale







B. Doyle et al., “Transistor elements for 30 nm physical gate length and beyond,” Intel Technology Journal, pp. 42-54 (2002)

Scaling for CMOS Image Sensor

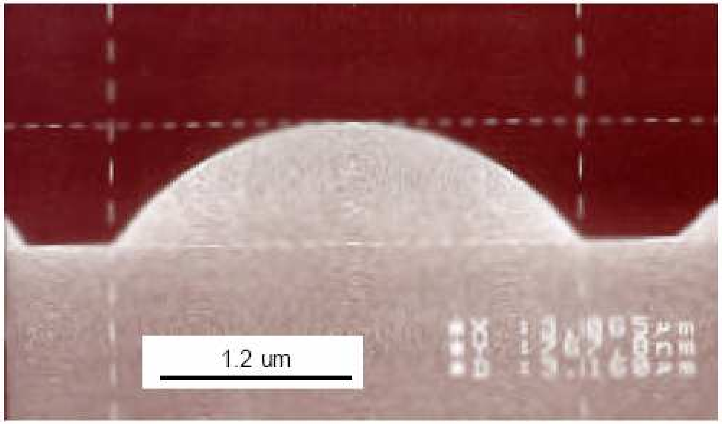
- Straight-forward scaling does not work for CMOS image sensors
- Photogate and photodiode collection region too shallow
- Leakage too high
  - Gate dielectric, subthreshold current, pn junction band to band tunneling,
- Power supply too low

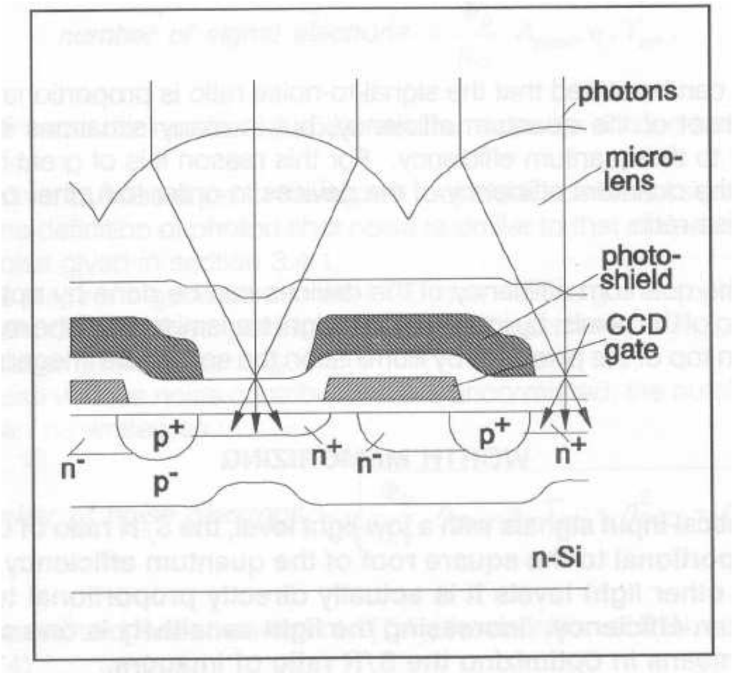
Industry Trends

- Most CMOS image sensors uses 0.18 μm CMOS
    - 3.3V, thick oxide transistors for the pixel
- Pinned photodiode for CMOS image sensors (at low voltage)
- Cu backend to reduce dielectric stack height
- Migration to 0.13 μm CMOS may need substantial process changes
- Pixel size reduction to 2 μm driven mostly by cost

Microlens

- Focus light onto photo-sensitive region – increases effective fill factor from 25-40% to 60-80% (and sensitivity by $\geq$ 2X)
- Less effective if photosensitive area is irregularly shaped



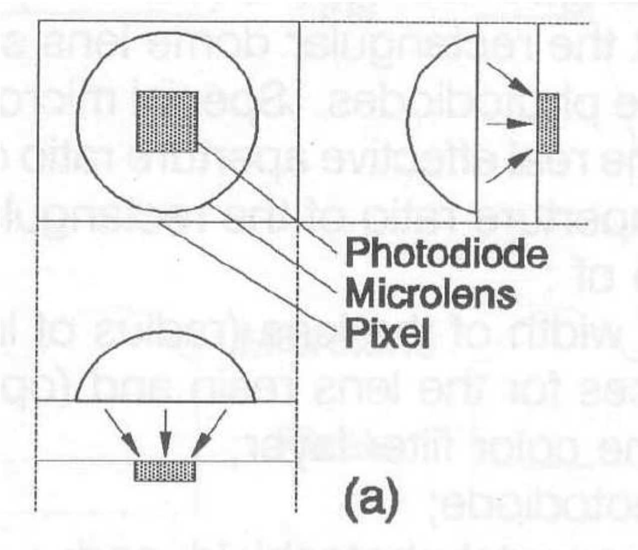


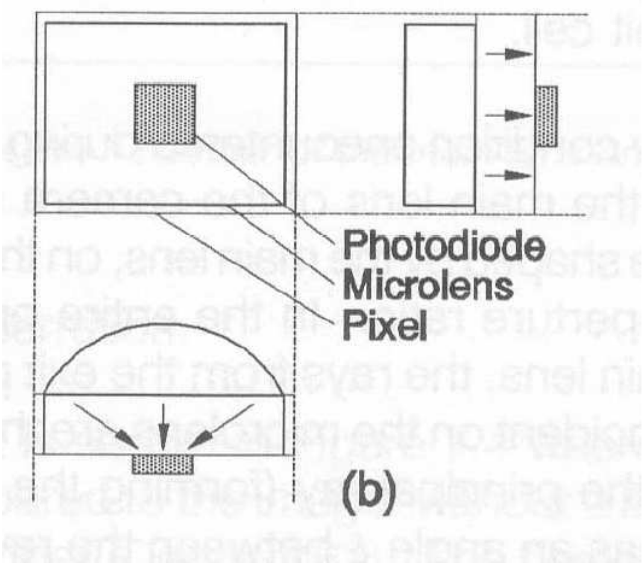
A. Theuwissen, “Solid State Imaging with Charge-Coupled Devices,” Kluwer (1995)

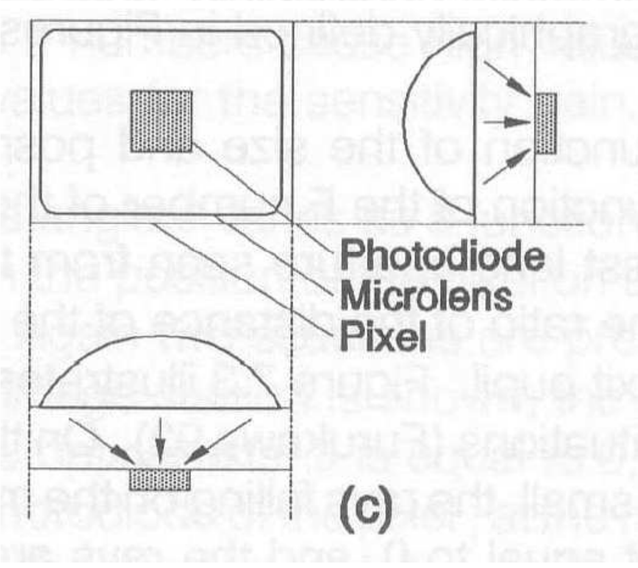
S.G. Wuu et al., “High performance 0.25 μm CMOS color imager technology with non-silicide source/drain pixel,” IEDM Tech. Dig., pp. 705-708 (2000)

Microlens Types

- (a) Hemispherical lens
- (b) Semi-cylindrical lens
- (c) Rectangular dome lens



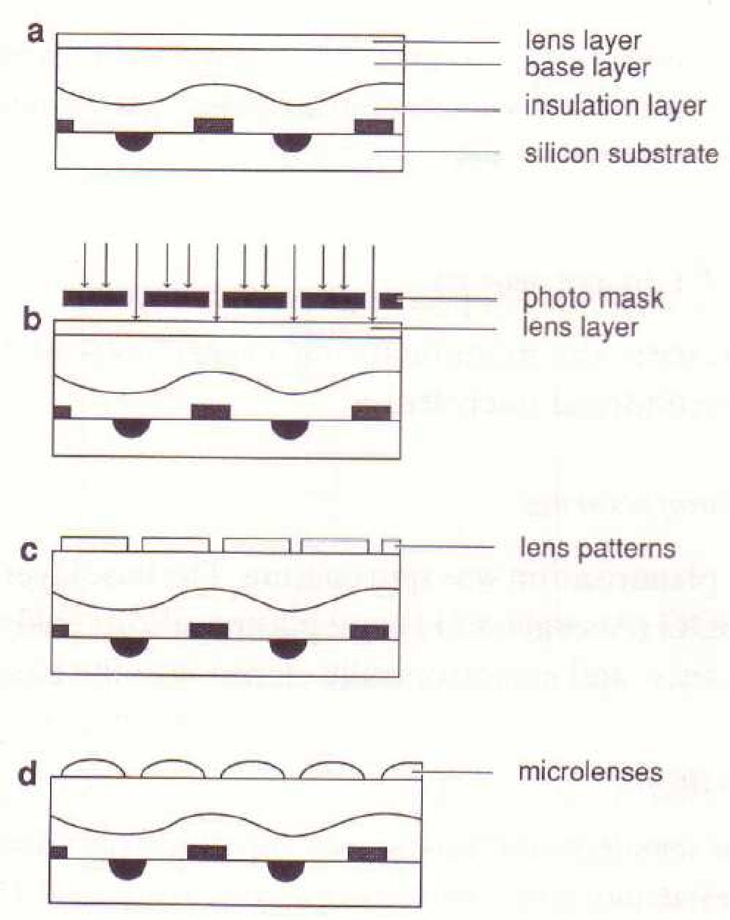




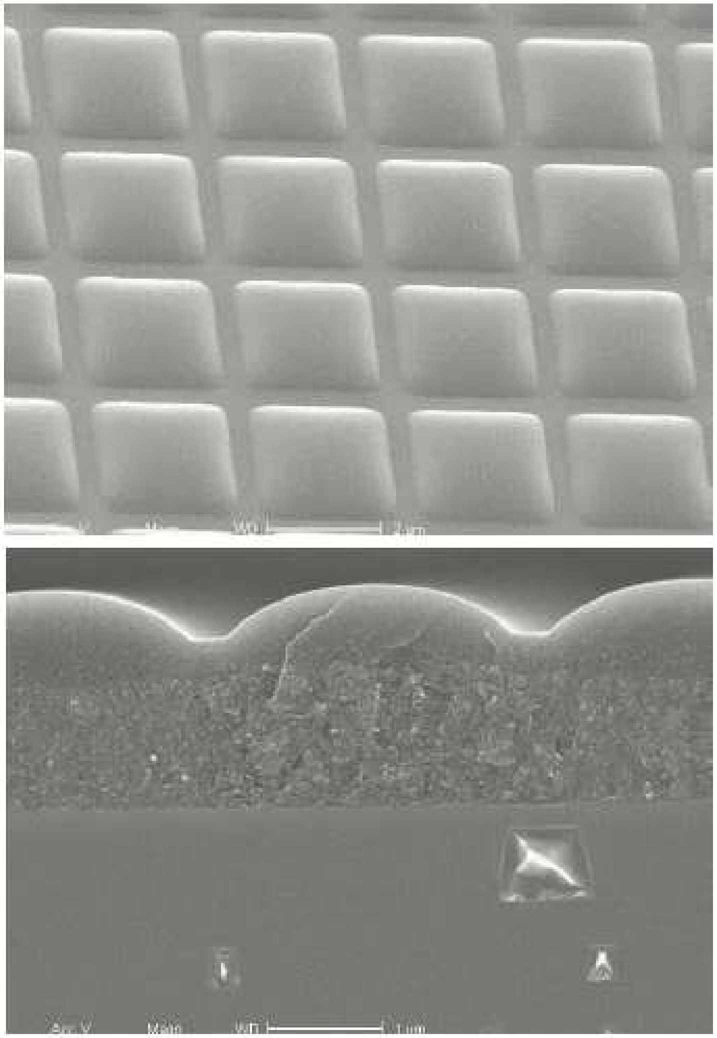
A. Theuwissen, "Solid State Imaging with Charge-Coupled Devices," Kluwer (1995)

Microlens Fabrication

- Lens material requirements:
    - ○ Highly transparent in the visible light region
    - ○ Index of refraction > 1.59
    - ○ Can be applied below 500C
    - ○ No degradation or aging
    - ○ Semiconductor processing compatible
    - ○ Can be patterned with feature size commensurate with the pixel size
- Lens materials are typically i-line or DUV resists
- Base materials are acrylic-based resists, polyimide resists, epoxy resists, polyorganosiloxane, polyorganosilicate



Example CMOS Image Sensor Chip

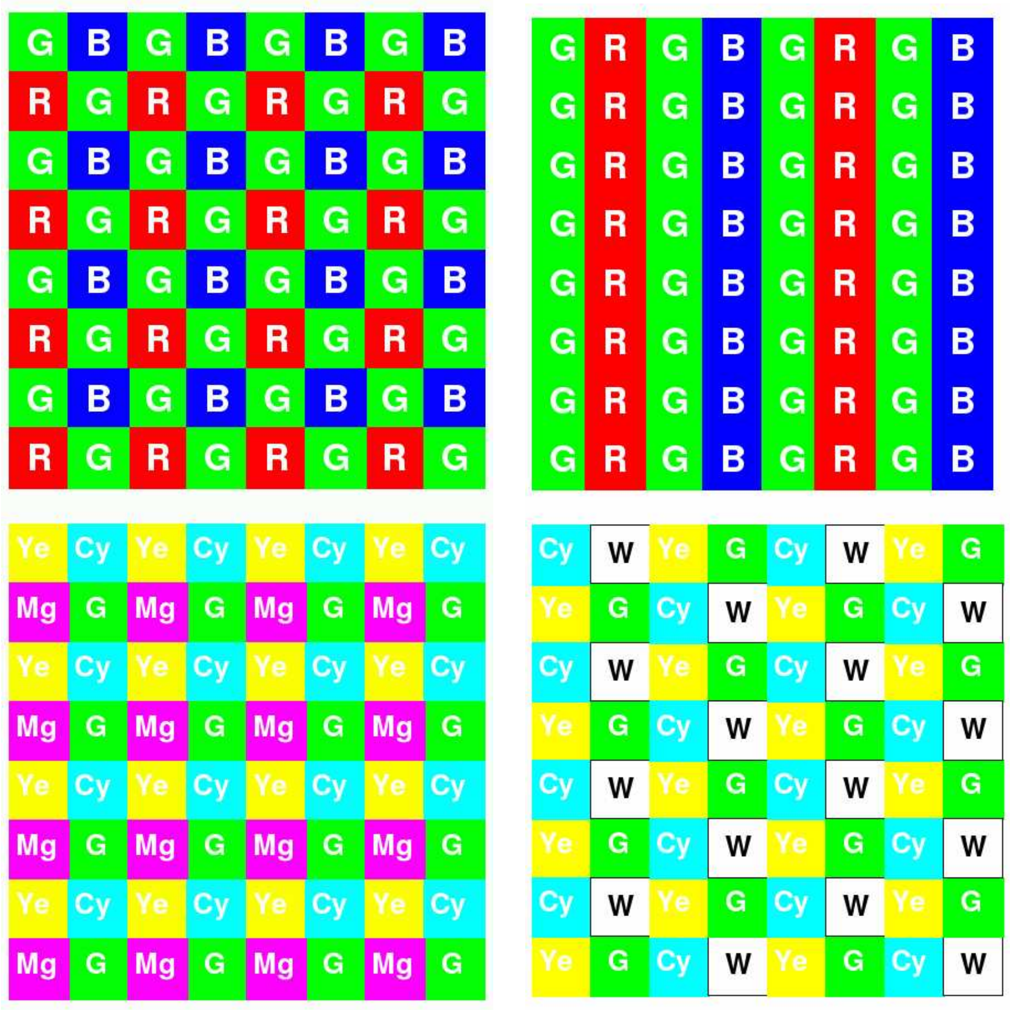


H. Rhodes et al., “CMOS imager technology shrinks and image performance,” IEEE Workshop on Microelectronics and Electron Devices, pp.7-18 (2004)

On-Chip Color Filter Arrays

Bayer

Stripe



Bayer

G	B	G	B	G	B	G	B
R	G	R	G	R	G	R	G
G	B	G	B	G	B	G	B
R	G	R	G	R	G	R	G
G	B	G	B	G	B	G	B
R	G	R	G	R	G	R	G
G	B	G	B	G	B	G	B
R	G	R	G	R	G	R	G

Stripe

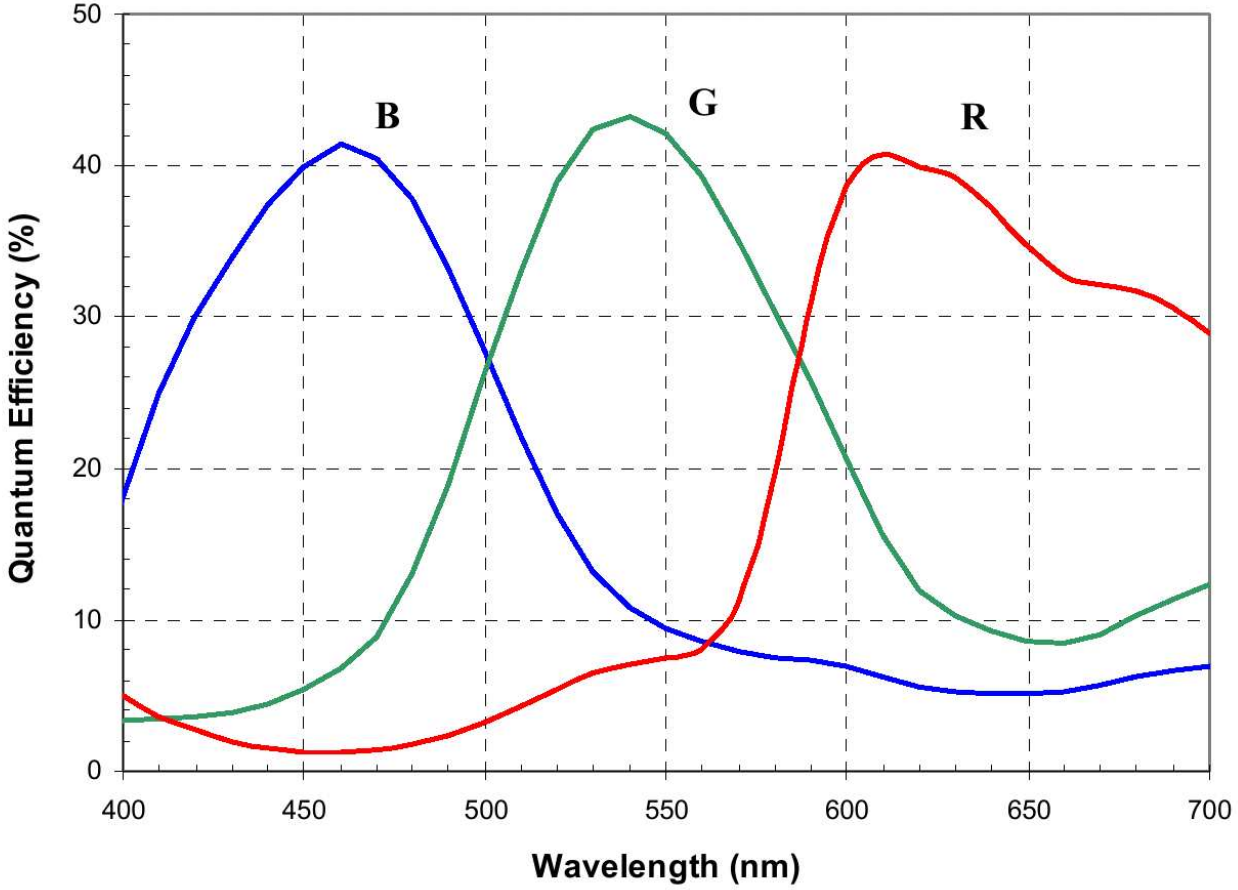
G	R	G	B	G	R	G	B
G	R	G	B	G	R	G	B
G	R	G	B	G	R	G	B
G	R	G	B	G	R	G	B
G	R	G	B	G	R	G	B
G	R	G	B	G	R	G	B
G	R	G	B	G	R	G	B
G	R	G	B	G	R	G	B

Ye	Cy	Ye	Cy	Ye	Cy	Ye	Cy
Mg	G	Mg	G	Mg	G	Mg	G
Ye	Cy	Ye	Cy	Ye	Cy	Ye	Cy
Mg	G	Mg	G	Mg	G	Mg	G
Ye	Cy	Ye	Cy	Ye	Cy	Ye	Cy
Mg	G	Mg	G	Mg	G	Mg	G
Ye	Cy	Ye	Cy	Ye	Cy	Ye	Cy
Mg	G	Mg	G	Mg	G	Mg	G

Cy	W	Ye	G	Cy	W	Ye	G
Ye	G	Cy	W	Ye	G	Cy	W
Cy	W	Ye	G	Cy	W	Ye	G
Ye	G	Cy	W	Ye	G	Cy	W
Cy	W	Ye	G	Cy	W	Ye	G
Ye	G	Cy	W	Ye	G	Cy	W
Cy	W	Ye	G	Cy	W	Ye	G
Ye	G	Cy	W	Ye	G	Cy	W

K. Parulski, IEEE Trans. Electron Devices, p. 1381, 1985

Example Color Filter Spectral Response



- This data includes the spectral response of both the sensor and CFA

H. Rhodes et al., "CMOS imager technology shrinks and image performance," IEEE Workshop on Microelectronics and Electron Devices, pp.7-18 (2004)

On-Chip Color Filter Array Fabrication

- Color filter materials are dyed photoresists
- Fabrication steps:
    - Spin coat
    - Soft bake
    - Expose
    - Develop
    - Cure
    - Repeat for other colors