memories by showing the possibility of using a printed circuit transformer which could be economical as a mass-produced device. It seems reasonable to assume that the additional cost of the transformer will be a small percentage of the cost of the tunnel diode, but only for air core printed circuit transformers or some other type of batch-fabricated technique.

The requirements on the transformer tend to limit the application to very high speeds. Fortunately, the major use of such a memory is at high speeds. A clever feature of the authors' word circuitry is the use of a differentiating transformer driven with a triangular current to generate the bipolar word pulse. This is compatible with the low volt-second capability of practical transformers for this memory. Some additional data on the transformer would have been useful, particularly that relating to the size and packaging problems of a large number in a practical array.

The new arrangement gives rise to some desirable operating advantages. The word and bit circuits are now completely independent from a dc standpoint, and sneak paths, common voltage point, and ground-coupled noise should be significantly reduced. Because of this independence, basically simple and straightforward drive and sense circuitry is possible.

The authors have described their work on the high-speed version (20-nsec cycle time) as a series of critical experiments and they point out (wisely) that things often are different in a fully populated memory. Some things that tend to be worse in a complete memory array are noise coupling from the word to the bit line, sense SNR, worst-case digit noise from the digit transition, and cross-coupling from digit line to digit line. These have not been discussed in the authors' paper and are, obviously, of prime importance to a practical memory.

One prime problem area in tunnel diode memories has received no discussion at all: the effect of tolerances of both the tunnel diode and of the applied drive signals. This is the type of thing that will usually "make" or "break" a memory for engineering applications, and it is unfortunate that a discussion was not presented.

In summary, the technique looks interesting and is worthy of more development for small, very high speed tunnel diode memories. It is, in the authors' words, "a fresh and promising attack on the problems associated with high-speed memory design."

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B. BIONICS

R64-42 Simulation of an Assembly of Simplified Nerve Cells on a Digital Computer—R. E. Sears and S. M. Khanna (*Proc. 1963 Fall Joint Computer Conference*).

This paper describes a network of simulated "neurons" having 80 digital inputs, 800 neurons in 10 layers of 80 neurons each, and 80 digital outputs. Each neuron has 11 input signals flowing through variable weights which are intended to simulate variable synapses. There are a total of 8800 synapses in the network. Each neuron has a threshold firing level which decays over time and which is suddenly increased just after firing (giving the effect of a refractory period). The synaptic values are changed in accord with the firings of the neurons to which they are attached. In the experiments described in the paper, various input stimuli are presented to the network, most which are repetitive, and certain initial conditions are utilized. Transient responses of the network under study are shown graphically.

The paper is well written, and is very clear in the nature of the experiments done, the network organization, the nature of the computer simulation program, and the kinds of results obtained. Although the experiments themselves are interesting, they would be much more instructive if some theoretical justification for the observed responses were also presented. Since the authors claim to be modeling certain forms of living neural behavior, it would be helpful if there were more discussion of the relationship between their network and its experimental responses with a corresponding living neural network having similar organization and exhibiting similar responses. The authors claim to be modeling "peripheral processing" in the nervous system. I do not know what this is, and after checking with several neurologists, I cannot get a definition of peripheral processing that would relate at all to the subject of this paper.

The networks under study can actually be thought of as a discrete representation of a two-dimensional continuously-distributed multivibrator. But any basis for directed learning seems to be missing. There is no way of "training" the network or "rewarding" it. The net rewards itself internally for firing, but of what purpose is the firing? Is long-term memory possible in such nets? Is there any way that such nets could do useful things? If not, this would seem to rule them out for being models of portions of living systems.

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C. CIRCUITS

R64-43 Transient Analysis and Device Characterization of ACP Circuits—K. G. Ashar, *et al.* (*IBM J. Res. & Dev.*, vol 7, pp. 207–223; July, 1963.)

This paper presents a comprehensive analysis of the IBM's Advanced Circuit Program (ACP) circuits. Since the design aspect of ACP circuits is discussed in a separate paper published in the same issue of the journal, only the analysis aspects of the circuits and device characterization used is covered here. The analysis of the high-speed switching circuits is performed by a digital computer simulation.

Describing the object and purpose of the paper in its introduction, the paper proceeds to discuss the transistor model and measuring techniques for the parameters to be used.

As the paper mentions, due to the excess phase shift in the transport factor of modern diffused-junction high-speed transistors, the model derived by Ebers and Moll, as well as the original Beaufoy and Spark's charge control model, is inadequate for use in transient analysis of today's high speed switching circuits. Thomas and Moll suggested, in this regard, that a delay factor be added in the single pole approximated gain α of a transistor.

Unfortunately, it is generally quite cumbersome to measure the delay or phase shift factor from the complex plot of α vs frequency; therefore, it is convenient to have a lumped high-frequency key parameter in which the effect of excess phase shift is included. From this consideration, the paper derives a model based on the charge-control concept. The time constant defined by $\Delta Q_b/\Delta I_e$, where Q_b is the charge storage in the base region and I_e is the applied emitter current, is the effective base transit time, and it includes not only the intrinsic pass-band characteristic determined by the base structure and the minority carrier life time, but also the effect of the built-in field in the base region. The paper has proved this fact by deriving the complex α based on the charge equation and by comparing it with Thomas and Moll's equation. Thus, the base storage $Q_b(S)$ is given by

$$Q_b(S) = I_e(S) \Big/ \left(S + \frac{1}{T_e}\right),$$

where T_e is the emitter time constant. This base storage, then, is transformed into collector current $I_c(S)$ by

$$I_c(S) = Q_b(S)/T_c(S)$$

where T_c is the collector time constant. Baker and May suggest the form as

$$T_c(S) = T_c(1 + ST_d),$$

where T_c is the dc base transport factor and T_d is a delay time constant. From above relations, the complex $\alpha(S)$ is given:

$$\alpha(S) = I_c(S)/I_e(S) = \frac{T_c/T_e}{(1 + ST_e)(1 + ST_d)} = \frac{\alpha_0}{(1 + ST_e)(1 + ST_d)},$$

where α_0 is defined T_c/T_e, while from Thomas and Moll's equation,