Techniques for Pixel Level Analog to Digital Conversion

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Approaches to Integrating ADC with Image Sensor

- Chip Level

- Column Level

- Pixel Level
Pixel Level ADC

- Advantages
  - Continuous observation of the pixel
  - Low noise
  - Low power

- Disadvantages
  - Limited area at the pixel level – this becomes less of a problem as technology scales
Outline

⇒ • Architecture
  - $\Sigma \Delta$ ADC
  - MCBS ADC
  - Readout circuitry

• Circuits
  - $\Sigma \Delta$ pixel
  - MCBS pixel

• Results

• Comparision
Pixel Level ADC

- Pixel size limits ADC architecture
- Cannot use conventional bit-parallel ADC techniques, because they require memory at the pixel
- Bit serial ADC is required but conventional techniques are too complicated
- To overcome this problem we developed two bit serial techniques
  - Oversampled
  - Nyquist rate
Oversampled ADC

- Robust operation over process variation and noise
- Simple imprecise circuits can be used
- Use first order 1 bit ΣΔ modulation
  - Requires small silicon area
First Order 1 Bit $\Sigma\Delta$ Modulation

Output decimated using LPF to obtain pixel values - performed off chip.
Oversampling Ratio \( L \) as a function of SNR

Number of bit planes \( L \) per frame for a desired average SNR

\[
\log_2(L) = \frac{\text{SNR} + 5.2\text{dB}}{9.0}
\]

Examples:
- \( \text{SNR} = 48\text{dB} \) (8 bits) \( \Rightarrow \) \( L = 60 \)
- \( \text{SNR} = 20\text{dB} \) (3.3 bits) \( \Rightarrow \) \( L = 7 \)
ΣΔ ADC Limitations

- Increased output bandwidth caused by oversampling
- Decimation/DSP is required to resample the data at the Nyquist frequency
- Poor low light response due to nonuniform quantization
Pixel Level Nyquist Rate ADC

Recently developed a new multi-channel bit-serial (MCBS) ADC technique (Yang, Fowler, El Gamal CICC’98)

- Low output data rate
- Requires very few transistors at the pixel
- Uses very simple circuits
- Complex circuits shared by all pixels
- No external DSP is required to construct image
MCBS ADC

ADC assigns binary codewords to quantization intervals
3-bit example: signal $S \in [0, 1)$

<table>
<thead>
<tr>
<th>Quantization table</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S$</td>
</tr>
<tr>
<td>---</td>
</tr>
<tr>
<td>0</td>
</tr>
<tr>
<td>1/8</td>
</tr>
<tr>
<td>1/4</td>
</tr>
<tr>
<td>1/2</td>
</tr>
<tr>
<td>3/8</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>5/8</td>
</tr>
<tr>
<td>7/8</td>
</tr>
</tbody>
</table>

Key observation: Each output bit can be viewed as a binary-valued function over intervals (independent of other bits!)
Operation of the 1-bit Comparator/Latch

3 Bit LSB Example
MCBS ADC – Block Diagram
MCBS ADC Limitation

The gain bandwidth product must exceed $2F_d \times 4^m$

- To perform $m$ bit quantization at least $2^m - 1$ comparison must be performed
- Assuming uniform quantization, the gain of the comparator must be proportional to $2^m$. 
Block Diagram for Image Sensor with Pixel Level ADC

Sense Amplifiers and Latches
Output of Image Sensor with Pixel Level ADC
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  - MCBS pixel

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Multiplexed $\Sigma \Delta$ Pixel Block Diagram - 17 Transistors
Multiplexed $\Sigma\Delta$ Pixel Block Circuit Schematic - 17
Transistors
ΣΔ ADC Circuit

- Advantages
  - Small size
  - Low sensitivity to transistor noise, and no offset FPN
  - Large charge handling capacity

- Disadvantages
  - Moderate gain FPN
  - Poor low light response
  - High output data rate
MCBS ADC Pixel Block Circuit Schematic - 19

Transistors
MCBS ADC

- **Advantages**
  - Small size
  - Low gain and offset FPN
  - Complete testability

- **Disadvantages**
  - Moderate comparator gain-bandwidth
  - Reduced sensitivity caused by sample capacitor
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  - MCBS pixel

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## Chip Characteristics

<table>
<thead>
<tr>
<th></th>
<th>ΣΔ ADC</th>
<th>MCBS ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.8 µm 3M1P</td>
<td>0.35 µm 4M1P</td>
</tr>
<tr>
<td>Pixel Area</td>
<td>20.8 µm × 19.8 µm</td>
<td>8.9 µm × 8.9 µm</td>
</tr>
<tr>
<td>Transistors per pixel</td>
<td>4.25 (17 per four pixels)</td>
<td>4.5 (18 per four pixels)</td>
</tr>
<tr>
<td>Fill Factor</td>
<td>30%</td>
<td>25%</td>
</tr>
<tr>
<td>Array Size</td>
<td>128×128</td>
<td>320×240</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>3.3 v</td>
<td>3.3 v</td>
</tr>
</tbody>
</table>
$\Sigma \Delta$ ADC Output Waveforms

SNR = 43dB with OSR = 64, Gain FPN = 1%
**Measured MCBS ADC Transfer Function**

\[
\text{INL} = 2.3 \text{ LSB}, \quad \text{DNL} = 1.2 \text{ LSB}, \quad \text{Gain FPN} = 0.24\%, \quad \text{and Offset FPN} = 0.2\%
\]
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## Pixel Level ADC Comparison

<table>
<thead>
<tr>
<th>Feature</th>
<th>ΣΔ ADC</th>
<th>MCBS ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size</td>
<td>4.25 transistors per pixel</td>
<td>4.5 transistor per pixel</td>
</tr>
<tr>
<td>Conversion mode</td>
<td>Charge to bits</td>
<td>Voltage to bits</td>
</tr>
<tr>
<td>Charge handling Capacity</td>
<td>Large</td>
<td>Small</td>
</tr>
<tr>
<td>FPN</td>
<td>Moderate</td>
<td>Small</td>
</tr>
<tr>
<td>Transistor noise sensitivity</td>
<td>Small</td>
<td>Moderate</td>
</tr>
<tr>
<td>Date rate</td>
<td>Large</td>
<td>Small</td>
</tr>
<tr>
<td>Quantization</td>
<td>Nonuniform – fixed by $L$</td>
<td>Programmable</td>
</tr>
<tr>
<td>External processing</td>
<td>Decimation Filtering</td>
<td>None</td>
</tr>
<tr>
<td>Required memory</td>
<td>Large</td>
<td>Small</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>Moderate</td>
<td>Small</td>
</tr>
</tbody>
</table>
Conclusions

• Σ∆ ADC is better suited to IR sensors
  – Large charge handling capacity
  – Fine quantization near the center of the range
    (i.e. small difference between large charge value can be determined)

• MCBS ADC is better suited to visible range sensors
  – Low output data rate
  – Programmable quantization
  – High sensitivity