

22.4 A 256×256 CMOS Image Sensor with $\Delta\Sigma$ -Based Single-Shot Compressed Sensing

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Low power consumption is a primary concern in many CMOS image-sensor applications. As the resolution of these sensors has increased while maintaining or increasing their frame rates, A/D conversion has become the dominant component of power consumption [1]. Conventional image compression can help reduce the readout rate [2] (and hence its power consumption), but cannot reduce the A/D conversion power consumption, since it is performed after all pixel values have been converted to the digital domain.

Compressed sensing (CS), e.g., see [3], promises to reduce the ADC sampling rate without adversely affecting signal recoverability. The basic premise is that if a signal can be efficiently represented using only a few coefficients in some transform domain, then it can be recovered using a much smaller number of random linear measurements than the number of samples dictated by the Nyquist rate. Several implementations of CS in image sensors have been proposed [4,5]. In [4], CS is implemented in the optical domain using a single pixel and a digital micromirror array. However, this implementation suffers from limited resolution and large camera size. In [5], CS is implemented on-chip at the analog-processing level. This implementation allows for small camera size, but the current-summing operations result in high readout noise. These CS implementations are also not well suited for video applications (where CS can help the most) because the measurements are performed sequentially, i.e., using multiple shots.

In this paper, we describe a CMOS image sensor in which CS is performed at the A/D conversion level. Our architecture addresses the limitations of previous CS implementations, allowing for single-shot imaging and high S/N readout with negligible power and area overhead. The number of CS samples, and hence the number of A/D conversions and readout rate, can be reduced by a programmable compression ratio (CR) of 1/4, 1/8, or 1/16. The sensor frame rate can be proportionally boosted to 480, 960 and 1920fps with power consumption close to that of the standard frame rate of 120fps.

Figure 22.4.1 depicts the architecture of the CMOS image sensor. It comprises a 256×256 pixel array with row block/pixel selectors, column block selectors, compressed-sensing multiplexers (CS-MUX) controlled by a pseudo-random pattern generator (LFBSRs), column-parallel $\Delta\Sigma$ ADCs with decimation filters, and a column output scanner. Since implementing CS across the entire array would be very costly in terms of die area and image reconstruction time, the pixel array is segmented into 16×16 pixel blocks and CS is performed over each block using the same M×256 random binary CS matrix Φ_{BLK} (defined by the 16b one-hot code Θ and the 64b bit stream Φ_B), where M=64, 32, or 16 is the number of random linear samples per block depending on the selected CR. Alternatively, conventional sensor operation can be performed by bypassing the CS-MUXs and directly reading out the pixel array values. The pixel comprises a pinned photodiode and 4 transistors. The transfer and reset gates in each pixel are controlled by TRG_{kl} and RST_{kl}, respectively, in a per-block fashion, while the select gate is controlled by SEL_l in a per-row-fashion.

Chip readout operation is described with the help of Figs. 22.4.2 and 22.4.3 for CR=1/4 and an example block CS matrix Φ_{BLK} . As shown in the top 3 waveforms of Fig. 22.4.2, readout is performed simultaneously for each 4-block group (k,b), (k,b+4), (k,b+8), (k,b+12) within block row k=0,...,15 for b=0,1,2,3. During this readout, M=64 consecutive ADCs are dedicated to each of the four blocks. Digital correlated double sampling is performed by first obtaining random linear samples of the pixel reset values according to Φ_{BLK} and then obtaining the corresponding random linear samples of the pixel signal values. The operation in each phase is performed one pixel row at a time (see bottom parts of Figs. 22.4.2 and 22.4.3). For each row i=0,...,15, and simultaneously for the 4-block group, 8 out of the 16 pixel values are sequentially selected by each column selector. This selection is performed using a different shift of the 16b one-hot

code Θ to control each of the four column selectors. The purpose of this selection step is to reduce the oversampling ratio and the load on each pixel column output. The selected pixel value at the output of each column selector is then either applied to each of 4 ADC inputs AD_l or not via a signal selector controlled by the stream Φ_B (a reference voltage V_g is applied to AD_l when a pixel value is not selected). The same procedure is repeated for each row of pixels within the selected 4-block group until all random linear samples from these blocks are read out. The entire readout process is then repeated for the other 4-block groups within the block row. The next block row is then read out in the same fashion and the process is repeated until all 64×256 linear samples of the current frame are obtained. Image reconstruction is performed off chip. The segmentation of the CS-MUXs can be programmed to implement other compression ratios. For example, to achieve CR=1/8, eight blocks are chosen at a time and 32 ADCs are dedicated to each block.

The ADC is composed of a 1st-order algorithmic $\Delta\Sigma$ modulator [2] followed by a decimation filter. The $\Delta\Sigma$ modulator samples the ADI signal generated by the CS-MUX and outputs a 128b stream corresponding to a coarse quantization of the sum of the selected pixel values. The residual voltage of the integrator is then fed back to the input for an additional 32b stream. The decimation filter is implemented using 8b and 6b up/down ripple counters with digital CDS capability.

Figure 22.4.4 shows a sample image taken at CR=1/4. A 256×256 image is reconstructed from 64×256 CS samples using a block-based recovery algorithm involving 2-step iterative curvelet thresholding [6]. The figure also shows three close-ups that compare the captured image at CR=1/4, the image captured with no compressed sensing, and an image captured by conventional downsampling at the same 1/4 ratio. Note that the image with compressed sensing offers a more detailed texture than the downsampled image and is very close to the image with no compression, which is captured at 1/4th the frame rate of the compressed-sensing image.

Figure 22.4.5 compares the energy consumption per frame, SSIM (Structural Similarity), and PSNR for images captured with different compression ratios to the normal capture image. Note that the reduction in energy consumption per frame is almost the same as the compression ratio, with only 3.4% increase in overall power consumption using CR=1/16 relative to normal capture. Also, note that both SSIM and PSNR drop only marginally with the compression ratio.

Figures 22.4.6 and 22.4.7 show the main chip characteristics and the chip microphotograph, respectively. The image sensor is fabricated in a 1P6M 0.15 μ m CMOS process with MIM capacitors and pinned photodiodes in a 2.9×3.5mm² die. The pixel pitch is 5.5 μ m and the column ADC pitch is 11 μ m. The column readout circuits are split between the top and the bottom of the array to allow for a wider ADC pitch. The measured readout noise is 368 μ V_{rms} in the normal mode of 120fps with a conversion gain of 20 μ V/e⁻ and the saturation level is 25,000e⁻. In CS mode with CR=1/4, the readout noise is 351 μ V_{rms}. The measured 12b differential nonlinearity is within -0.76 to +1.80 LSB.

References:

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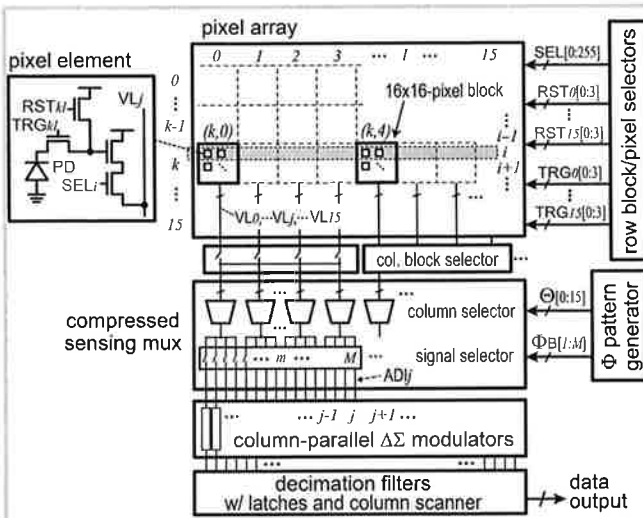


Figure 22.4.1: Image sensor architecture configured for compression ratio of 1/4.

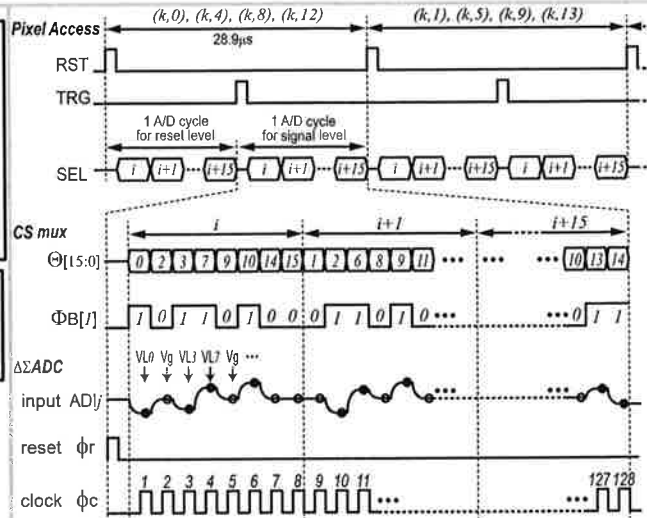


Figure 22.4.2: Readout timing diagram for row block k at compression ratio of 1/4.

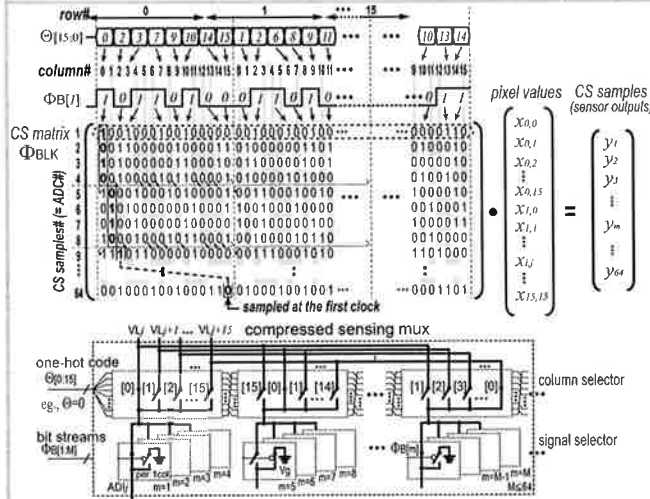


Figure 22.4.3: Example Φ BLK matrix (CR=1/4) and CS-MUX schematics configured for readout of random linear sample.

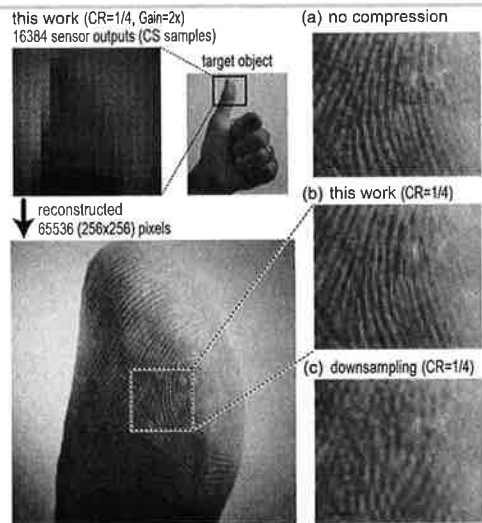


Figure 22.4.4: Captured images.

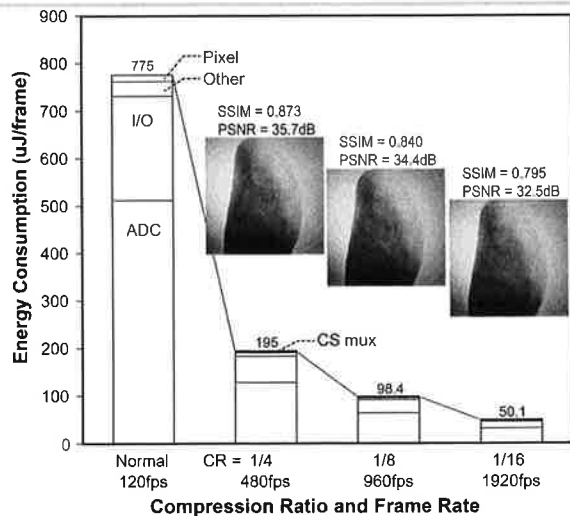


Figure 22.4.5: Energy consumption per frame, SSIM and PSNR vs. compression ratio.

Parameter	Value
Technology	0.15 μ m 1P6M CMOS process MIM cap, pinned photodiode (no color filter, no on-chip lens)
Chip Size	2.9 mm (H) x 3.5 mm (V)
Power Supplies	3.3 V / 2.0 V / 1.8 V
Num. of Effective Pixels	256 (H) x 256 (V)
Pixel Size	5.5 μ m x 5.5 μ m
Pixel Type	4T + Pinned Photodiode
Conversion Gain	20 μ V/e ⁻
Saturation Level	25,000 e ⁻
Read Noise	368 μ Vrms, 1.52 LSBrms (normal mode) 351 μ Vrms, 1.45 LSBrms (CS mode, 25%)
Frame Rate	120 fps (no compression) 480, 960, 1920 fps (w/ 1/4, 1/8, 1/16 compression)
Power Consumption	93.1 mW / 96.2 mW at 120fps / 1920fps
A/D Resolution	12 bit, 242 μ V/LSB
DNL	-0.76/+1.80 LSB
INL	< \pm 0.6%
Column FPN	0.57 LSBrms at dark level

Figure 22.4.6: Chip characteristics.

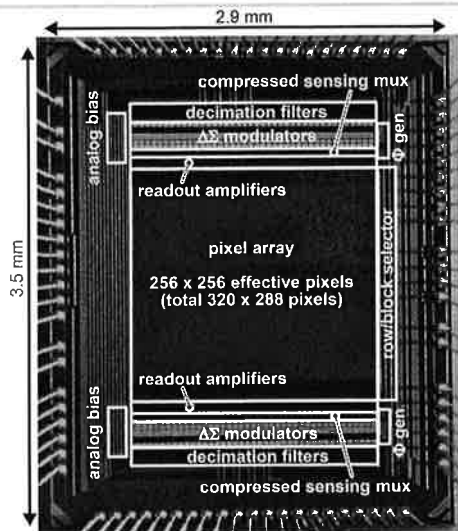


Figure 22.4.7: Chip microphotograph of the prototype image sensor.