CMOS IMAGE SENSORS DYNAMIC RANGE AND SNR ENHANCEMENT VIA STATISTICAL SIGNAL PROCESSING

A DISSERTATION

SUBMITTED TO THE DEPARTMENT OF ELECTRICAL ENGINEERING

AND THE COMMITTEE ON GRADUATE STUDIES

OF STANFORD UNIVERSITY

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

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June 2002

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Abstract

Most of today's video and digital cameras use CCD image sensors, where the electric charge collected by the photodetector array during exposure time is serially shifted out of the sensor chip resulting in slow readout speed and high power consumption. Recently developed CMOS image sensors, by comparison, are read out non-destructively and in a manner similar to a digital memory and can thus be operated at very high frame rates. A CMOS image sensor can also be integrated with other camera functions on the same chip ultimately leading to a single-chip digital camera with very compact size, low power consumption and additional functionality. CMOS image sensors, however, generally suffer from lower dynamic range than CCDs due to their high read noise and non-uniformity. Moreover, as sensor design follows CMOS technology scaling, well capacity will continue to decrease, eventually resulting in unacceptably low SNR.

In this dissertation, new pixel architectures and algorithms are presented that enhance the dynamic range and SNR of CMOS image sensors by utilizing their high speed readout and integration advantages. The thesis is divided into three parts. First, a 352×288 Digital Pixel Sensor (DPS) chip with per-pixel single-slope ADC and dynamic memory fabricated in a standard digital 0.18μm CMOS process is presented that demonstrates the high speed potential and scaling advantage of CMOS image sensors. The chip performs "snap-shot" image acquisition at continuous rate of $10,000$ frames/s or 1 Gpixels/s. Second, an algorithm based on statistical signal processing techniques is presented that synthesizes a high dynamic range, motion blur free, still image or video sequence from multiple image captures. The algorithm

is recursive and consists of two main procedures – photocurrent estimation and motion/saturation detection. Photocurrent estimation is used to reduce read noise and thus to enhance dynamic range at the low illumination end. Saturation detection is used to enhance dynamic range at the high illumination end, while motion blur detection ensures that the estimation is not corrupted by motion. Motion blur detection also makes it possible to extend exposure time and to capture more images, which can be used to further enhance dynamic range at the low illumination end. The algorithm operates completely locally and recursively, its modest computation and storage requirements make the algorithm well suited for single chip digital camera implementation. Finally, to solve the problem with CMOS technology scaling and further enhance sensor SNR at high illumination, a self-resetting scheme is presented. In this scheme, each pixel resets itself one or more times during exposure time as a function of its illumination level, resulting in higher effective well capacity and thus higher SNR. The photocurrent estimation algorithm is then extended to take new noise components into consideration, and simulations results demonstrate significant dynamic range and SNR improvements.

Acknowledgments

I am deeply indebted to many people who made my Stanford years an enlightening, rewarding and memorable experience.

First and foremost, I would like to thank professor Abbas El Gamal for having accepted me into his research group. His continuing support and invaluable guidance were an inspiration during my Ph.D studies at Stanford. I have benefited from his vast technical expertise and insight, as well as his high standards in research and publication.

I am grateful to my associate advisor professor Mark Horowitz, for his support in this research, serving on my orals committee and reading my dissertation. I am also grateful to professor Brian Wandell for his support and help throughout this PDC program. It was a great pleasure working with him.

I want to thank professor Gordon Kino. It is a great honor to have him as my oral chair. I also want to thank professor Yoshihisa Yamamoto, professor John Gill, professor Leonard Tyler, professor Joseph Goodman, and professor Peter Glynn for their help and guidance.

I gratefully appreciate the support and encouragement from Dr. Boyd Fowler, Dr. David Yang, Dr. Michael Godfrey and Dr. Hao Min. Boyd deserves special recognition.

I gratefully acknowledge Dr. Hui Tian, Dr. Stuart Kleinfelder, Sukhwan Lim, Ting Chen, Khaled Salama, Helmy Eltoukhy and Ali Ercan for their collaboration and working as officemates, along with Hossein Kakavand, Sam Kavusi and Sina Zahedi. They made our office an enjoyable environment to be working in. I would

also like to thank all the people in the PDC program for their cooperation, and all my friends for their encouragements and generous help.

I thank all the administrative associates in ISL for their kind assistance and cheerful spirit.

The programmable digital camera project is sponsored by Canon, Kodak, Hewlett-Packard, Agilent and Interval Research. I would like to thank all the companies for their support.

I am deeply indebted to our families. Without their love, I could not have reached today. Especially, I would like to thank my wife, Min, for her unconditional support and encouragement. This thesis is dedicated to her.

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Chapter 1

Introduction

Digital cameras comprise a system of components that must work together and provide a high quality result. Figure 1.1 shows the block diagram of the components in a typical digital camera system. After passing through the lens and the color filter array (CFA), light is converted into electrical signal in the image sensor. The signal is amplified by the automatic gain control (AGC) and then converted into digital signal. Finally, the digital signal is processed and compressed before it stored as a digital image. The continued scaling of CMOS technology, together with the progress in the design of mixed-signal CMOS circuits, has enabled the integration of AGC, analog to digital converter (ADC), color processing and image compression functions into a single chip. To integrate the image sensor on the same chip with the rest circuits, however, a number of issues are yet to be solved.

The image sensor plays a pivotal role in the final image quality. Most of today's video and digital cameras use Charge-Coupled Devices (CCD). In these sensors, the electric charge collected by the photodetector array during exposure time is serially shifted out of the sensor chip, thus resulting in slow readout speed and high power consumption. CCD is fabricated using specialized process with optimized photodetectors, it has very low noise and good uniformity. Since this process is incompatible with the standard CMOS process, the CCD sensor can not be integrated on the same

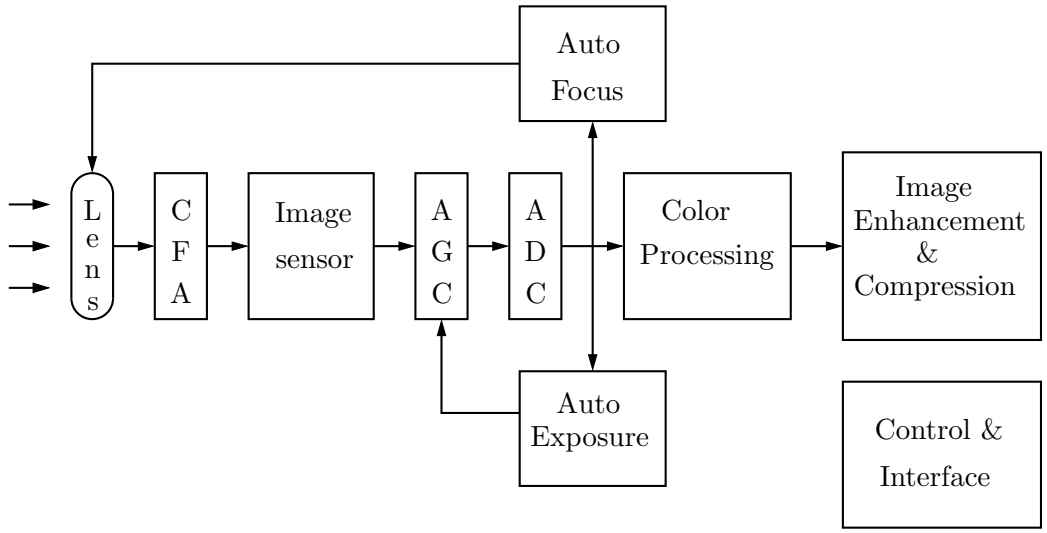


Figure 1.1: A typical digital camera system.

CMOS chip with the rest circuitry.

Recently developed CMOS image sensors, by comparison, are read out non-destructively and in a manner similar to a digital memory and can thus be operated at very high frame rates. The CMOS image sensor can be integrated on the same chip, ultimately leading to a single-chip digital camera with very compact size, low power consumption and additional functionality. These appealing advantages of CMOS image sensors further expand their applications beyond traditional digital cameras, into fields such as PC cameras, mobile phones, PDAs, and automobiles. However, due to their high read noise and high fixed pattern noise (FPN), CMOS image sensors generally suffer from lower signal to noise ratio (SNR) and dynamic range than CCDs. Enhancing the SNR and dynamic range of CMOS image sensor, therefore, is a common goal that industry and research community are striving for.

This chapter first presents a review on the characteristics of solid state image sensors and the architectures of an interline CCD sensor and three CMOS image sensors — Passive Pixel Sensor (PPS), Active Pixel Sensor (APS), and Digital Pixel Sensor (DPS). The dominating factors in limiting sensor SNR and dynamic range are then discussed. Finally, previous work on image sensor dynamic range enhancement

is presented.

1.1 Solid State Image Sensors

The image capturing devices in digital cameras are all solid state area image sensors. An area image sensor array consists of $n \times m$ pixels, ranging from 320×240 (QVGA) to 7000×9000 (very high end astronomy sensor). Each pixel contains a photodetector and devices for readout. The pixel size ranges from $15\mu\text{m} \times 15\mu\text{m}$ down to $3\mu\text{m} \times 3\mu\text{m}$, where the minimum pixel size is limited by dynamic range and cost of optics. Pixel fill factor is the fraction of pixel area occupied by the photodetector, which ranges from 0.2 to 0.9. High fill factor is always desirable.

The photodetector [1] converts incident radiant power (photons/sec) into photocurrent that is proportional to the radiant power. There are several types of photodetectors, the most commonly used are the photodiode, which is a reverse biased pn junction, and the photogate, which is an MOS capacitor. Figure 1.2 shows the photocurrent generation in a reverse biased photodiode [3]. The photocurrent, i_{ph}, is the sum of three components: i) current due to generation in depletion (space charge) region, i_{ph}^{sc} — almost all carriers generated are swept away by strong electric field; ii) current due to holes generated in n-type quasi-neutral region, i_{ph}^{p}— some diffuse to space charge region and get collected; iii) current due to electrons generated in p-type region, i_{ph}^{n}. Therefore, the total photo-generated current is:

$$i_{ph} = i_{ph}^{sc} + i_{ph}^{p} + i_{ph}^{n}. \tag{1.1}$$

The detector spectral response $\eta(\lambda)$ is the fraction of photon flux that contributes to photocurrent as a function of the light wavelength λ, and the quantum efficiency (QE) is the maximum spectral response over λ.

The photodetector dark current i_{dc} is the detector leakage current, *i.e.*, current not induced by photogeneration. It is called dark current since it corresponds to the photocurrent under no illumination. Dark current is caused by the defects in silicon,

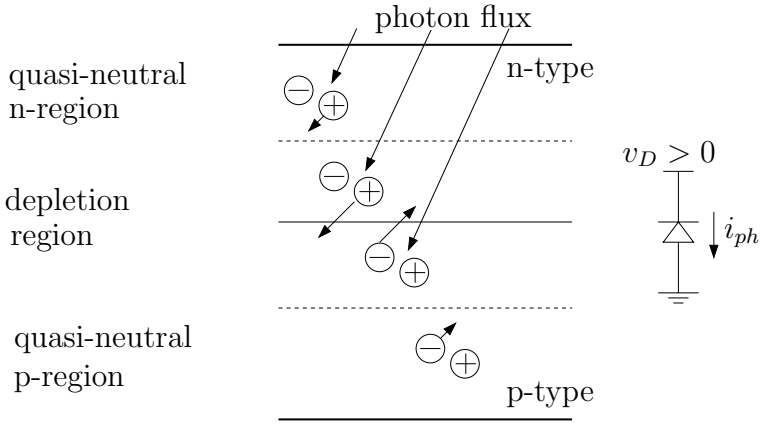


Figure 1.2: Photocurrent generation in a reverse biased photodiode

which include bulk defects, interface defects and surface defects. Dark current limits the photodetector dynamic range because it reduces the signal swing and introduces shot noise.

Since the photocurrent is very small, normally on the order of tens to hundreds of fA (10^{-15} Amp), it is integrated into charge and the accumulated charge (or converted voltage) is read out. This type of operation is called direct integration, the most commonly used mode of operation in an image sensor. In this operation, the photodiode is reset to the reverse bias voltage at the start of the image capture exposure time, or integration time. The diode current is integrated on the diode parasitic capacitance during integration time and the accumulated charge or voltage is read out at end.

1.1.1 CCD Image Sensors

CCD image sensors [2] are the most widely used solid state image sensors in today's digital cameras. The primary difference between CCD and CMOS image sensors is the readout architecture. For CCDs, the integrated charge is shifted out using capacitors.

Figure 1.3 depicts the block diagram of the widely used interline transfer CCD image sensors. It consists of array of photodetectors and vertical and horizontal CCDs

for readout. During exposure, the charge is integrated in each photodetector, and it is simultaneously transferred to vertical CCDs at the end of exposure for all the pixels. The charge is then sequentially readout through the vertical and horizontal CCDs by charge transfer.

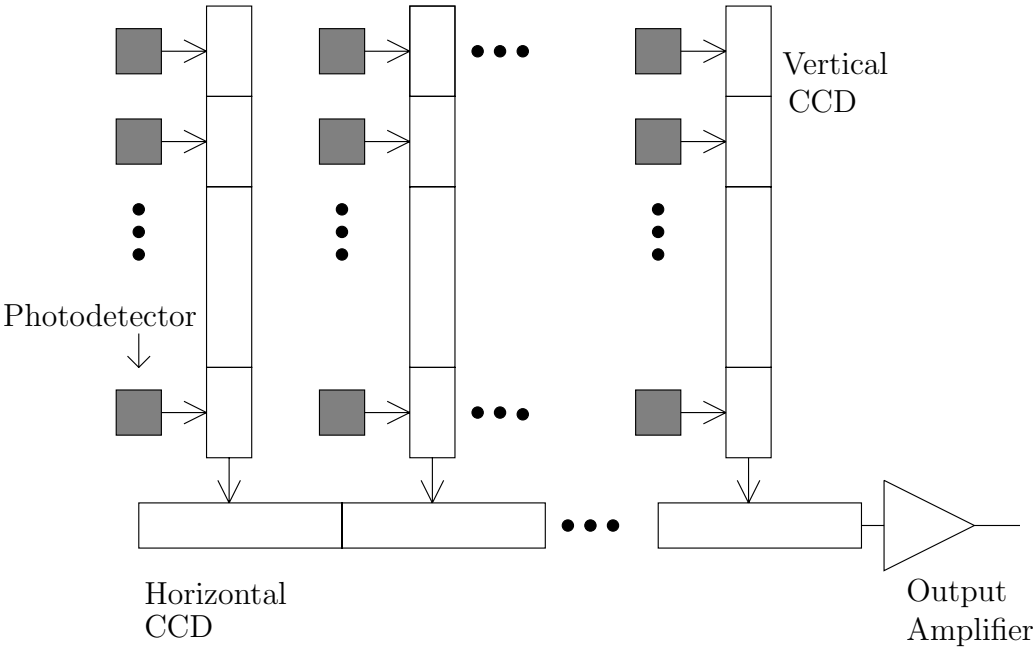


Figure 1.3: Block diagram of a typical interline transfer CCD image sensors.

A CCD is a dynamic charge shift register implemented using closely spaced MOS capacitors clocked at different phases as shown in Figure 1.4. The capacitors operate in deep depletion regime when clock is high. Charge is transferred from one capacitor whose clock is switching from high to low, to the next capacitor whose clock is switching from low to high at the same time. During this transfer process, most of the charge is transferred very quickly by repulsive force among electrons, which creates self-induced lateral drift, the remaining charge is transferred slowly by thermal diffusion and fringing field.

The charge transfer efficiency describes the fraction of signal charge transferred from one CCD stage to the next. It must be made very high (≈ 1) since in a CCD image sensor charge is transferred up to $n+m$ CCD stages for a $m \times n$ pixel sensor. The

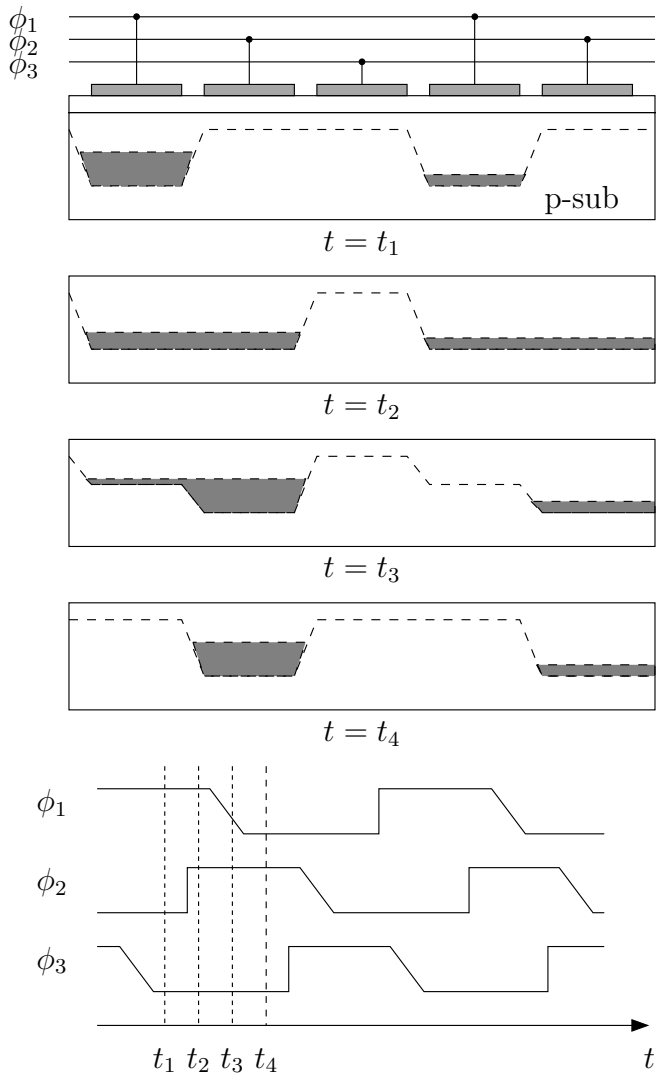


Figure 1.4: Potential wells and timing diagram during the transfer of charge in a three-phase CCD

charge transfer must occur at high enough rate to avoid corruption by leakage, but slow enough to ensure high charge transfer efficiency. Therefore, CCD image sensor readout speed is limited mainly by the array size and the charge transfer efficiency requirement. As an example, the maximum video frame rate for an 1024×1024 interline transfer CCD image sensor is less than 25 frames/s given a 0.99997 transfer efficiency requirement and 4μm center to center capacitor spacing.

The biggest advantage of CCD is its high quality. It is fabricated using specialized process [2] with optimized photodetectors, very low noise, and very good uniformity. The photodetectors have high QE and low dark current. No noise is introduced during charge transfer. The disadvantages of CCD include: i) it can not be integrated with other analog or digital circuits such as clock generation, control and A/D conversion; ii) it is highly non-programmable; iii) it has very high power consumption because the entire array is switching at high speed all the time; iv) it has limited frame rate, especially for large sensors due to required increase in transfer speed while maintaining acceptable transfer efficiency.

Note that CCD readout is destructive, the pixel charge signal can only be readout once. The act of reading discharges the capacitor, eliminates the data.

1.1.2 CMOS Image Sensors

CMOS image sensors [18]-[22] are fabricated using standard CMOS process with no or minor modification. The pixels in the array are addressed through the horizontal word line and the charge or voltage signal is readout from each pixel through the vertical bit line. The readout is done by transferring one row at a time to the column storage capacitors, then reading out the row using the column decoder and multiplexer. This readout method is similar to a memory structure. Figure 1.5 shows a CMOS image sensor architecture. There are three pixel architectures: Passive pixel (PPS), Active pixel (APS) and Digital pixel (DPS).

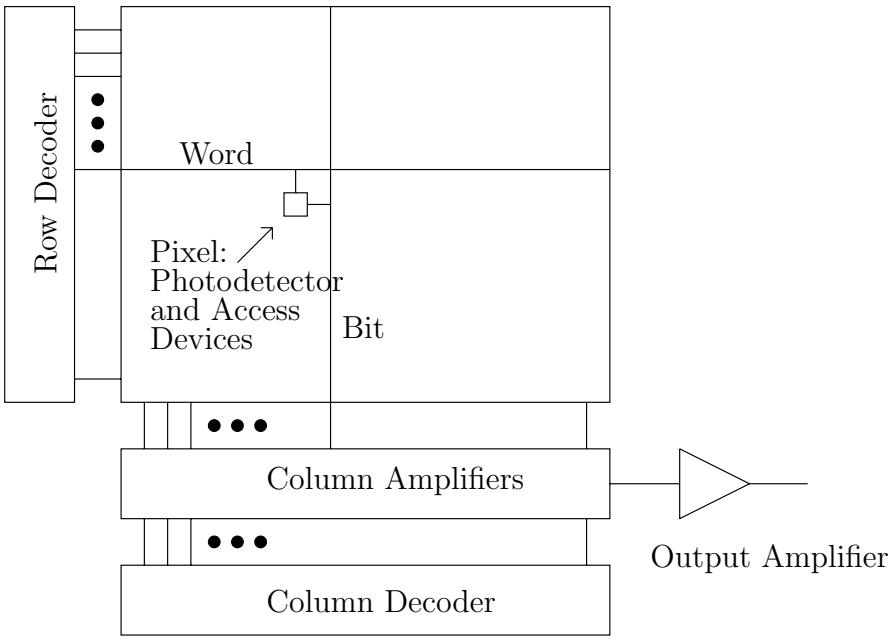


Figure 1.5: Block diagram of a CMOS image sensors.

Passive and Active Pixel Sensors

PPS [23]-[29] has only one transistor per pixel, as shown in Figure 1.6. The charge signal in each pixel is read out via a column charge amplifier, and this readout is destructive as in the case of CCD. PPS has small pixel size and large fill factor, but it suffers from slow readout speed and low SNR. PPS readout time is limited by the time of transferring a row to the output of the charge amplifiers.

APS [30]-[45] normally has three or four transistors per pixel where one transistor works as buffer and amplifier. As shown in Figure 1.7, the output of the photodiode is buffered using pixel level follower amplifier, therefore, output signal is in voltage and the reading is not destructive. In comparison to PPS, APS has larger pixel size and lower fill factor, but its readout is faster and has higher SNR.

Figure 1.8 shows a CMOS photogate APS pixel. The photogate PG is biased in deep depletion during integration and the photon induced charge is accumulated underneath the gate. Then during reading, the photogate voltage is lowered to 0V and the charge is transferred to the floating node D, which is reset to a certain

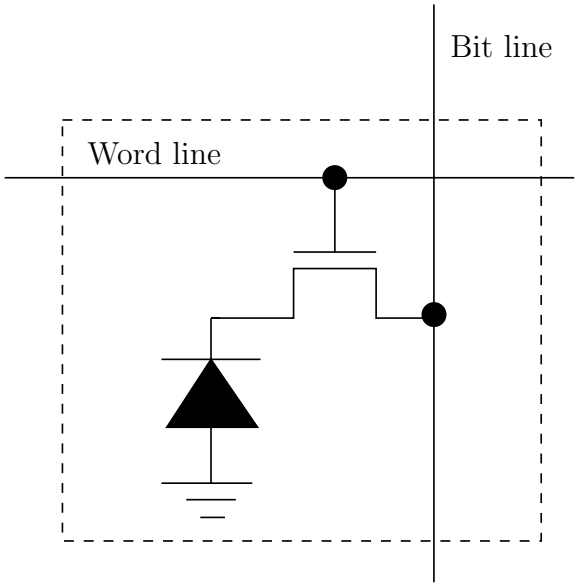


Figure 1.6: Passive pixel sensor (PPS)

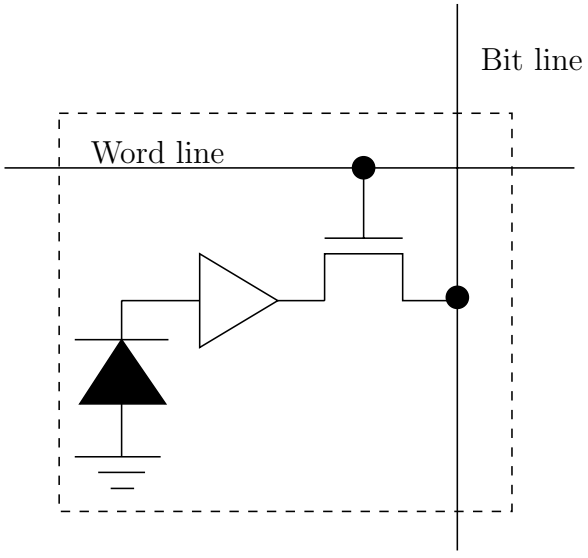


Figure 1.7: Active Pixel Sensor (APS)

voltage prior to the charge transfer. The transfer gate TX can be either switched from low to high or kept at a constant intermediate voltage during the charge transfer. The output signal from the pixel is still in voltage that is converted by the floating node capacitance. The column and chip circuits of photogate APS are identical to photodiode APS.

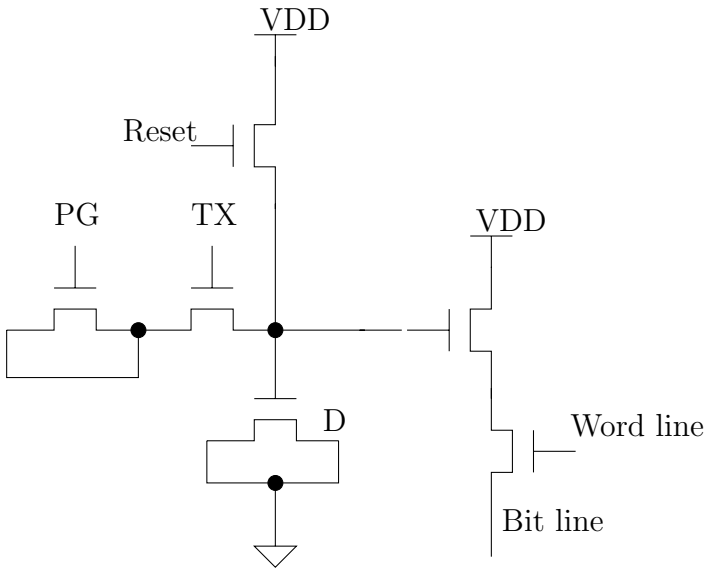


Figure 1.8: Photogate APS

CMOS Digital Pixel Sensors

In a Digital Pixel Sensor (DPS) [52]-[60], each pixel has an ADC, all ADCs operate in parallel, and digital data stored in the memory is directly read out of the image sensor array as in a conventional digital memory (see Figure 1.9). The DPS architecture offers several advantages over analog image sensors, such as Active Pixel Sensors (APS). These include better scaling with CMOS technology due to reduced analog circuit performance demands and the elimination of read related column fixed-pattern noise (FPN) and column readout noise. With an ADC and memory per pixel, massively parallel "snap-shot" imaging, A/D conversion and high speed digital readout become practical, eliminating analog A/D conversion and readout bottlenecks. This

benefits traditional high speed imaging applications (*e.g.*, [100, 101]) and enables efficient implementations of several still and standard video rate applications such as sensor dynamic range enhancement and motion estimation [65, 67, 66, 68].

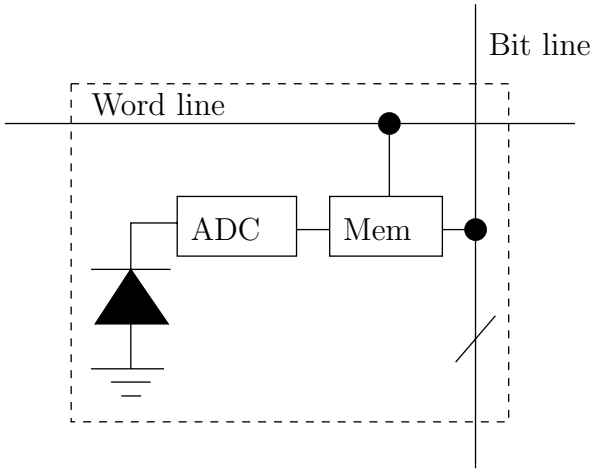


Figure 1.9: Digital Pixel Sensor (DPS)

The main drawback of DPS is its large pixel size due to the increased number of transistors per pixel. Since there is a lower bound on practical pixel sizes imposed by the wavelength of light, imaging optics, and dynamic range considerations, this problem diminishes as CMOS technology scales down to 0.18μm and below. Designing image sensors in such advanced technologies, however, is challenging due to supply voltage scaling and the increase in leakage currents [19].

Note that only DPS is capable of performing high-speed, non-destructive, "snap-shot" image capture. CCD and PPS readout is destructive; APS can not perform real "snap-shot" capture due to the different integration time for each row during exposure.

1.2 SNR and Dynamic Range Enhancement

SNR and dynamic range are important figures of merit for image sensors. Dynamic range quantifies the sensor's ability to adequately image both high lights and dark shadows in a scene. CMOS image sensors generally suffer from high read noise and non-uniformity, resulting in lower SNR and dynamic range than CCDs. In this section, after quantifying sensor SNR and dynamic range and discussing their dependencies on key sensor parameters, we will review previous works on image sensor dynamic range enhancement.

1.2.1 SNR and Dynamic Range

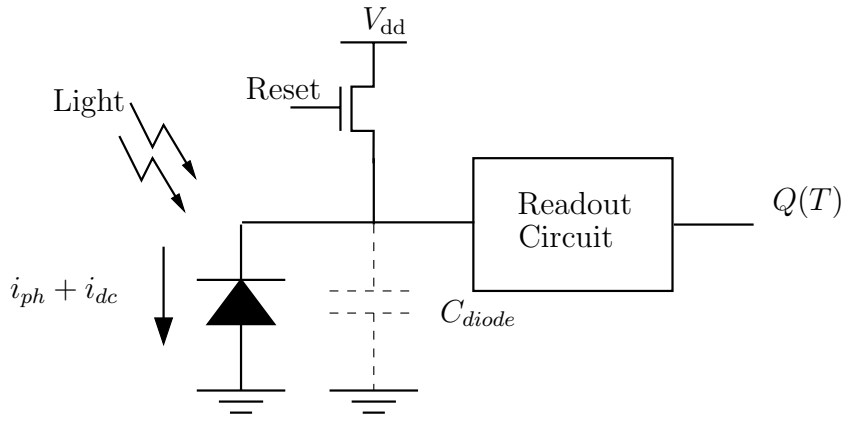


Figure 1.10: CMOS image sensor pixel model.

Figure 1.10 shows a typical CMOS image sensor pixel operating in direct integration. The photodiode is reset before the beginning of capture. During exposure, the photocurrent is integrated onto the photodiode parasitic capacitor C_{diode} and the charge $Q(T)$ (or voltage) is read out at the end of exposure time T. Dark current i_{dc} and additive noise are also integrated with the photocharge. The noise can be expressed as the sum of three independent components:

- Shot noise $U(T)$, which is generated when current passes through the diode

junction, can be approximated by a Gaussian $U(T) \sim \mathcal{N}(0, q\int_0^T (i_{ph}(t) + i_{dc})dt)$ when photocurrent is large enough. Here q is the electron charge.

- Reset noise (including offset fixed pattern noise (FPN)), which is generated during reset, also has a Gaussian distribution, $C \sim \mathcal{N}(0, \sigma_C^2)$.
- Readout circuit noise $V(T)$ (including quantization noise) with zero mean and variance σ_V^2.

Therefore the output charge from a pixel can be expressed as

$$Q(T) = \int_0^T (i_{ph}(t) + i_{dc})dt + U(T) + V(T) + C, \tag{1.2}$$

provided $Q(T) \leq Q_{sat}$, the saturation charge, also referred to as *well capacity*.

If photocurrent is constant over exposure time, signal-to-noise ratio (SNR) is given by

$$\text{SNR}(i_{ph}) = 20\log_{10}\frac{i_{ph}T}{\sqrt{q(i_{ph} + i_{dc})T + \sigma_V^2 + \sigma_C^2}}. \tag{1.3}$$

Equation 1.3 shows that SNR increases with i_{ph}, first at 20dB per decade when reset and readout noise variance dominates, and then at 10dB per decade when shot noise variance dominates. Since SNR also increases with T, it is always preferred to have the longest possible exposure time. Saturation and change in photocurrent due to motion, however, set an upper limit on exposure time.

Sensor dynamic range quantifies the ability to adequately image both high lights and dark shadows in a scene. It is defined as the ratio of the largest non-saturating photocurrent i_{max} to the smallest detectable photocurrent i_{min}, typically defined as the standard deviation of the noise under dark conditions. For a sensor with fixed well capacity Q_{sat}, saturation limits the highest signal and sensor read noise limits the lowest detectable signal. Using the sensor model, the dynamic range can be expressed as

$$\text{DR} = 20\log_{10}\frac{i_{max}}{i_{min}} = 20\log_{10}\frac{Q_{sat}}{\sqrt{qi_{dc}T + \sigma_V^2 + \sigma_C^2}}. \tag{1.4}$$

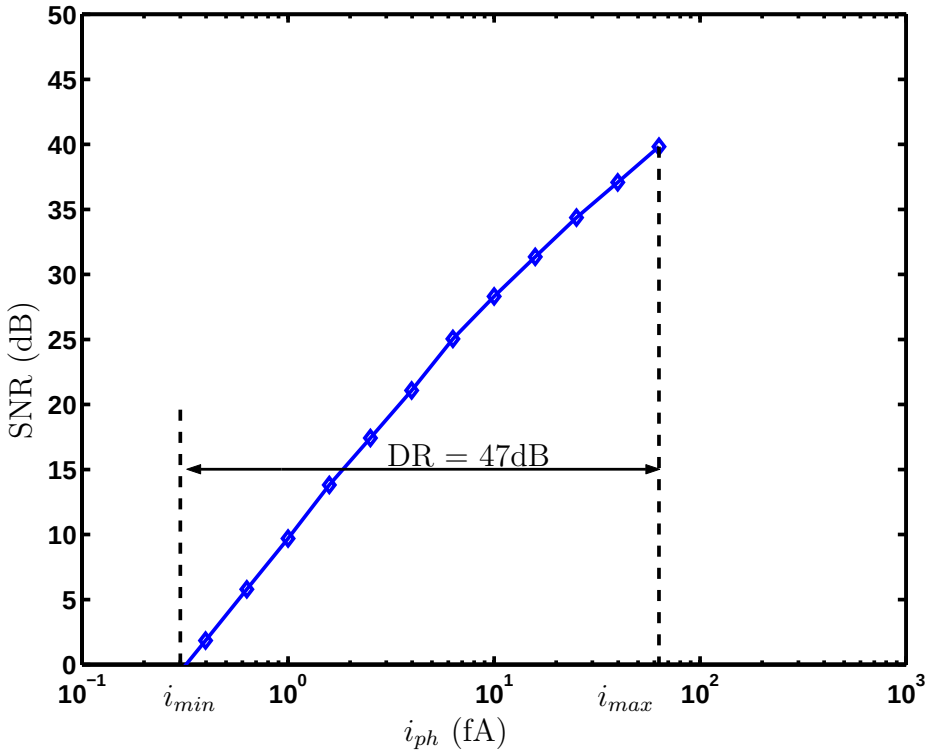


Figure 1.11: SNR and dynamic range for a typical sensor with well capacity, $Q_{well} = 18,750e^{-}$, readout noise, $\sigma_V = 60e^{-}$, reset nois, $\sigma_C = 62e^{-}$, and total integration time, $T = 32$ms.

Figure 1.11 plots the SNR and dynamic range vs. photocurrent for a typical sensor. In this specific example, given a well capacity, $Q_{well} = 18,750e^-$, readout noise, $\sigma_V = 60e^-$, reset nois, $\sigma_C = 62e^-$, and total integration time, $T = 32$ms, the sensor dynamic range is 47dB and the peak SNR is less than 40dB. This dynamic range is not high enough to capture a typical outdoor scene where both bright sun light and dark shadow exist.

1.2.2 Review of Dynamic Range Enhancement Schemes

Several techniques and architectures [71]-[95] have been proposed for extending image sensor dynamic range. Below is a review of some representative schemes.

Well capacity adjusting

In [81, 82], a well capacity adjusting scheme was proposed to enhance the sensor dynamic range. In this scheme, the well capacity is increased one or more times during integration. For APS, this is done by adjusting the reset signal one or more times during integration [83]. As a result, pixel current to charge transfer function is compressed, and the maximum non-saturating current is extended.

The increase in dynamic range, however, comes at the expense of decrease in SNR, as shown in [65]. Moreover, the smallest detectable signal does not change in this scheme, so dynamic range is only enhanced at high illumination end.

Multiple capture

In [80, 102], a multiple capture scheme was proposed to enhance the sensor dynamic range. The idea is to capture several images at different times within the normal exposure time — shorter exposure time images capture the brighter areas of the scene while longer exposure time images capture the darker areas of the scene. A high dynamic range image is then synthesized from the multiple captures by appropriately scaling each pixel's last sample before saturation.

In [65], it was shown that this scheme achieves higher SNR than well capacity adjusting scheme. However, this scheme does not take full advantage of the captured images. Since readout noise is not reduced, dynamic range is only extended at the high illumination end.

Spatially varying exposure

Another dynamic range enhancement scheme is spatially varying exposure [84, 85], which implements multiple capture using a conventional sensor by sacrificing spatial resolution. The idea is to deposit an array of neutral density filters on the sensor so that in a single capture pixels with darker filters sample high lights while pixels with lighter filters sample low lights. The high dynamic range image is synthesized using low pass filtering or more sophisticated techniques such as cubic interpolation.

This scheme is very simple to implement and requires no change to the sensor itself; however, the blocking of light due to neutral density filters reduces sensor sensitivity and SNR. Also, very high resolution sensor is needed since the spatial resolution is reduced. The dynamic range is extended at the high illumination end only, which is same as the above two schemes.

Time-to-saturation

In [86, 87, 88], a time to saturation scheme was proposed. The idea is to measure the integration time required to saturate each pixel. In this scheme, the minimum detectable current is limited by the maximum allowable integration time and the maximum detectable current is limited by circuit mismatches, readout speed and FPN.

The challenge in implementing this scheme is to find a way to detect saturation for each pixel, and then record the time — if global circuits are used, contention can severely limit performance; if the detection and recording are done at the pixel level, the pixel size may become unacceptably large. The sensor SNR is quite uniform at all signal levels, and the peak SNR is limited by the well capacity.

Logarithmic sensor

In a logarithmic sensor [89, 90, 91], the photocurrent is directly converted to voltage for readout. The sensor achieves high dynamic range via logarithmic compression during conversion to voltage via the exponential I-V characteristics of the MOS transistor in subthreshold. Up to 5-6 decades of dynamic range can be compressed into a voltage range around 0.5V depending on the transistor threshold voltage and the number of series transistors.

There are several issues associated with this scheme. First of all, transistor mismatches are significant due to the poorly defined subthreshold MOSFET characteristics as well as varying threshold voltages. Second, succeeding circuitry must be extremely precise to make use of the dynamic range afforded by the compressed output voltage. Finally, the non-integrating nature limits the achievable SNR in even high illumination due to the exponential transconductance relationship.

1.3 Organization

Previously proposed high dynamic range enhancement schemes mainly focus on extending the sensor dynamic range at high illumination end, sensor dynamic range extension at low illumination has not been addressed. For some schemes, the increase in dynamic range comes at the expense of decrease in SNR; and for others, SNR is the same since sensor readout noise is not reduced. Moreover, all the previous schemes are subject to potential motion blur, which limits the maximum exposure time and hence SNR at both low and high illumination ends.

In this dissertation, a new pixel architecture and algorithm are presented that enhance SNR and dynamic range of CMOS image sensors at both low and high illumination ends, and simultaneously eliminate motion blur. Our algorithm takes advantage of the unique high speed, multiple non-destructive operation of CMOS Digital Pixel Sensor, as we will demonstrate using a $10,000$ frames/s DPS chip in Chapter 2. The algorithm consists of two main procedures – photocurrent estimation and motion/saturation detection. Estimation is used to reduce read noise and thus to

enhance dynamic range at the low illumination end. Besides the saturation detection used to enhance dynamic range at the high illumination end, a motion blur detection algorithm is added to ensure that the estimation is not corrupted by motion. This motion blur detection further makes it possible to extend exposure time and to capture more images, which can be used to further enhance dynamic range at the low illumination end.

Finally, to solve the problem with CMOS technology scaling and further enhance sensor SNR at high illumination, a self-resetting architecture is presented. In this architecture, each pixel resets itself one or more times during exposure time as a function of the illumination level, resulting in higher effective well capacity and thus higher SNR. Further SNR and dynamic range improvement is achieved by utilizing our photocurrent estimation and saturation/motion detection algorithm by taking new noise components into consideration. As will be shown, simulation results demonstrate significant dynamic range and SNR improvements.

This dissertation is organized into six chapters of which this is the first. Chapter 2 presents a 352×288 pixel DPS test chip that demonstrates the high speed, non-destructive readout advantages of CMOS digital pixel image sensor. Chapter 3 presents three photocurrent estimation algorithms that can be used to reduce read noise and enhance dynamic range at the low illumination end. Chapter 4 presents a new method that synthesizes the high dynamic range, motion blur free image from multiple image captures, motion/saturation detection algorithms. Experimental results achieved with this algorithm are also presented. In Chapter 5, a self-reset architecture to solve the reduced well capacity problem associated with CMOS technology scaling is presented. By extending our photocurrent estimation and motion/saturation detection algorithm into this new architecture, the SNR and dynamic range of CMOS image sensor are further improved. Finally, in Chapter 6, the contributions of this research are summarized, and directions for future work are suggested.

Chapter 2

A 10,000 Frames/s Digital Pixel Sensor

Several high speed CMOS APS chips have been reported. Krymski *et. al.* [104] describe a 1024×1024 APS, followed by column-level 8-bit ADCs that achieves over 500 frames/s. Readout and digitization are performed one row at a time and each digitized row is read out over a 64-bit wide output bus. Fully pixel-parallel image acquisition ("snap shot" acquisition) and short shutter durations are important requirements in high speed imaging to prevent image distortion due to motion. These requirements, however, cannot be achieved using the standard APS architecture used in [104]. To address this limitation, Stevanovic *et. al.* [105] describe a 256×256 APS with per-pixel storage capacitor to facilitate pixel-parallel image acquisition. Analog pixel values are multiplexed and read out through 4 analog outputs, achieving over 1000 frames/s.

Moving ADC from column/chip level into pixel level not only reduces the stringent requirement of signal integrity when shifting the analog signal out from the pixel array, it also reduces the time requirement in digitizing the signals from all the pixels [52].

This is a key advantage of DPS over APS employing column-level, chip-level, or off-chip ADCs where digitization rates do not scale linearly with the number of pixels in the array. Storing the instantaneous data into the digital memory embedded in each pixel further increase the frame rate for a given I/O bandwidth since the sensor integration and readout phases can now be overlapped.

The DPS architecture (see Figure 2.1) described in this chapter fulfills the requirements of high speed imaging with practically no limit on array size. It performs fully pixel-parallel image acquisition. Pixel reset is performed in parallel for all pixels and the reset duration is completely programmable, permitting higher shutter speeds. The massively-parallel per-pixel A/D conversion scheme demonstrated here results in a high digitization rate.

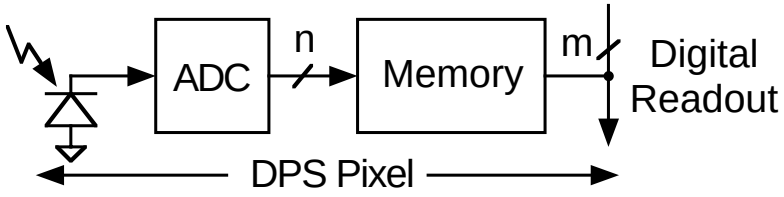


Figure 2.1: Simple DPS pixel block diagram.

In this chapter, the DPS chip architecture and main characteristics are first presented. Next, the circuit implementation of the pixel design is presented and the chip operation including the different imaging modes is discussed. Finally, in Section 2.4, experimental measurements of the chip characteristics including ADC performance, QE, dark current, noise, digital noise coupling, and sample images are presented.

2.1 DPS Chip Overview

A photomicrograph of the DPS chip is shown in Figure 2.2 and the main chip characteristics are listed in Table 2.1. The chip contains 3.8 million transistors on a 5×5mm die. The sensor array is 352×288 pixels in size, conforming to the CIF format. The

pixel is 9.4μm on each side and contains 37 transistors, including a photogate, transfer gate, reset transistor, a storage capacitor, and an 8-bit single-slope ADC with an 8-bit 3T-DRAM. The chip also contains test structures that we used for detailed characterization of APS and DPS pixels [107]. The test structures can be seen in upper center area of the chip.

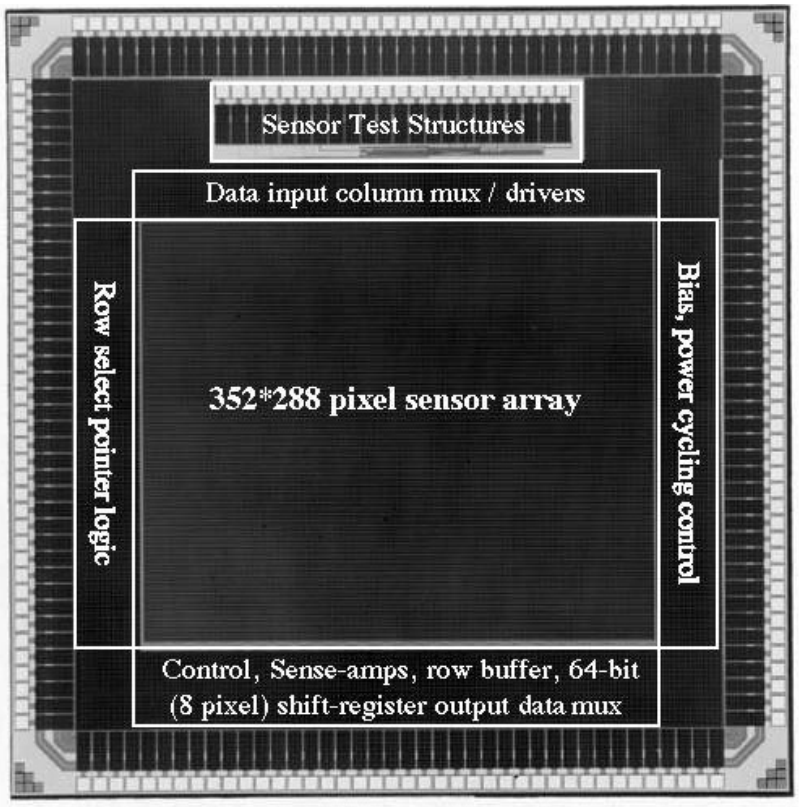


Figure 2.2: DPS Chip photomicrograph. The chip size is 5 × 5mm.

Figure 2.3 shows a block diagram of the DPS chip. At the center is the sensor array. The periphery above the sensor core contains an 8-bit gray code counter, an auxiliary code input, and multiplexers and tri-state column data drivers that are used to write data into the memory within the pixel array. The column multiplexers can be used to substitute arbitrary patterns for the standard gray code during data conversion. This facilitates the use of nonlinear ADC transfer functions, for example, for compression of dynamic range and contrast stretching. To the left of the sensor

Technology	0.18μm 5-metal CMOS
Die size	5×5 mm
Array size	352×288 pixels
Number of transistors	3.8 million
Readout architecture	64-bit (167 MHz)
Max output data rate	> 1.33 GB/s
Max continuous frame rate	$> 10,000$ frames/s
Max continuous pixel rate	> 1 Gpixels/s
Pixel size	$9.4 \times 9.4\mu$m
Photodetector type	nMOS Photogate
Number of transistors/pixel	37
Sensor fill factor	15%

Table 2.1: Chip characteristics.

array is the readout control periphery that includes a row select pointer for addressing the pixel-level memory during readout. To the right of the sensor array is the bias generation and power-down circuits, which are used to digitally control the per-pixel ADC and memory sense-amp biases. The analog ramp signal input to the array needed for the per-pixel ADCs is supplied by an off-chip DAC.

Below the sensor core is the digital readout circuits that include column sense-amps for reading the pixel-level memory and an output multiplexing shift register. The pixel values are read out of the memory one row at a time using the row select pointer and column sense-amps. Each row is then buffered and pipelined so that as one row is being shifted out of the chip the following row is read out of the memory. A 64-bit wide parallel-in, serial-out shift-register bank was used instead of a large multiplexer since in a shift register data moves in small increments, reducing local capacitance and drive circuit performance requirements. With each clock cycle, eight 8-bit pixel values are read out in a continuous stream with no waits or gaps between rows. An entirely closed-loop clocking system is used to assure clock and data integrity. The 64-bit output bus is clocked at 167 MHz for a 1.33 GB/s readout rate.

In the lower left corner of the chip is the readout control block. Since the chip is to be clocked at upwards of 167 MHz, it was important to keep off-chip high speed

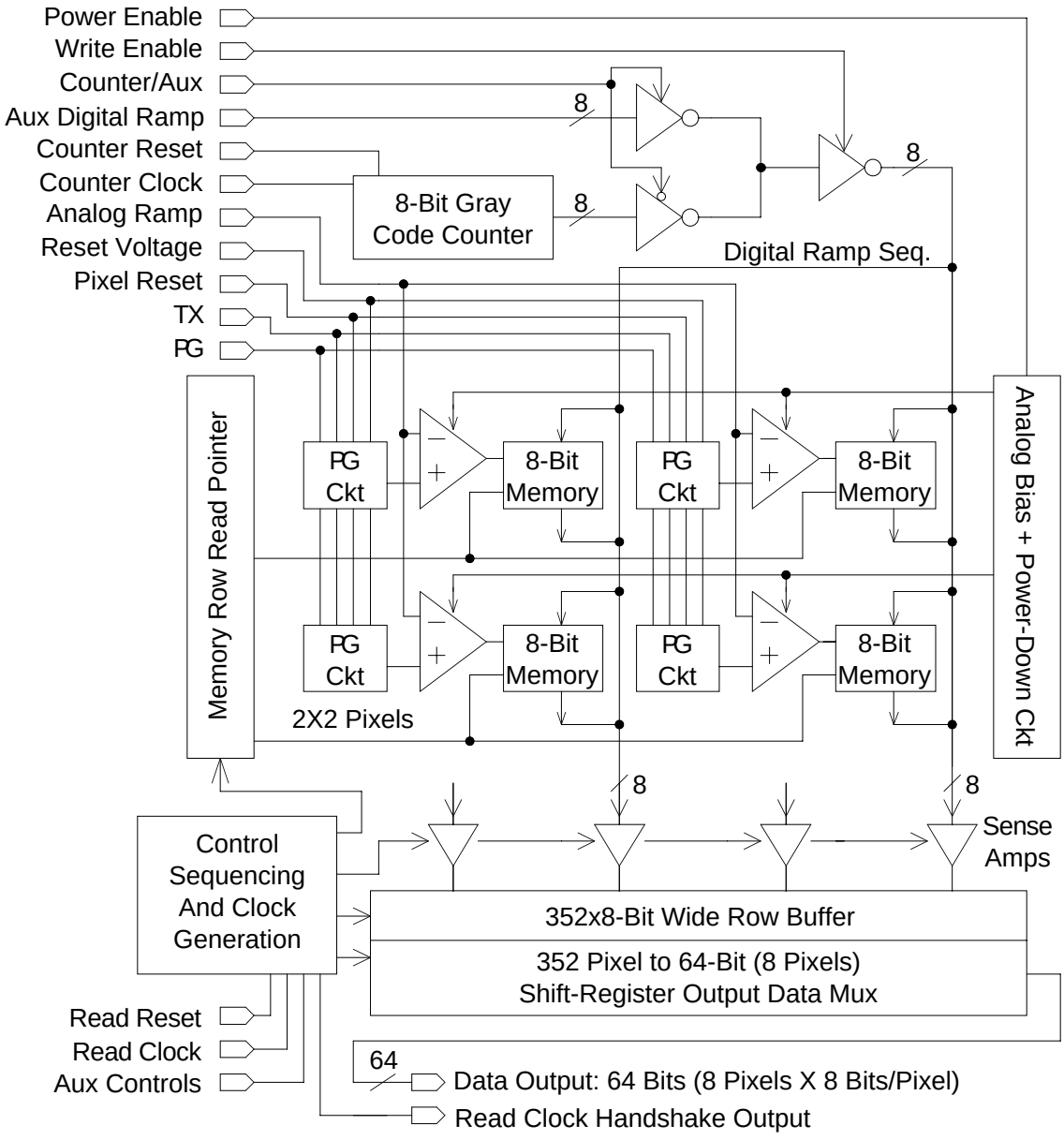


Figure 2.3: DPS block diagram.

controls to a minimum. The control block provides all the signals needed for readout from a single frame reset followed by a single continuous clock burst. A 6-phase clock generator using feedback to ensure correct margins is used to drive the shift registers. During chip testing or experimental operation, the control block can be bypassed and a set of auxiliary input controls used. Almost all digital circuitry in the periphery of the chip was designed using static logic to permit arbitrarily low clock rates.

2.2 Pixel Design

The pixel circuit is shown in Figure 2.4. It consists of a photogate circuit, a comparator and an 8-bit memory. The photogate circuit consists of an nMOS photogate, a transfer gate, a reset transistor and a sample capacitor. We decided to use a photogate to achieve high conversion gain and because preliminary process data indicated that native photodiodes have unacceptably high leakage. We implemented the photogate circuit using the standard thick oxide (3.3V) transistors that normally used in I/O circuits, to avoid the high gate and subthreshold leakage currents of the thin oxide (1.8V) transistors. Implementing the photogate and reset transistor using thick oxide transistors also makes it possible to use higher gate voltages than the nominal 1.8V supply to increase voltage swing.

The comparator consists of a differential gain stage, a single-ended gain stage, followed by a CMOS inverter. It is designed to provide gain sufficient for 10-bits of resolution with an input swing of 1V and a worst case settling time of 80ns. This provides the flexibility to perform 8-bit A/D conversion over a 0.25V range in under 25μs, which is desirable for high speed and/or low light operation. In our earlier implementation [58], the pixel-level comparator was configured as a unity feedback amplifier during reset to perform auto zeroing. Since in this implementation we needed very high gain-bandwidth product at low power consumption and small area, we chose to run the comparator open loop and sacrifice the auto zeroing capability. To cancel the high comparator offset voltages we rely on digital CDS. Due to the low operating

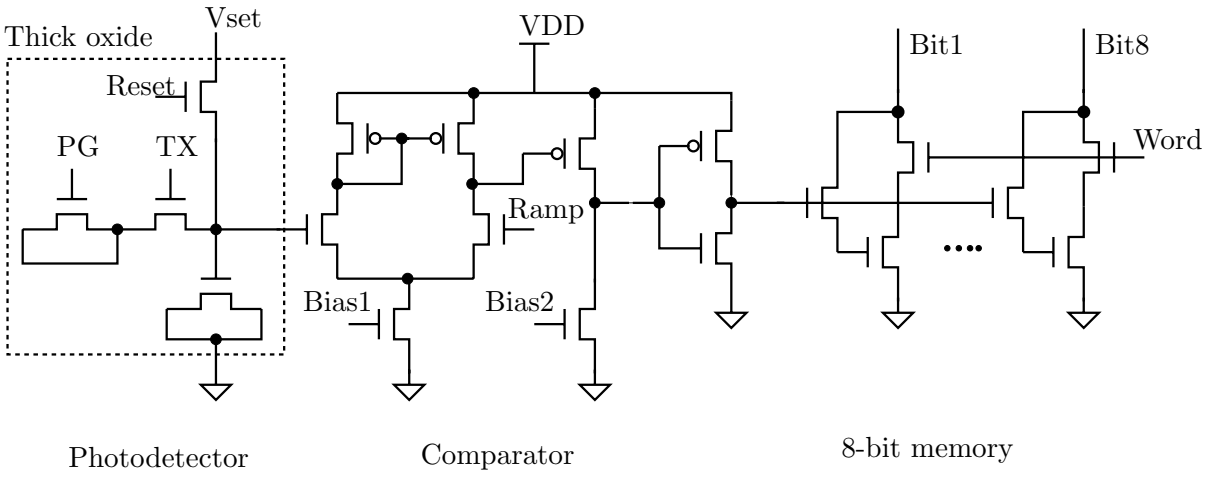


Figure 2.4: Pixel schematic.

voltage and the desire for a large input swing, we could not use a cascode architecture. Instead we used a three stage architecture, with a CMOS inverter as the third stage to saturate the output voltage levels. Figure 2.5 plots the simulated comparator gain-bandwidth product vs. input voltage at all fabrication corners (normal, fast-fast, fast-slow, slow-fast,slow-slow).

The pixel-level memory was implemented using 3T dynamic memory cells with a single read/write port to achieve small area and high speed readout. The memory was designed for a maximum data hold time of 10ms. This required the use of larger than minimum gate length access transistors and holding the bit lines at around Vdd/2 to combat high transistor off-currents. Writing into the memory is locally controlled by the comparator. During readout, single-ended charge-redistribution column sense-amps, located in the periphery and not shown in the figure, are used for robustness against the effects of capacitive coupling between the closely spaced bit lines.

The comparator and pixel-level memory circuits can be electrically tested by applying analog signals to the sense node through the V_{set} signal, performing A/D conversion using the normal input ramp and the on-chip gray-code generator, and then reading out the digitized values. In this way, except for the photodetectors, the DPS chip can be electrically tested and characterized without the need for light or optics.

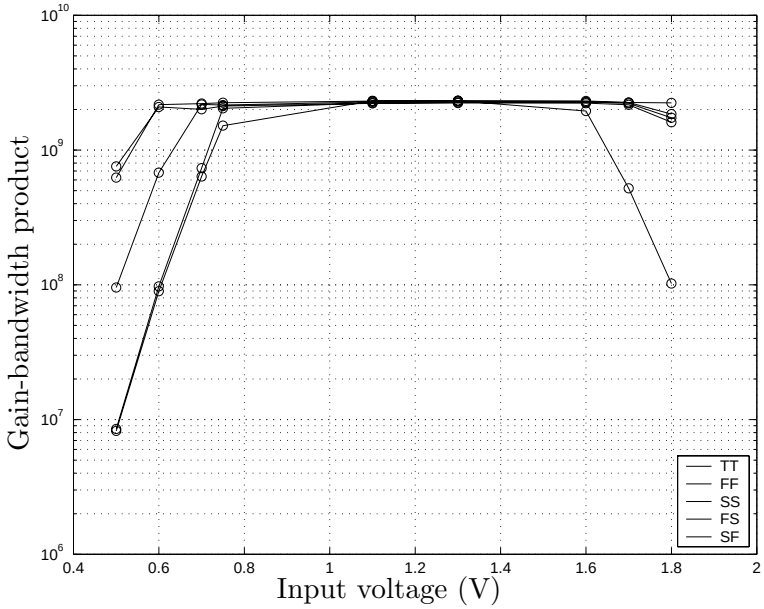


Figure 2.5: Comparator gain-bandwidth product vs. input voltage.

Figure 2.6 shows the layout of a 2×2 pixel block. The four large squares are the photogates, which are sized and spaced equally in the horizontal and vertical dimensions. The fill factor of this pixel is 15%. The silicide layer, which is opaque, was blocked from the photogates. The 3-stage comparators are seen near the top and bottom of the pixel quad. The digital memory is located in the two sections near the center of the quad. The smaller squares are the capacitors, with the transfer and reset transistors near by.

The pixels are mirrored about the horizontal axis in order to share the n-well and some of the power and bias lines. With digital CDS as discussed in Section 2.3, we did not observe any offset FPN due to mirroring. A small layout asymmetry, however, has resulted in odd/even row gain FPN. Memory bitlines (metal 3) and digital ground (metal 1) run vertically over the memory, while analog signal (metal 2) and power distribution (metal 4) run horizontally on top of the comparators. Metal 5 covers most of the array and acts as a light shield. Pixel array analog and digital grounds are kept separate in order to reduce noise coupling from the digital memory into the sensitive analog components.

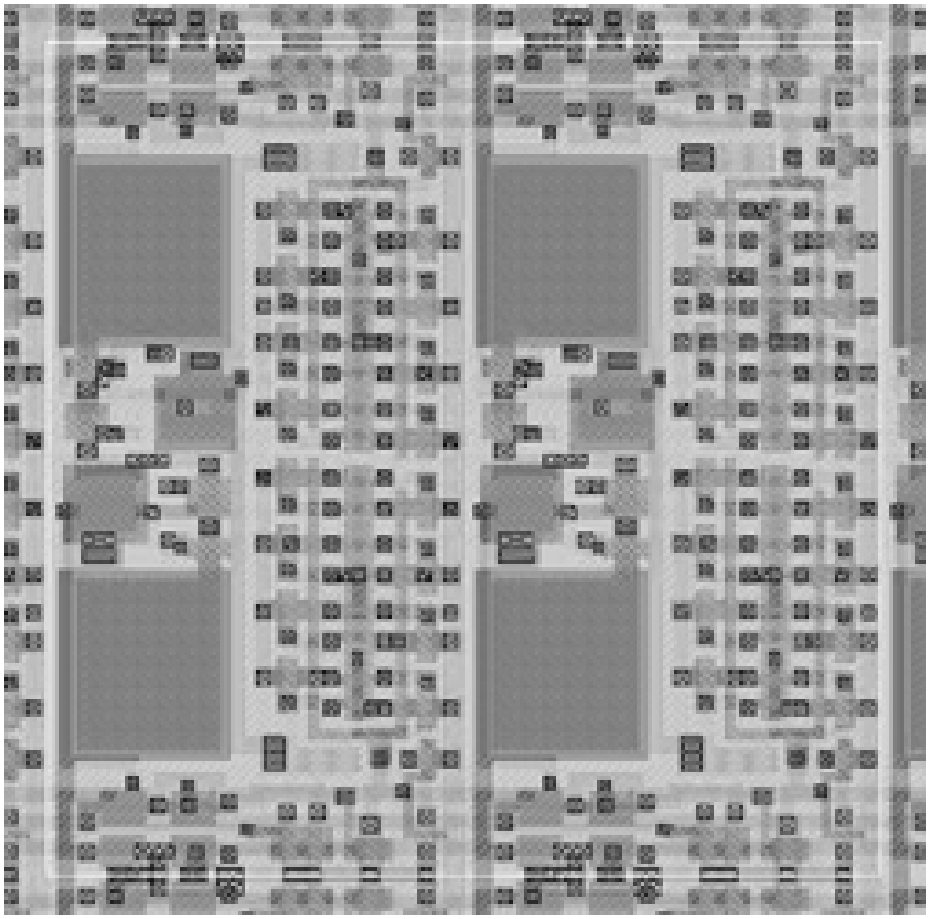


Figure 2.6: DPS pixel layout (2×2 pixel block shown). Pixel size is $9.4 \times 9.4\mu$m.

2.3 Sensor operation

In this section we describe the details of the DPS chip operation. First we describe the A/D conversion operation. Next we discuss the basic imaging modes of operation including single frame capture, digital correlated double sampling, high speed operation, and multiple image capture.

2.3.1 A/D conversion operation

Figure 2.7 illustrates the per-pixel single-slope A/D conversion technique used in our chip. The globally distributed voltage ramp is connected to each pixel's comparator inverting ("−") input. The non-inverting ("+") input on each comparator is directly connected to the sense node. The globally distributed gray coded counter values, shown as a stepped "digital ramp," are simultaneously applied to the per-pixel memory bit lines.

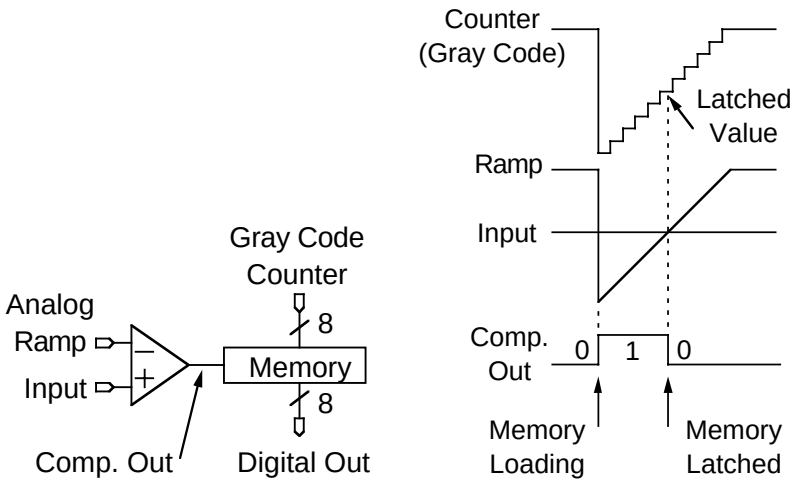


Figure 2.7: Single-slope ADC operation.

At the beginning of conversion, the ramp voltage is lowered to just below the lowest expected sense node voltage, which sets the comparator output to high. This enables the per-pixel memory to begin loading the gray code values. The ramp is

then swept linearly until it exceeds the reset voltage. Simultaneously, the gray code counter sweeps across an equivalent set of values (256 for 8 bits). As the ramp crosses each pixel's sense node voltage, its comparator output switches low, and the gray code value present at that moment is latched in the pixel's memory. At the end of conversion, each pixel's memory contains an 8-bit gray coded value that is a digital representation of its input voltage.

Although using a linear ramp is the typical approach, it is possible to use alternative ramp profiles such as piecewise linear or exponential curves that compress or expand different illumination ranges. It is also possible to change the gain of the A/D conversion by changing the voltage range of the analog ramp. One may also use alternate sequences for the digital inputs using the auxiliary inputs.

2.3.2 Imaging modes

Figure 2.8 depicts a simplified timing diagram for the DPS chip. Operation can be divided into four main phases: reset, integration, A/D conversion, and readout. The reset, integration and A/D conversion phases occur completely in parallel over the entire array, *i.e.*, in "snap-shot" mode, thus avoiding image distortion due to the row by row reset and readout of APS. To minimize charge injection into the sense node, which causes high FPN, a shallow reset signal falling edge is used. Sensor integration is limited by dark current or signal saturation on the long end and by internal time constants on the short end. Practical lower and upper bounds on integration time were found to be under 10μs to well over 100ms.

After integration, per-pixel single-slope A/D conversion is simultaneously performed for all pixels, as discussed in the previous subsection. Typical conversion time is 25μs, and can be as low as 20μs at the highest frame rates. After conversion, readout commences. The readout of one frame is completed in around 75μs.

Figure 2.9 shows the bias generation circuits for the pixel-level comparators, including the power-down circuitry. It consists of two sections, each with a current mirror, a transmission gate and a pull-down transistor. The comparators and the sense amps are turned on only during A/D conversion and readout phases by raising

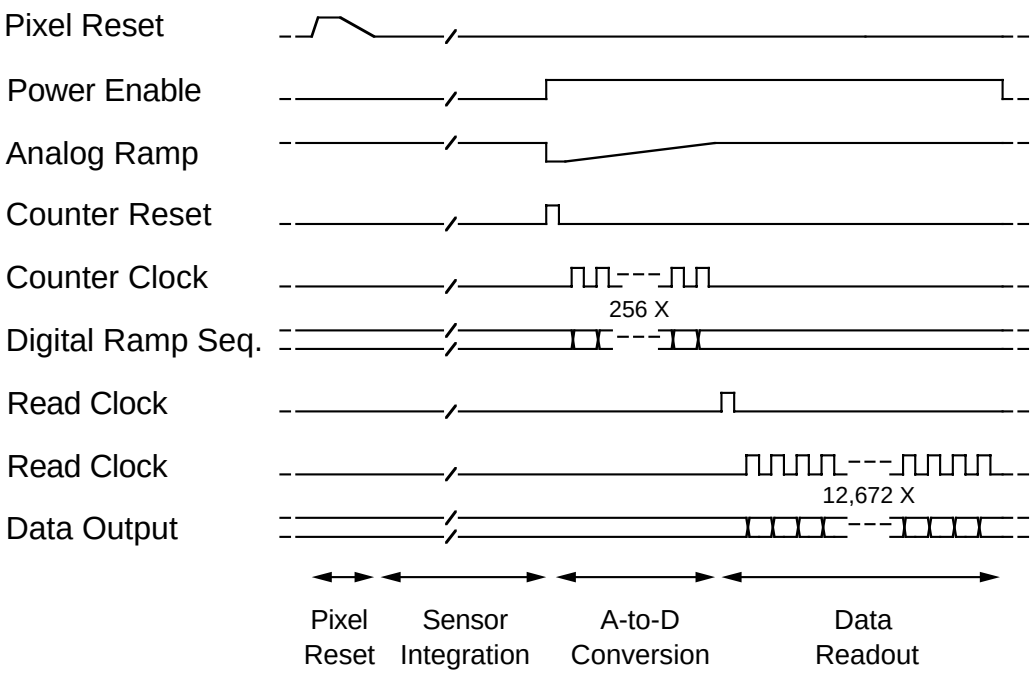


Figure 2.8: Simplified DPS timing diagram.

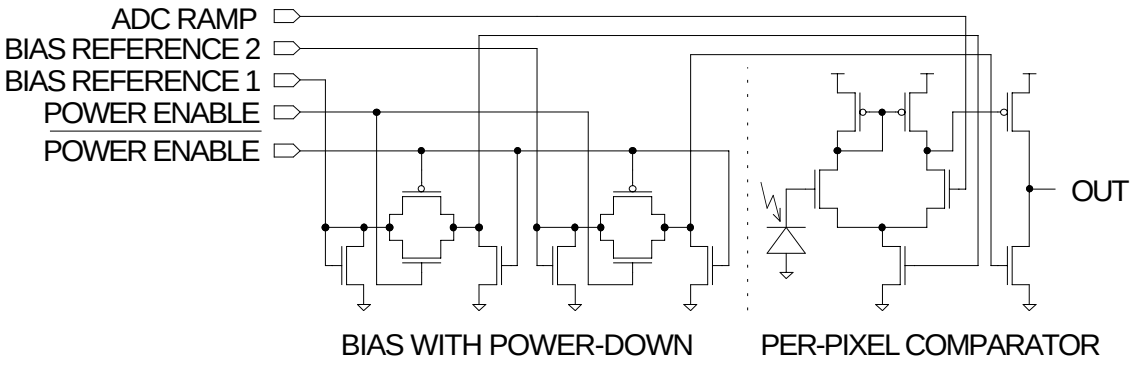


Figure 2.9: Comparator bias generation with power-down.

the Power Enable control. Power cycling is not essential, but since full frame conversion and readout can be accomplished in as little as 100μs, it can save several orders of magnitude of power when the chip is running at low frame rates and hence low A/D conversion/readout duty cycles.

The current mirrors divide down the external references ("Bias1, Bias2") by a factor of 100 in order to reduce the impedance of the external references for higher noise immunity. The transmission gates, operated by "Power Enable" and its complement, control whether the current mirror outputs are connected to the pixel array. When they are not connected, a pull-down transistor in each bias section connects the bias lines to ground, which shuts off the current source transistors in the two biased comparator stages. The circuits were designed, based on the loading of the 352×288 pixel array, to power down or up within 100ns.

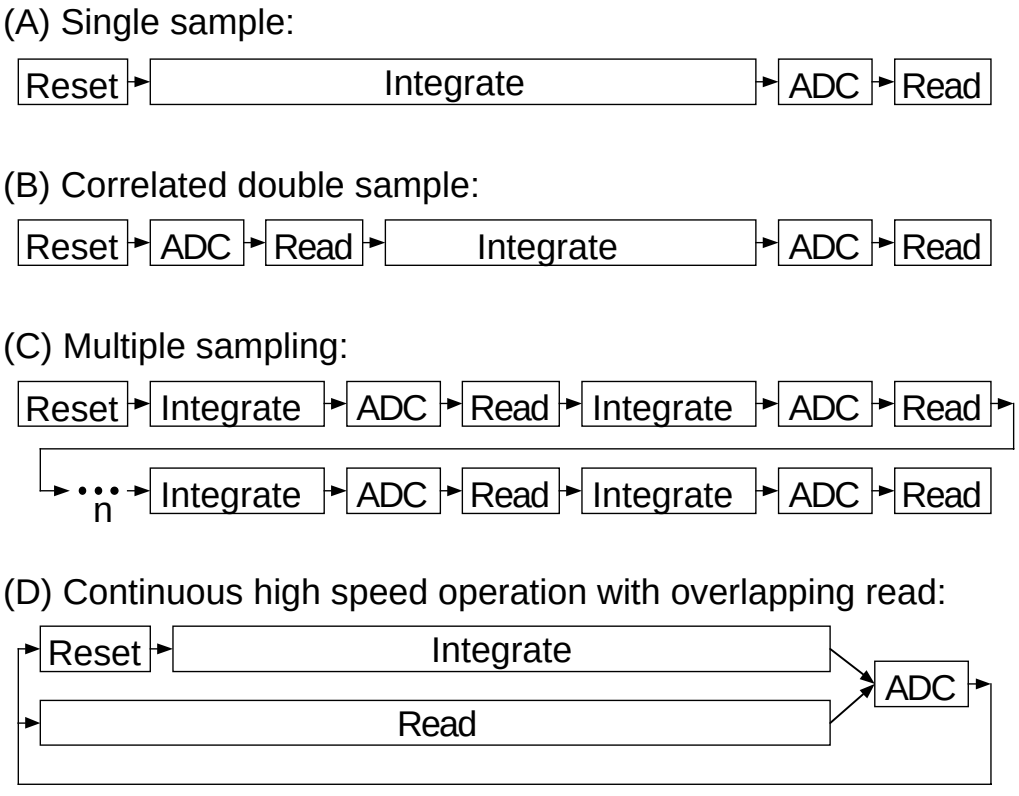


Figure 2.10: Basic DPS operation schemes.

The DPS chip operation is quite flexible. The timing and order of different phases can be easily programmed for different imaging applications. Figure 2.10 illustrates some of the possible imaging modes of the chip. Mode (A) is the single frame capture scenario we detailed in the previous subsection. At low speeds, each phase can be kept completely separate so that, for example, noise coupling due to digital readout need not influence the sensor reset, integration or conversion. Mode (B) is used to implement digital correlated double sampling by converting and reading a "reset frame" right after reset. The digitized reset frame is subtracted from the the digitized image frame externally. This is a "true" CDS operation, albeit digital in nature, in the sense that the two frames are taken after the same reset. Since a full frame conversion and readout can be completed in 100μs or less, more frames can be converted and read out during a single exposure time. This is denoted by mode (C) in Figure 2.10. For example, in a typical 30ms exposure time, tens or even hundreds of frames can be converted and read out. This "oversampling" can be used to implement several image enhancement and analysis applications such as dynamic range enhancement, motion estimation and compensation, and image stabilization. At the highest speeds, one can overlap and pipeline phases to maximize integration time and thus reduce the amount of illumination needed, as illustrated in mode (D). For example, at 10,000 frames/s, the combined reset, A/D conversion and readout time closely approaches the full frame period. By overlapping integration with readout of the previous frame, integration time can be increased from close to zero to about 75μs out of the 100μs frame period.

2.4 Testing and characterization

The DPS chip has been tested and characterized and shown to be fully functional. In the following subsections, we present the electrical, optical, and noise characterization results, and show results demonstrating that digital readout noise has little or no effect on the imaging performance of the chip.

2.4.1 Electrical and optical characterization results

Table 2.2 summarizes the DPS characterization results. Of particular interest is the measured average power consumption of only 50mW at 10,000 frames/s. The pixel-level comparators consume around 30mW of static power, while the digital readout circuits consume around 20mW of dynamic power. The poor imaging performance of the standard 0.18μm CMOS process resulted in high dark signal of 130mV/s and low QE of 13.6%. With conversion gain of 13.1μV/e$^-$, sensitivity was just over 0.1V/lux.s. Dark current and QE can be significantly improved with minor process modifications that should not significantly affect pixel area or chip performance. The ADC integral nonlinearity (INL) was measured over the maximum useful input range of 1V, at a typical 1,000 frames/s, without correlated double sampling, and averaged for all pixels. It was found to be 0.22% or 0.56 LSB. We also found that reducing the swing to 0.9V improves INL to 0.1% or 0.25 LSB.

Power used at 10K fps	50 mW, typical
ADC architecture	Per-pixel single-slope
ADC resolution	8-bits
ADC conversion time, typical	$\sim 25\mu$s, ($\sim 20\mu$s, min.)
ADC range, typical	1 V
ADC integral nonlinearity	<0.22% (0.56 LSB)
Dark current	130 mV/s, 10 nA/cm^2
Quantum efficiency	13.6%
Conversion gain	13.1 μV/e$^-$
Sensitivity	0.107 V/lux.s
FPN, dark w/CDS	0.027% (0.069 LSB)
Temporal noise, dark w/CDS	0.15% (0.38 LSB)

Table 2.2: DPS chip characterization summary. All numbers, except for power consumption are at 1000 frames/s.

To determine dark current, conversion gain, and QE of the DPS pixel, our chip included single pixel APS and DPS test structures that can be individually accessed and whose sense node voltages can be directly readout. The test structures are described in detail in [107]. For completeness, we provide the results that are relevant to the DPS chip.

The measured quantum efficiency curve for the photogate is shown in Figure 2.11. The maximum QE is around 13.6% at wavelegth of 600nm. The major reason for the low QE is the high recombination rate in the highly doped substrate.

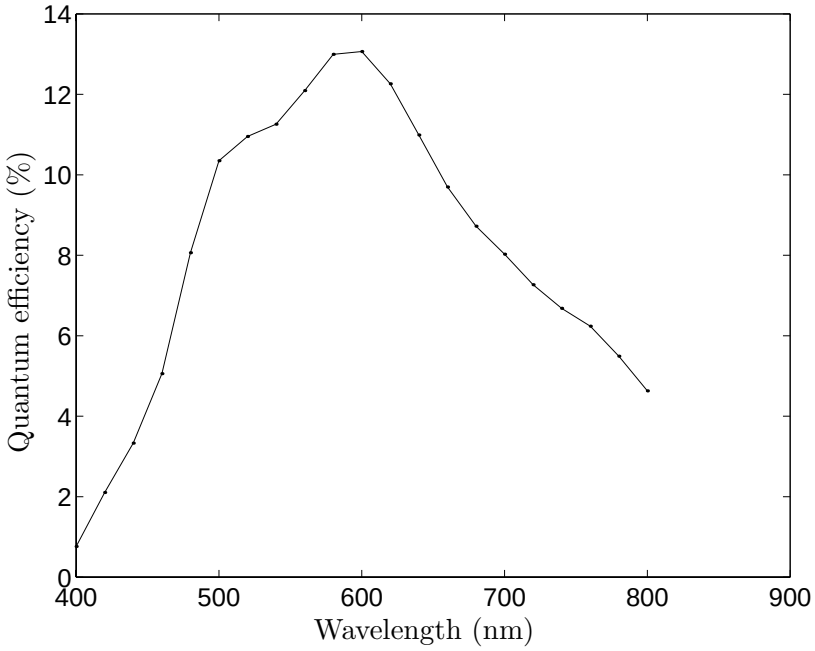


Figure 2.11: Measured quantum efficiency.

The measured dark current density was found to increase superlinearly with reverse bias voltage as shown in Figure 2.12. Since lowering PG voltage was also found to have little effect on QE [107], we typically operated PG at 2.1V or less.

We found that the transfer transistor of the photogate circuit suffered from high off-current in spite of using a thick oxide transistor. We performed an experiment to find out the transfer gate voltage needed to turn it off. Figure 2.13 plots the normalized quantum efficiency of the photogate device for TX voltage from 1V down to -0.6V. During the experiment, the reset voltage is kept at 1.15V and PG is pulsed between 0 and 2.1V. It is clear that the transfer gate cannot be turned off unless the gate voltage (TX) is negative.

Since the transfer gate cannot be turned off using non-negative TX voltages, we often operated the photogate as a photodiode by setting both PG and TX voltages to

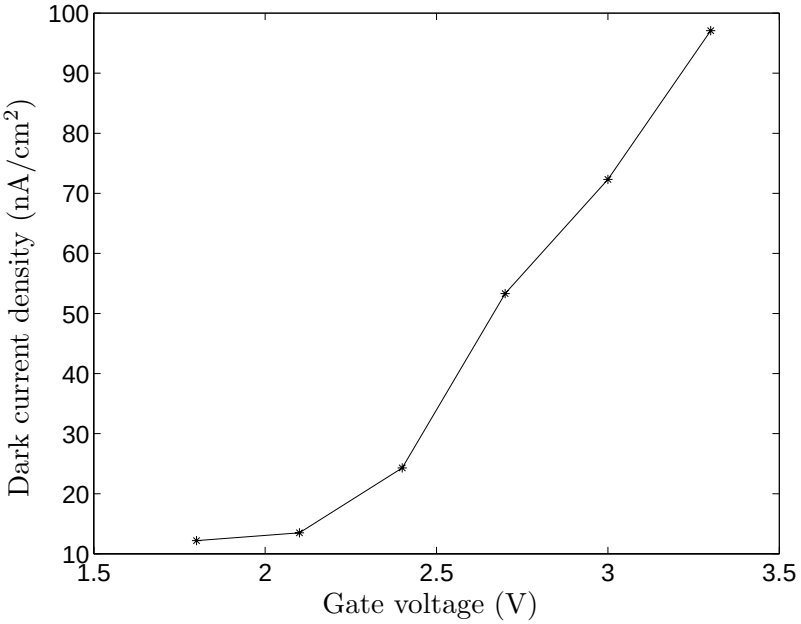


Figure 2.12: Measured photogate leakage current as a function of gate voltage.

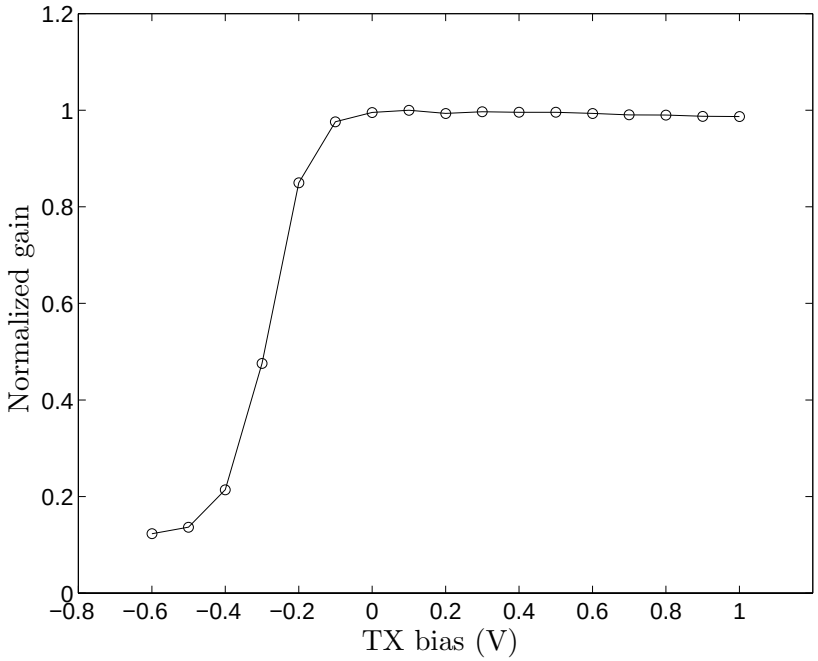


Figure 2.13: Normalized gain versus TX bias voltage.

optimum fixed voltages. We found that QE in this mode is only slightly lower than when operating in the normal photogate mode. In this photodiode mode, however, ADC linearity is slightly compromised at high frame rates, since integration continues during A/D conversion.

2.4.2 Temporal Noise and FPN

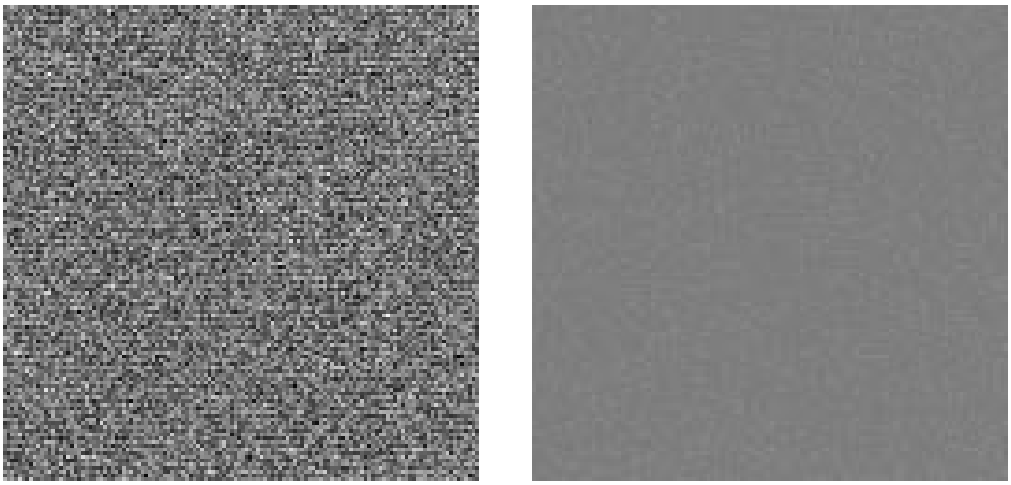


Figure 2.14: Images of fixed pattern noise without digital CDS (left) and with digital CDS (right) for an integration time of 1ms.

Correlated double sampling is perhaps the simplest example of how multiple image acquisitions within one integration can improve image quality. With digital CDS, FPN due to comparator offset and reset transistor threshold voltage and reset temporal noise are greatly reduced. In Figure 2.14, two images rendered using the same scale, show fixed pattern noise with and without correlated double sampling (performed digitally off-chip). On the left one can see significant noise that is primarily due to random variations in the pixel-level ADC comparator offset voltages. This random pattern of noise tends to be less visually objectionable than column fixed pattern noise, common in typical analog APS designs, that results in streaks. On

the right is the result after external digital CDS. The FPN has been reduced from 0.79% to 0.027%, RMS, a reduction by nearly a factor of 30. The final FPN number is about 1/15th of an LSB.

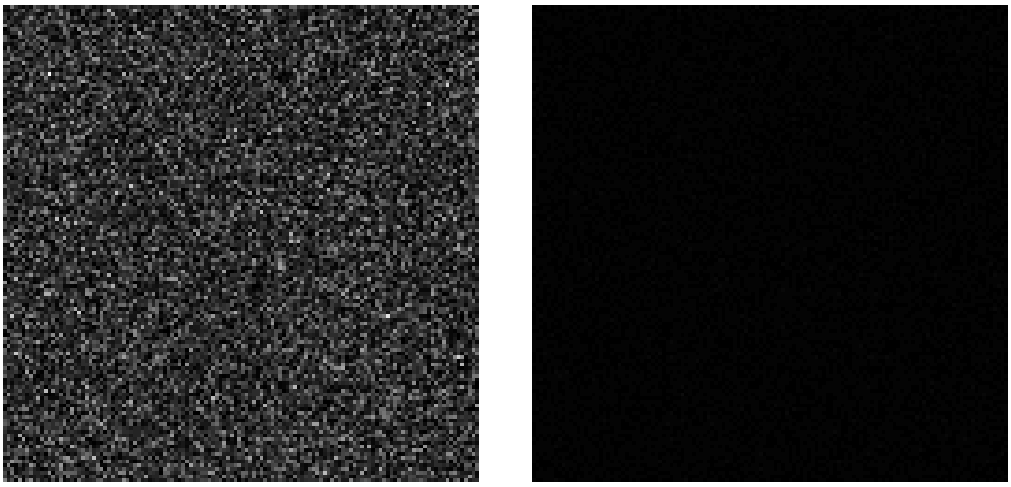


Figure 2.15: Images of temporal noise without digital CDS (left) and with digital CDS (right).

Figure 2.15 shows two images of temporal noise, with and without CDS, using a 1ms integration time, in the dark. In this case, the images show the variability in pixel values over time, with FPN removed. Using digital CDS, temporal noise has been reduced from 1.6% to 0.15% RMS, which is less than 1/3 of an LSB.

2.4.3 Digital noise coupling

Since DPS operation involves per-pixel digitization, digital pixel readout and high-speed I/O switching during integration, it is important to investigate the impact of digital coupling on the sensor performance. This is an especially important question given the ability of the DPS architecture to take hundreds of image samples within a single integration. To examine this issue, we devised the experiment explained with

the aid of Figure 2.16. The experiment was conducted under worst-case noise conditions, where the total integration time was minimized and the time spent converting and reading out was maximized to the point of being continuous.

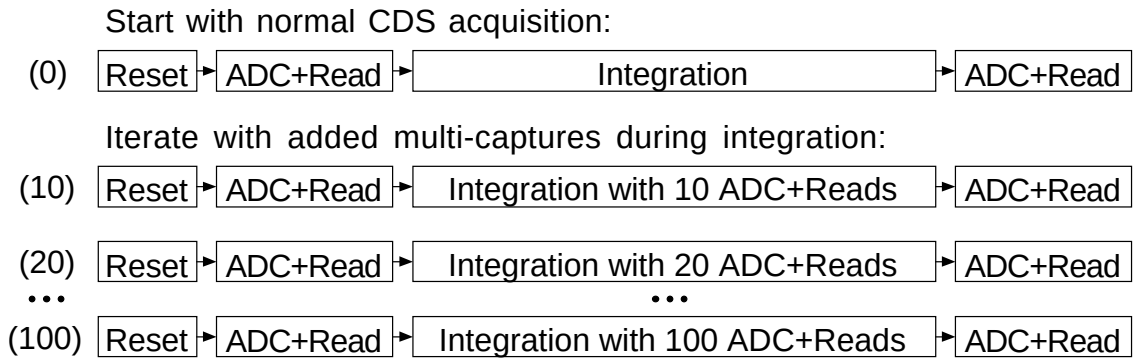


Figure 2.16: Digital read-induced noise experiment.

The experiment consisted of 11 sets of measurements. In the first set we performed a reset followed by an A/D conversion and a readout, integrated for 24ms, and then performed a final A/D conversion and a readout. Digital CDS was performed on the two captures to increase the sensitivity of the measurements. This is our baseline measurement that should include the least amount of digital coupling noise. The remaining 10 measurements were performed with $10, 20, \ldots, 100$ additional captures (*i.e.*, A/D conversions and frame readouts) within the 24ms integration time, respectively. Digital CDS was performed in each case, using the first and last samples immediately before and after the 24ms integration. Readout speed was set at 1.33GB/s and the total A/D conversion and readout time was 240μs per capture. With 100 captures within the 24ms integration, the chip was continuously converting and reading out during the integration period, with no gaps. The entire experiment was repeated twice: once in the dark and once using light from a stabilized light source and an integrating sphere to provide stable, uniform illumination.

The results are plotted in Figure 2.17. It is evident from the data that the noise curves are essentially flat: any trend is insignificant compared to the baseline (with no multi-capture) noise levels.

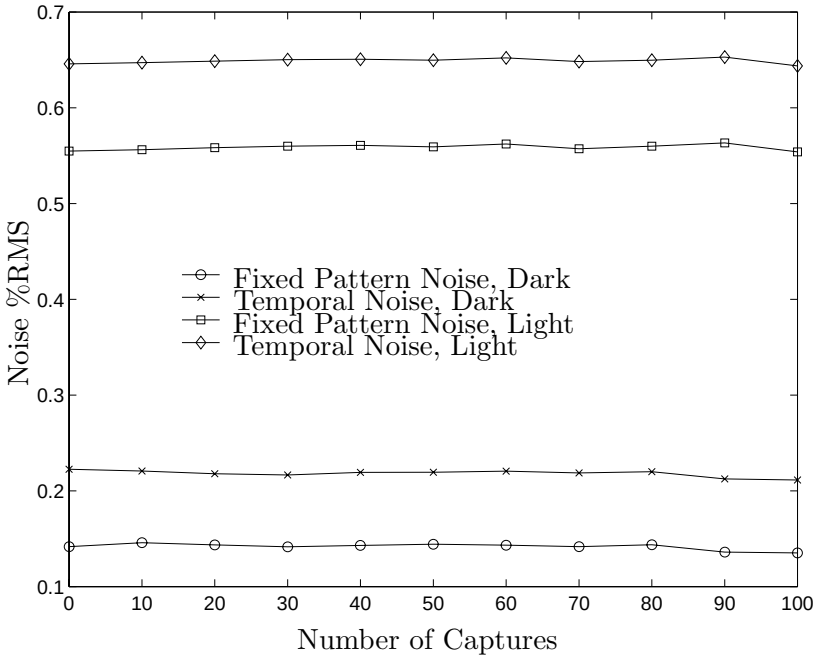


Figure 2.17: Plot of digital noise coupling results.

2.4.4 Sample images

Figure 2.18 shows an image acquired from a 1,000 frames/s (integration time just under 1ms) video stream. Except for digital CDS, no other processing was performed on the image. While the image is of a stationary subject, the chip was operated in continuous video mode. It highlights the image quality that can be obtained at these speeds, even with a small array size and fill factor. Note the subtle aliasing patterns in the finely engraved hair and down-sampling of the background engraving due to the low spatial resolution of the sensor.

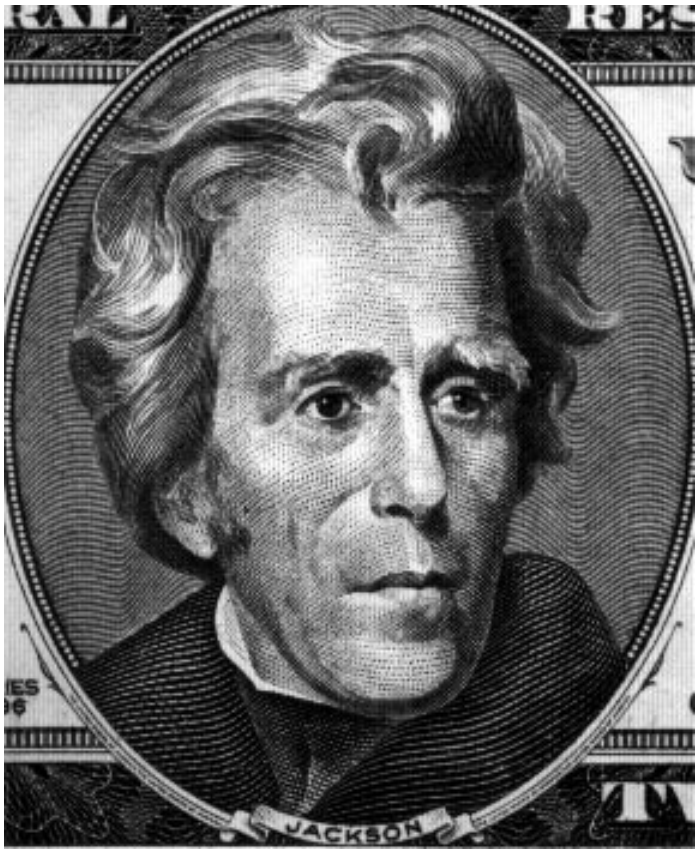


Figure 2.18: Sample image.

Figure 2.19 shows 4 frames (1, 11, 12 and 31) from a continuous 10,000 frames/s video sequence. They show a model airplane propeller rotating in front of a stationary resolution chart. The propeller is rotating at about 2,200 RPM, which results in each blade rotating by about 40 degrees. The scene is lit from two sides, forming two shadows that follow the propeller. At this speed, neither CDS nor power cycling is used, and each frame's reset and integration is overlapped with the readout of the previous frame's data (mode (D) in Figure 2.10), as explained earlier. The overall image quality appears to be satisfactory for high speed motion analysis and other high speed video applications.

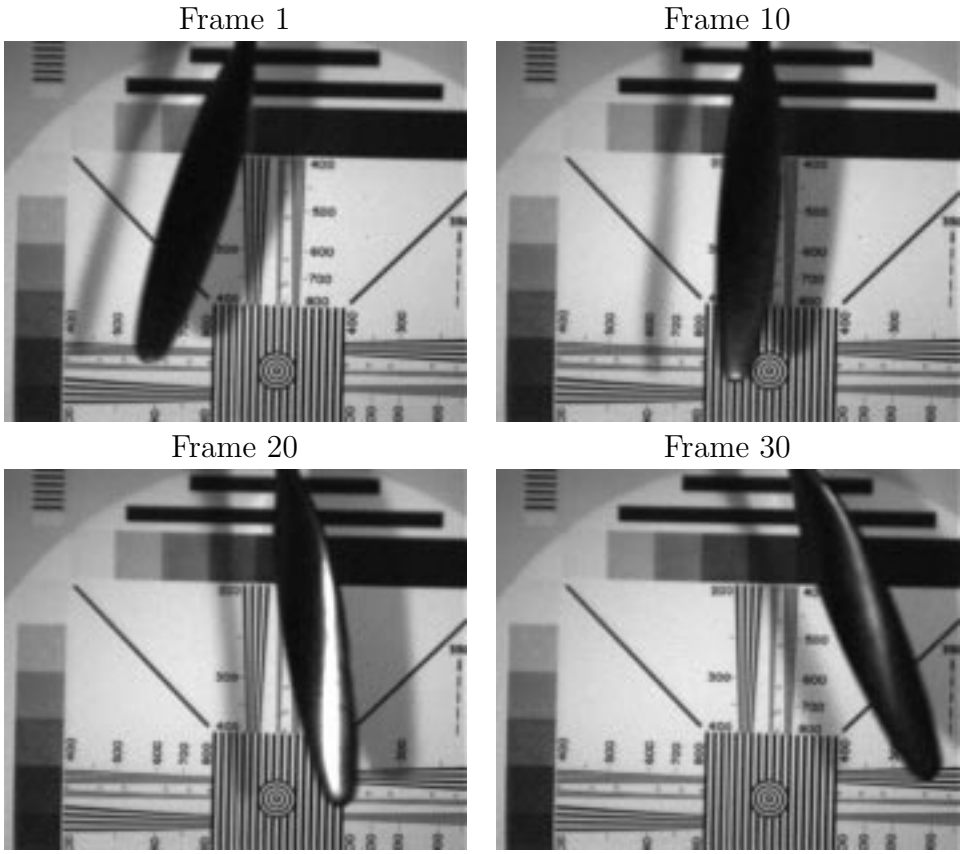


Figure 2.19: 10,000 frames/s image sequence (frames 1, 10, 20, and 30 are shown).

2.5 Summary

A Digital Pixel Sensor implemented in a standard digital CMOS 0.18μm process was described. The 3.8 million transistor chip has 352×288 pixels. Each $9.4 \times 9.4\mu$m pixel contains 37 transistors implementing a photogate circuit, an 8-bit single-slope ADC, and 8 3T DRAM cells. Pixel reset, integration and A/D conversion occur in full frame parallel "snap-shot" fashion. Data is read out via a 64 bit wide bus at 167 MHz for a peak data bandwidth of 1.34GB/s. The DPS chip achieved continuous 10,000

frames/s operation and sustained 1 Gpixels/s throughput. With further scaling, significant additional per-pixel memory, processing power and speed will inevitably become practical, further enhancing the capabilities of the DPS approach.

With this test chip, we demonstrated the scalability and high speed potential of DPS. The test chip provides a platform for experimenting with algorithms and circuits that exploit high speed non-destructive readout advantage of CMOS image sensors, as will be described in the following chapters.

Chapter 3

Photocurrent Estimation Algorithms

Chapter 2 demonstrated the high speed, non-destructive readout capability of CMOS digital pixel image sensor, however, as described in Chapter 1, CMOS image sensors generally suffer from lower SNR and dynamic range than CCDs due to their higher readout noise, and thus higher noise under dark conditions. The high speed non-destructive readout capability of a CMOS image sensor and the ability to integrate memory and signal processing with the sensor on the same chip, open up many possibilities for enhancing its SNR and dynamic range.

Earlier work [80, 102] have demonstrated the use of multiple capture to enhance image sensor dynamic range. The idea is to capture several images at different times within the normal exposure time — shorter exposure time images capture the brighter areas of the scene while longer exposure time images capture the darker areas of the scene. The captured images are then combined into a single high dynamic range image by appropriately scaling each pixel's last sample before saturation. Conventional correlated double sampling (CDS) is used to reduce reset and offset FPN. It was shown that this multiple capture scheme achieves higher SNR than other dynamic

range enhancement schemes [65]. However, this scheme does not take full advantage of the multiple pixel samples. Readout noise, whose power is doubled as a result of performing CDS, remains as high as for conventional sensor operation. As a result, dynamic range is only extended at the high illumination end.

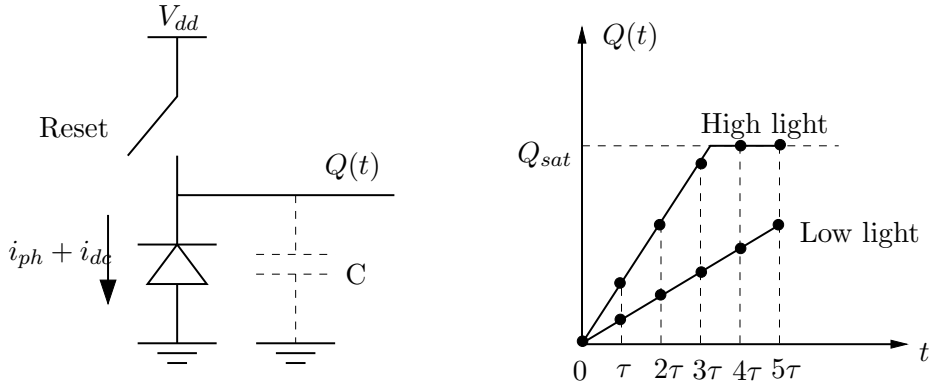


Figure 3.1: Simplified photodiode pixel model and the photocharge $Q(t)$ vs. time t under different light intensity

Figure 3.1 depicts the idea. During capture, each pixel converts incident light into photocurrent i_{ph}, for $0 \leq t \leq T$, where T is the exposure time. The photocurrent is integrated onto a capacitor and the charge $Q(T)$ (or voltage) is read out at the end of exposure time T. Dark current i_{dc} and additive noise corrupt the photocharge. The noise can be expressed as the sum of three independent components, (i) shot noise $U(T) \sim \mathcal{N}(0, q(i_{ph} + i_{dc})T)$, where q is the electron charge, (ii) readout circuit noise $V(T)$ (including quantization noise) with zero mean and variance σ_V^2, and (iii) reset and FPN noise C with zero mean and variance σ_C^2, which is the same for all multiple captures. Thus the output charge from a pixel can be expressed as

$$Q(T) = \begin{cases} (i_{ph} + i_{dc})T + U(T) + V(T) + C, & \text{for } Q(T) \leq Q_{sat} \\ Q_{sat}, & \text{otherwise} \end{cases}$$

where Q_{sat} is the saturation charge, also referred to as *well capacity*. The SNR can

be expressed as

$$\mathrm{SNR}(i_{ph}) = 10 \log_{10} \frac{(i_{ph}T)^2}{q(i_{ph} + i_{dc})T + \sigma_V^2 + \sigma_C^2}$$

Note that SNR increases with i_{ph}, first at 20dB per decade when reset and readout noise dominate, then at 10dB per decade when shot noise dominates. SNR also increases with T. Thus it is always preferred to have the longest possible exposure time. Therefore, [80, 102] use the last sample before saturation with proper scaling as the photocurrent estimate. The justification for ignoring all other samples before saturation is that the last sample has the highest SNR. This is quite acceptable at the high illumination end, where shot noise dominates. However, only using the last sample to estimate the photocurrent is virtually like throwing away the signal and noise information carried in those earlier samples. As will be shown in this chapter, this will result in suboptimal SNR and dynamic range, especially at low illumination condition.

This chapter explores the use of linear mean-square-error estimation to more fully exploit the multiple pixel samples to reduce readout noise and thus extend dynamic range at the low illumination end. We present three estimation algorithms: (1) a recursive estimator when reset noise and offset FPN are ignored, (2) a non-recursive algorithm when reset noise and FPN are considered, and (3) a recursive estimation algorithm for case (2), which achieves mean square error close to the non-recursive algorithm without the need to store all the samples. The later recursive algorithm is attractive since it requires the storage of only a few pixel values per pixel, which makes its implementation in a single chip digital imaging system feasible.

3.1 Estimation Algorithms

We assume $n+1$ pixel charge samples Q_k captured at times $0, \tau, 2\tau, \ldots, n\tau = T$ and define the pixel current $i = i_{ph} + i_{dc}$. The kth charge sample is thus given by

$$Q_k = ik\tau + \sum_{j=1}^{k} U_j + V_k + C, \text{ for } 0 \le k \le n, \tag{3.1}$$

where V_k is the readout noise of the kth sample, U_j is the shot noise generated during the time interval $((j-1)\tau, j\tau]$, and C is the reset noise. The U_js, V_k, C are independent zero mean random variables with

$$\begin{aligned} E(V_k^2) &= \sigma_V^2 > 0, \text{ for } 0 \le k \le n, \\ E(U_j^2) &= \sigma_U^2 = qi\tau, \text{ for } 1 \le j \le k, \text{ and} \\ E(C^2) &= \sigma_C^2. \end{aligned}$$

We wish to estimate the photocurrent i from the $n+1$ samples. This is a parameter estimation problem that can be formulated using several criteria, such as likelihood ratio and mean square error [109]. Maximum likelihood estimation achieves the smallest probability of error, but is generally difficult to derive and leads to non-linear solutions that are not easy to implement in practice. In this thesis we will only focus on linear minimum mean square estimation (MMSE) [108].

Due to motion and/or saturation, the estimation may not use all the $n+1$ samples. The detection algorithm presented in the next chapter determines the last sample before saturation/motion to be included in the estimation. Denoting the last sample to be included by k, $1 \le k \le n$, the linear MMSE problem is formulated as follows:

At time $k\tau$, we wish to find the best unbiased linear estimate, $\hat{I}_k$, of i given $\{Q_0, Q_1, \ldots, Q_k\}$, *i.e.*, we wish to find $b_0^{(k)}, b_1^{(k)}, \ldots, b_k^{(k)}$ such that [1]

$$\hat{I}_k = \sum_{j=0}^{k} b_j^{(k)} Q_j, \tag{3.2}$$

minimizes

$$\Phi_k^2 = E(\hat{I}_k - i)^2.$$

[1]For the coefficient $b_j^{(k)}$, we use superscript (k) to represent the number of captures used and use subscript as the index of the coefficients for each capture.

subject to

$$E(\hat{I}_k) = i.$$

Next, we present three estimation algorithms:

- An optimal recursive algorithm when reset noise and offset FPN are ignored. In this case only the latest estimate and the new sample are needed to update the pixel photocurrent estimate.
- An optimal non-recursive algorithm when reset noise and FPN are considered.
- A sub-optimal recursive estimator for the second case, which is shown to yield mean square error close to the non-recursive algorithm without the need to store all the samples.

The later recursive algorithm is attractive since it requires the storage of only a constant number of values per pixel.

3.1.1 Estimation Ignoring Reset Noise and FPN

Here we ignore reset noise and offset FPN, *i.e.*, set $C = 0$. Even though this assumption is not realistic for CMOS sensors, it is reasonable for high end CCDs using very high resolution ADC. As we shall see, the optimal estimate in this case can be cast in a recursive form, which is not the case when reset noise is considered.

To derive the best estimate, define the pixel *current samples* as

$$\tilde{I}_k = \frac{Q_k}{k\tau} = i + \frac{\sum_{j=1}^{k} U_j}{k\tau} + \frac{V_k}{k\tau}, \text{ for } 1 \le k \le n \tag{3.3}$$

Thus, given the samples $\{\tilde{I}_1, \tilde{I}_2, \ldots, \tilde{I}_k\}$, we wish to find the best unbiased linear estimate of the parameter i, *i.e.*, weights $a_1^{(k)}, a_2^{(k)}, \ldots, a_k^{(k)}$ such that

$$\hat{I}_k = \sum_{j=1}^{k} a_j^{(k)} \tilde{I}_j, \tag{3.4}$$

that minimizes

$$\Phi_k^2 = E(\hat{I}_k - i)^2, \tag{3.5}$$

subject to

$$E(\hat{I}_k) = i. \tag{3.6}$$

The mean square error (MSE) Φ_k^2 is given by

$$\begin{aligned} \Phi_k^2 &= E(\hat{I}_k - i)^2 \\ &= E(\textstyle\sum_{j=1}^{k} a_j^{(k)}(i + \frac{\sum_{l=1}^{j} U_l}{j\tau} + \frac{V_j}{j\tau}) - i)^2 \\ &= \textstyle\sum_{j=1}^{k}((\sum_{l=j}^{k} \frac{a_l^{(k)}}{l})^2 \frac{\sigma_U^2}{\tau^2} + (\frac{a_j^{(k)}}{j})^2 \frac{\sigma_V^2}{\tau^2}). \end{aligned} \tag{3.7}$$

This is a convex optimization problem with a linear constraint as in (3.6). To solve it, we define the Lagrangian

$$F(a_1^{(k)}, a_2^{(k)}, \ldots, a_k^{(k)}) = \Phi_k^2 + \lambda(\sum_{j=1}^{k} a_j^{(k)} - 1) \tag{3.8}$$

where λ is the Lagrange multiplier.

The optimal weights can be found using the conditions:

$$\begin{cases} \bigtriangledown F &= \left[\begin{array}{cccc} \frac{\partial F}{\partial a_1^{(k)}} & \frac{\partial F}{\partial a_2^{(k)}} & \cdots & \frac{\partial F}{\partial a_k^{(k)}} \end{array} \right]^T = 0, \\ \sum_{j=1}^{k} a_j^{(k)} &= 1. \end{cases} \tag{3.9}$$

and we get (see Appendix A)

$$a_j^{(k)} = ja_1^{(k)} + \frac{j}{j-1}a_{j-1}^{(k)} + \frac{j\sigma_U^2}{\sigma_V^2}(\sum_{l=1}^{j-1}\frac{a_l^{(k)}}{l}), \text{ where } 2 \leq j \leq k. \tag{3.10}$$

Now to see that the optimal estimate can be cast in a recursive form, we define the set of weights b_j, such that:

$$\begin{cases} b_1 &= 1, \\ b_j &= jb_1 + \frac{j}{j-1}b_{j-1} + \frac{j\sigma_U^2}{\sigma_V^2}(\sum_{l=1}^{j-1}\frac{b_l}{l}) \text{ for } j \geq 2. \end{cases} \tag{3.11}$$

$a_j^{(k)}$ can be represented in terms of b_j as:

$$a_j^{(k)} = \frac{b_j}{\sum_{l=1}^{k} b_l} \text{ for } 1 \leq j \leq k, \tag{3.12}$$

The optimal photocurrent estimate $\hat{I}_k$ can be written in a recursive form in terms of b_k, the latest photocurrent sample $\tilde{I}_k$, and the previous estimate $\hat{I}_{k-1}$ as (see Appendix A)

$$\hat{I}_k = \hat{I}_{k-1} + h_k(\tilde{I}_k - \hat{I}_{k-1}), \tag{3.13}$$

where

$$h_k = \frac{b_k}{g_k} \text{ and } g_k = \sum_{l=1}^{k} b_l. \tag{3.14}$$

The MSE Φ_k^2 can also be expressed in a recursive form as

$$\Phi_k^2 = \frac{g_{k-1}^2}{g_k^2}\Phi_{k-1}^2 + \frac{1}{g_k^2}((2b_k g_{k-1} + b_k^2)\frac{\sigma_U^2}{k\tau^2} + b_k^2\frac{\sigma_V^2}{(k\tau)^2}) \tag{3.15}$$

This is important because Φ_k^2 will be used later in the motion detection algorithm.

The first estimator $\hat{I}_1$ is approximated by $\tilde{I}_1$. In Equation 3.11, 3.15, $\sigma_U^2 = qi\tau$ is

approximated using the latest estimate of i, $\hat{I}_k$, *i.e.*, $\sigma_U^2 = q\hat{I}_k\tau$. We found that this approximation yields MSE very close to the optimal case, *i.e.*, when i is known.

3.1.2 Estimation Considering Reset noise and FPN

With reset noise and offset FPN taken into consideration, we redefine $\tilde{I}_k$ as

$$\tilde{I}_k = \frac{Q_k - wQ_0}{k\tau}, \text{ for } 1 \leq k \leq n. \tag{3.16}$$

The weight w is obtained by solving for the optimal b_0 in equation (3.2) (see Appendix B), which yields

$$w = \frac{\sigma_C^2}{\sigma_C^2 + \sigma_V^2}. \tag{3.17}$$

Note that $\tilde{I}_k$ corresponds to an estimate with a *weighted* correlated double sampling (CDS) operation. The weighting has the effect of reducing the additional readout noise due to CDS.

The pixel current estimate given the first k samples can be expressed as

$$\hat{I}_k = \mathbf{A}_k\tilde{\mathbf{I}}_k, \tag{3.18}$$

where

$$\begin{aligned} \mathbf{A}_k &= [a_1^{(k)}\ a_2^{(k)}\ \ldots\ a_2^{(k)}], \text{ and} \\ \tilde{\mathbf{I}}_k &= [\tilde{I}_1\ \tilde{I}_2\ \ldots\ \tilde{I}_k]^T. \end{aligned}$$

The optimal coefficient vector $\mathbf{A}_k$ is given by (see Appendix C)

$$\mathbf{A}_k = -(M_k\frac{\sigma_U^2}{\tau^2} + D_k\frac{\sigma_V^2}{\tau^2})^{-1}\frac{\lambda}{2}L_k \tag{3.19}$$

where

$$M_k = \begin{bmatrix} 1 & \frac{1}{2} & \dots & \frac{1}{k} \\ 1 & 1 & \dots & \frac{2}{k} \\ \dots & & & \\ 1 & 1 & \dots & 1 \end{bmatrix}, \; L_k = \begin{bmatrix} 1 \\ 2 \\ \vdots \\ k \end{bmatrix},$$

$$D_k = \begin{bmatrix} 2w & \frac{w}{2} & \frac{w}{3} & \dots & \frac{w}{k} \\ w & w & \frac{w}{3} & \dots & \frac{w}{k} \\ w & \frac{w}{2} & \frac{2w}{3} & \dots & \frac{3}{k} \\ \dots & & & & \\ w & \frac{w}{2} & \frac{w}{3} & \dots & \frac{2w}{k} \end{bmatrix}.$$

and λ is the Lagrange multiplier for the unbiased constraint.

It can be shown (see Appendix D) that the above solution cannot be expressed in a recursive form and thus finding $\hat{I}_k$ requires the storage of the vector $\tilde{\mathbf{I}}_k$ and inverting a $k \times k$ matrix.

3.1.3 Recursive Algorithm

Now, we restrict ourselves to recursive estimates, *i.e.*, estimates of the form

$$\hat{I}_k = \hat{I}_{k-1} + h_k(\tilde{I}_k - \hat{I}_{k-1}), \tag{3.20}$$

where again

$$\tilde{I}_k = \frac{Q_k - wQ_0}{k\tau}.$$

The coefficient h_k can be found by solving the equations

$$\begin{aligned} \frac{d\,\Phi_k^2}{d\,h_k} &= \frac{d\,E(\hat{I}_k - i)^2}{d\,h_k} = 0, \text{ and} \\ E\hat{I}_k &= i. \end{aligned}$$

Define the MSE of $\tilde{I}_k$ as

$$\Delta_k^2 = E(\tilde{I}_k - i)^2 = \frac{1}{k^2\tau^2}(k\sigma_U^2 + (1+w)\sigma_V^2) \tag{3.21}$$

and the covariance between $\tilde{I}_k$ and $\hat{I}_k$ as

$$\begin{aligned} \Theta_k &= E(\tilde{I}_k - i)(\hat{I}_k - i) \\ &= (1-h_k)\tfrac{k-1}{k}\Theta_{k-1} - \tfrac{(1-h_k)h_{k-1}}{k(k-1)\tau^2}\sigma_V^2 + h_k\Delta_k^2. \end{aligned} \tag{3.22}$$

The MSE of $\hat{I}_k$ can be expressed in terms of Δ_k^2 and Θ_k as

$$\begin{aligned} \Phi_k^2 &= (1-h_k)^2\Phi_{k-1}^2 + \tfrac{2(k-1)(1-h_k)h_k}{k}\Theta_{k-1} \\ &\quad - \tfrac{2h_{k-1}(1-h_k)h_k}{k(k-1)\tau^2}\sigma_V^2 + {h_k}^2\Delta_k^2. \end{aligned} \tag{3.23}$$

To minimize the MSE, we require that

$$\frac{d\,\Phi_k^2}{d\,h_k} = 0,$$

Which gives (see Appendix E)

$$h_k = \frac{\Phi_{k-1}^2 - \frac{(k-1)}{k}\Theta_{k-1} + \frac{h_{k-1}\sigma_V^2}{k(k-1)\tau^2}}{\Phi_{k-1}^2 - \frac{2(k-1)}{k}\Theta_{k-1} + \frac{2h_{k-1}\sigma_V^2}{k(k-1)\tau^2} + \Delta_k^2} \tag{3.24}$$

Note that h_k, Θ_k and Φ_k can all be recursively updated.

To summarize, the suboptimal recursive algorithm is as follows.

- Set initial parameter and estimate values as follows:

$$\begin{aligned} h_1 &= 1 \\ \tilde{I}_1 &= \frac{(Q_1 - wQ_0)}{\tau} \\ \hat{I}_1 &= \tilde{I}_1 \\ \Delta_1^2 &= \frac{\sigma_U^2 + (1+w)\sigma_V^2}{\tau^2} \\ \Phi_1^2 &= \Delta_1^2 \\ \Theta_1 &= \Delta_1^2 \end{aligned}$$

- At each iteration, the parameter and estimate values are updated as follows:

$$\tilde{I}_k = \frac{(Q_k - wQ_0)}{k\tau}$$

$$\Delta_k^2 = \frac{1}{k^2\tau^2}(k\sigma_U^2 + (1+w)\sigma_V^2)$$

$$h_k = \frac{\Phi_{k-1}^2 - \frac{(k-1)}{k}\Theta_{k-1} + \frac{h_{k-1}\sigma_V^2}{k(k-1)\tau^2}}{\Phi_{k-1}^2 - \frac{2(k-1)}{k}\Theta_{k-1} + \frac{2h_{k-1}\sigma_V^2}{k(k-1)\tau^2} + \Delta_k^2}$$

$$\Theta_k = (1-h_k)\frac{k-1}{k}\Theta_{k-1} - \frac{(1-h_k)h_{k-1}}{k(k-1)\tau^2}\sigma_V^2 + h_k\Delta_k^2$$

$$\Phi_k^2 = (1-h_k)^2\Phi_{k-1}^2 + 2h_k\Theta_k - {h_k}^2\Delta_k^2.$$

$$\hat{I}_k = \hat{I}_{k-1} + h_k(\tilde{I}_k - \hat{I}_{k-1})$$

Note that to find the new estimate $\hat{I}_k$ using this suboptimal recursive algorithm,

only three parameters, h_k, Φ_k and Θ_k, the old estimate $\hat{I}_{k-1}$, and the new sample value $\tilde{I}_k$ are needed. Thus only a small amount of memory per pixel is required independent of the number of images captured.

3.2 Simulation Results

In this section we present simulation results that demonstrate the SNR improvements using the non-recursive algorithm described in Subsection 3.1.2, the recursive algorithm in Subsection 3.1.3, and the multiple capture scheme [102].

The simulation results are summarized in Figures 3.2, 3.3, 3.4 and 3.5. The sensor parameters assumed in the simulations are as follows.

$$\begin{aligned} Q_{sat} &= 18750 \text{ e-} \\ i_{dc} &= 0.1 \text{ fA} \\ \sigma_V &= 60 \text{ e-} \\ \sigma_C &= 62 \text{ e-} \\ T &= 32 \text{ ms} \\ \tau &= 1 \text{ ms} \end{aligned}$$

Figure 3.2 plots the weights for the non-recursive and recursive algorithms in Subsection 3.1.2 and Subsection 3.1.3, respectively. Note that later samples are weighted much higher than earlier ones since later samples have higher SNR. As read noise decreases this becomes more pronounced – the best estimate is to use the last sample only if sensor read noise is zero. Also note that weights for the nonrecursive algorithm can be negative. It is preferred to weight the later samples higher since they have higher SNR, and this can be achieved by using negative weights for some of the earlier samples under the unbiased estimate constrain (sum of the weights equals one).

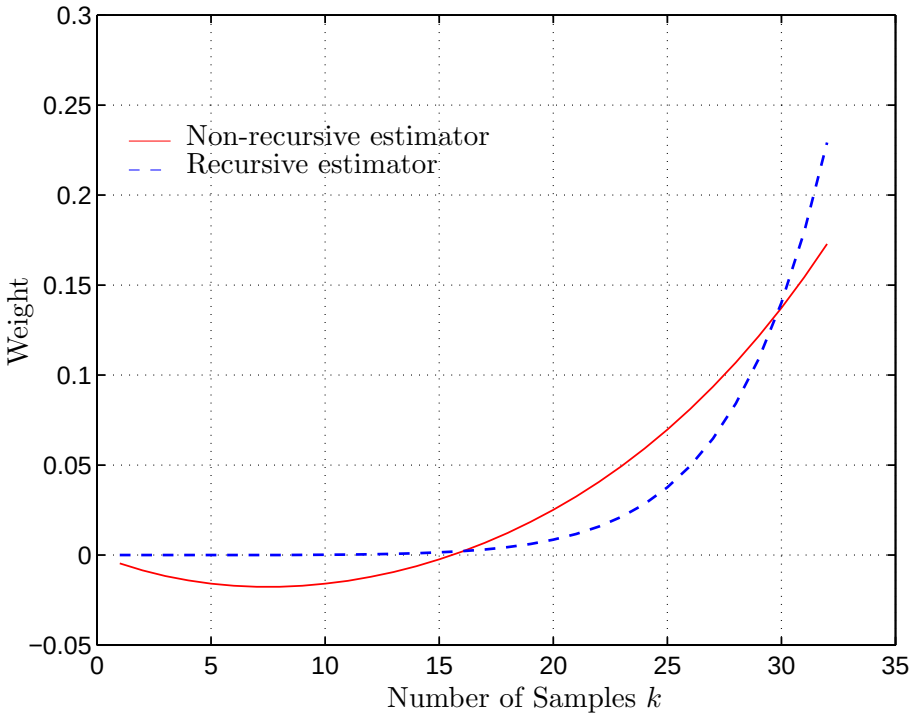


Figure 3.2: Estimation weights used in the non-recursive and recursive algorithms.

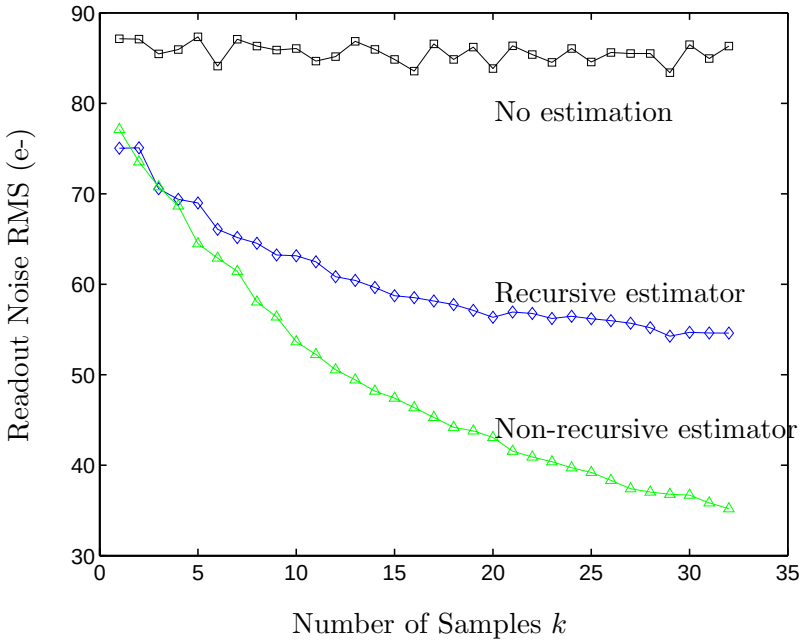


Figure 3.3: Equivalent Readout noise rms value vs. k.

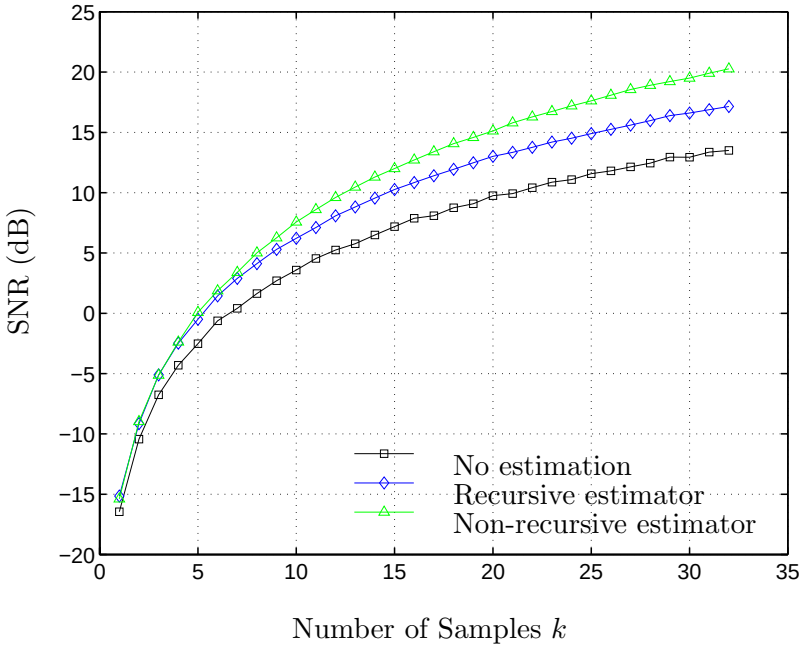


Figure 3.4: SNR vs. k.

Figures 3.3 and 3.4 compare the equivalent readout noise RMS and SNR values at low illumination level corresponding to $i_{ph} = 2$ fA as a function of the number of samples k for conventional sensor operation and using the non-recursive and the recursive estimation algorithms. As can be seen in Figure 3.3, the equivalent readout noise after the last sample is reduced from 86 e- when no estimation is used to 35.8 e- when the non-recursive estimator is used and to 56.6 e- when the recursive estimator is used. Equivalently, as can be seen in Figure 3.4, SNR increases by 6.6 dB using the non-recursive estimator versus 3.34 dB using the recursive estimator. Also note the drop in the equivalent readout noise RMS due to the weighted CDS used in our algorithms.

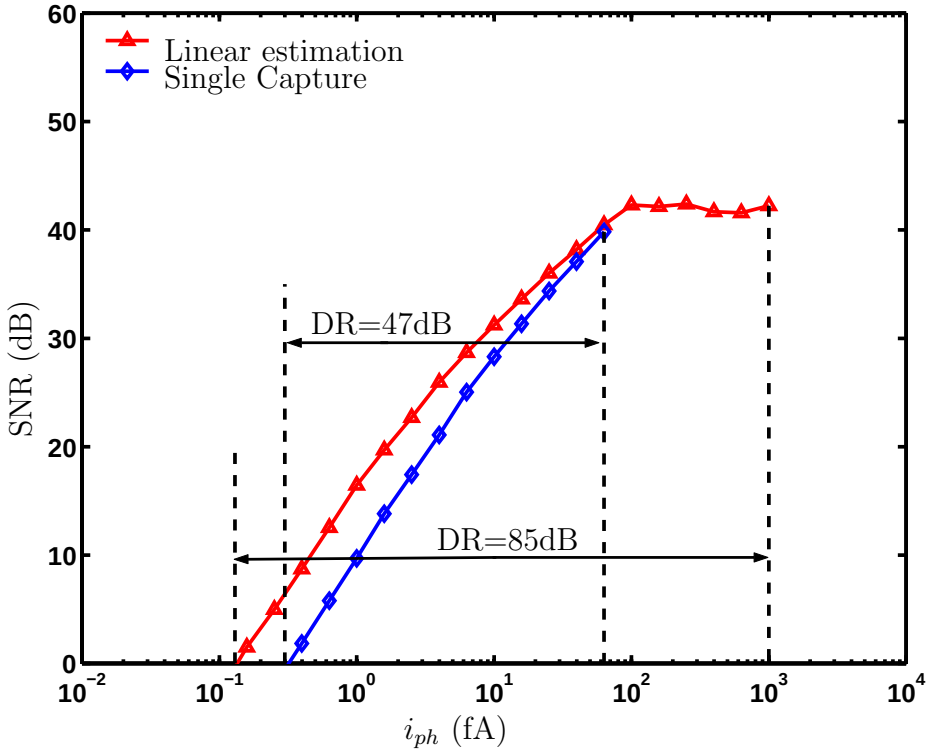


Figure 3.5: Estimation enhances the SNR and dynamic range

Figure 3.5 plots SNR versus i for conventional sensor operation, where the last sample $\tilde{I}_n$ is used, and using our estimation algorithm. Note that using our algorithm, SNR is consistently higher, due to the reduction in read noise. The improvement is

most pronounced at low light. In this example, sensor with single capture yields dynamic range of 47dB. Using our algorithm, dynamic range is extended to 85dB – increasing 30dB at the high illumination end and 8dB at the low illumination.

3.3 Summary

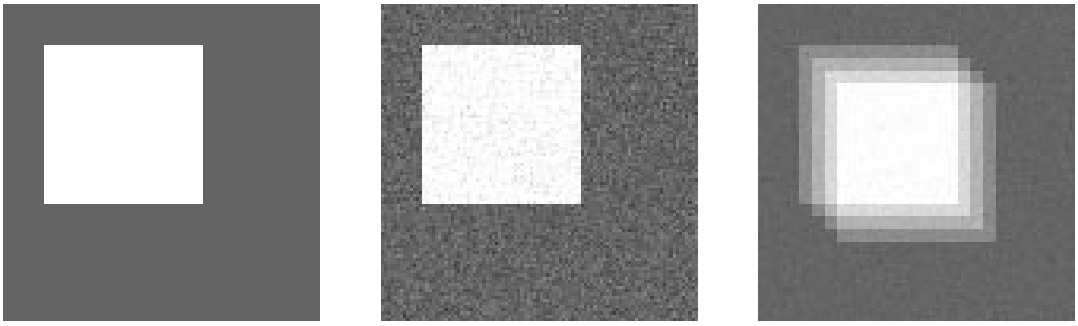
The estimation algorithms presented in this chapter exploit the high speed imaging capability of CMOS image sensors to enhance its dynamic range and SNR beyond the standard multiple capture scheme [80, 102]. While the standard multiple capture scheme extends dynamic range only at the high illumination end, our algorithms also extend it at the low illumination end by averaging out readout noise. The non-recursive estimation algorithm presented significantly increases dynamic range and SNR but requires the storage of all frames and performing costly matrix inversions. To reduce the storage and computational complexity we also derived a recursive algorithm. We showed that the dynamic range and SNR improvements achieved using the recursive estimator although not as impressive as using the non-recursive estimator, are quite significant. The recursive algorithm, however, has the important advantage of requiring the storage of only a few pixel values per pixel and modest computational power, which makes its implementation in a single chip digital imaging system quite feasible.

Chapter 4

Motion/Saturation Detection Algorithms

The derivation of the linear estimation algorithms in Chapter 3 assumed that $i(t)$ is constant and that saturation does not occur before $k\tau$. In this case, the longer the exposure time T, the higher the SNR and dynamic range will the image sensor achieve. However, due to the limited well capacity, the increase of exposure time T may lead to pixel saturation. Moreover, increasing the exposure time can result in potential motion blur. As an example, Figure 4.1 shows a bright square object moving diagonally across a dark background. If exposure time is set short, SNR deteriorates resulting in the noisy image. On the other hand, if exposure time is set long to achieve high SNR, it results in significant motion blur as shown. So, naturally, the question arises — what is the optimum exposure time?

In [80] and [102], the Last-Sample-Before-Saturation synthesis scheme was proposed, where the final image is reconstructed by using each pixel's last sample before saturation with appropriate scaling. Figure 4.2 shows an example of this scheme, where 6 images are captured at integration time 1ms, 2ms, 4ms, ..., 32ms. As integration time increases, the bright areas in the image saturate while the details in



Input Short exposure Long exposure

Figure 4.1: Examples of images captured with short and long exposure times. The scene consists of a bright square object moves diagonally across a dark background. Short exposure results in the noisy image while long exposure results in significant motion blur.

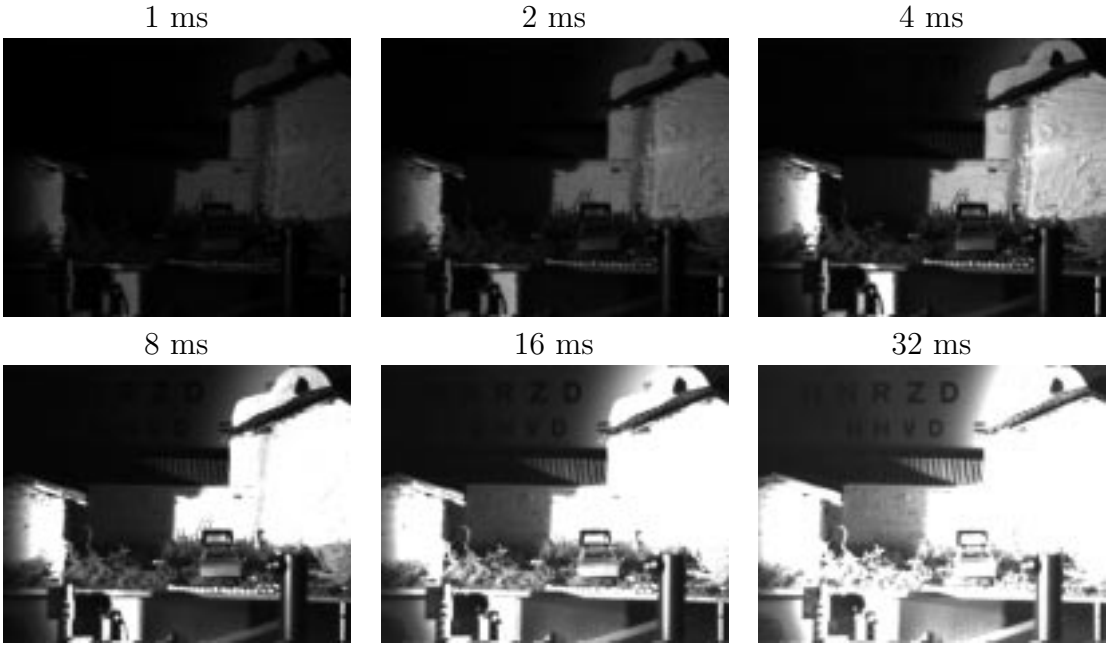


Figure 4.2: Example of multiple captures within one exposure time.

Figure 4.3: Example of high dynamic range image reconstructed using Last-Sample-Before-Saturation synthesis scheme.

the dark region gradually appear. Note that each region has its best representation in one of these captures, but no single image represents the whole scene well. Figure 4.3 shows the example of the reconstructed high dynamic range image from the above 6 multiple captures. Note that with the scheme, this final image has the best representation for all the regions in the scene.

However, as discussed in Chapter 3, this simple algorithm does not take full advantage of the multiple captures. The sensor dynamic range is only extended at the high illumination end, which in many applications is not enough. The sensor read noise is not reduced, therefore, for a given maximum exposure time T, dynamic range at low end is not improved. Moreover, this method can not detect the illumination condition change caused by motion, therefore it can not prevent motion blur.

In this chapter, we describe an algorithm for detecting change in the value of $i(t)$ due to motion or saturation before the new image is used to update the photocurrent

estimate. By performing the detection step prior to each estimation step we form a blur free high dynamic range image from the $n + 1$ captured images. We will also discuss the trade-off between motion induced distortion and SNR improvement by increasing the exposure time. Experimental results achieved by applying our algorithm to the prototype high speed DPS chip described in Chapter 2 will be presented at the end of this chapter.

4.1 Motion/Saturation Detection

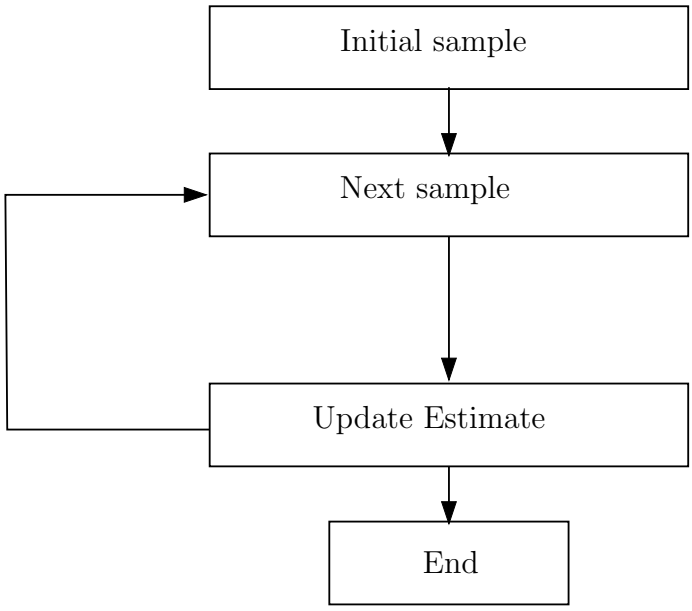


Figure 4.4: Recursive photocurrent estimation from multiple captures.

Recall the operation flow of our recursive photocurrent estimation algorithm (Figure 4.4) described in Chapter 3. It is clear that adding motion/saturation detection will prevent motion and saturation from corrupting the estimation process. This detection procedure also makes it possible to further extend exposure time and to capture more images, which can be used to further enhance dynamic range at the low illumination end. A high level flow chart of our algorithm is provided in Figure 4.5.

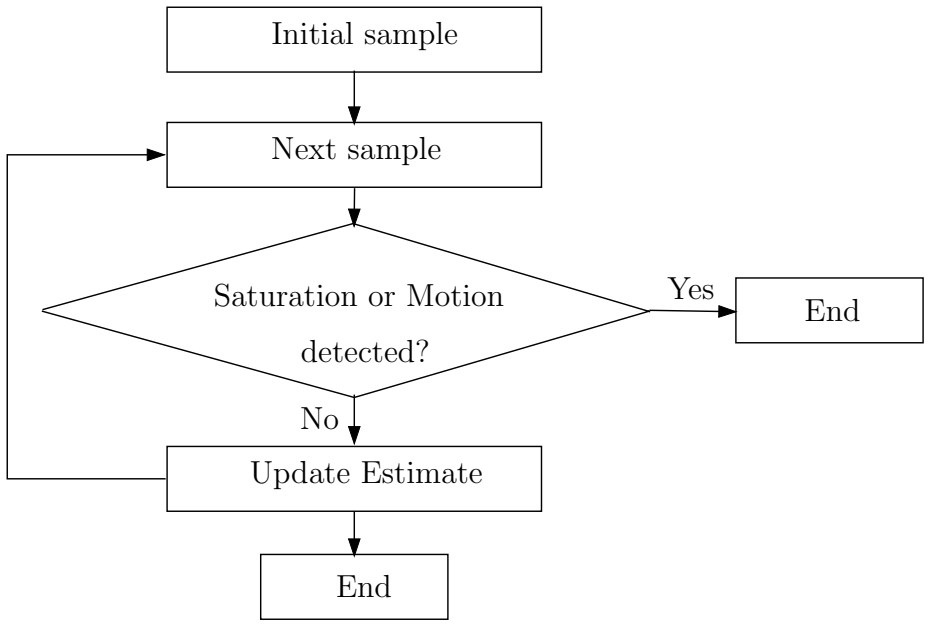


Figure 4.5: High dynamic range motion blur free synthesis from multiple captures.

The algorithm operates on n images [1] captured at times $\tau, 2\tau, \ldots, n\tau = T$ as follows:

1. Capture first image, set $k = 1$.
2. For each pixel: Use the *estimation algorithm* to find the photocurrent estimate $\hat{I}_1$ from $Q(\tau)$.
3. Capture next image.
4. For each pixel: Use the *motion detection algorithm* to check if motion/saturation has occurred

[1] Actually the algorithm operates on $n+1$ images, the first image, which is ignored here, is taken at $t = 0$ and is used to reduce reset noise and offset FPN as discussed in detail in Chapter 3.

(i) *Motion detected*: Set final photocurrent estimate

$$\hat{I}_n = \hat{I}_k.$$

(ii) *No Motion detected or decision deferred*: Use the *current estimation algorithm* to find $\hat{I}_{k+1}$ from $Q((k+1)\tau)$ and $\hat{I}_k$ and set $k = k+1$.

5. Repeat steps 3 and 4 until $k = n$.

From the flow chart as shown in Figure 4.5, it is clear that a recursive algorithm is desirable. Our algorithm is also a pixel-wise operation, *i.e.*, each pixel is processed separately. As a result, the algorithm requires small amount of memory that is independent of the number of captures and has very low computational complexity, which makes it well suited to camera-on-chip implementation.

Before we describe the details of motion/saturation detection, let's first further illustrate the operation of our algorithm on multiple pixel sampling using the examples in Figures 4.6. The first plot in Figure 4.6 represents the case of a constant low light. The second plot represents the case of a constant high light, where $Q(T) = Q_{\text{sat}}$, *i.e.*, the pixel saturate at the end of exposure. The third plot is for the case when light changes during exposure time, *e.g.*, due to motion.

For the examples in Figure 4.6, we capture four images at τ, 2τ, 3τ, and $T = 4\tau$. For the case that pixel is under constant low light, combining the four samples can help us get better estimation of the photocurrent than only using the last sample. As presented in Chapter 3, a weighted averaging of the multiple samples reduces the sensor readout noise and thus enhances the SNR and dynamic range at low illumination. For the case that the pixel is under constant high light, our saturation detection algorithm identifies the saturation at 3τ and photocurrent is estimated using the images captured at τ and 2τ only. For the case of motion, our motion detection algorithm detects motion at 2τ and therefore able to prevent motion blurring by only using the first sample. Applying the algorithm to the example in Figure 4.1, we get the image in Figure 4.7, which is almost blur free and less noisy.

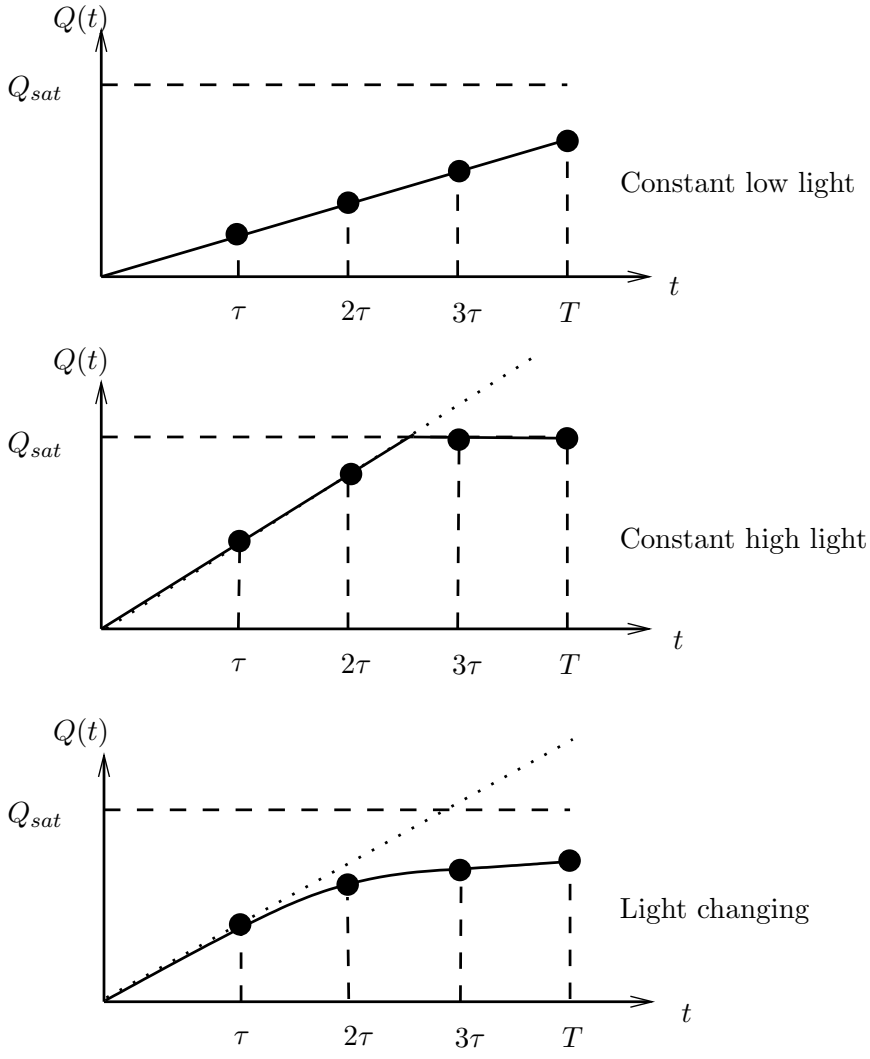


Figure 4.6: $Q(t)$ vs. t for three lighting conditions.

Figure 4.7: Image produced using our algorithm with the same scene as in Figure 4.1

4.1.1 Decision rules

The algorithm operates on each pixel separately. After the kth capture, the best MSE linear estimate of i, $\hat{I}_k$, and its MSE, Φ_k^2, are computed as detailed in Subsection 3.1.3. If the current stays constant, the next observation $\tilde{I}_{k+1}^{pre}$ would be

$$\tilde{I}_{k+1}^{pre} = i + \frac{\sum_{j=1}^{k+1} U_j}{(k+1)\tau} + \frac{V_{k+1} - wV_0}{(k+1)\tau} + \frac{(1-w)C}{(k+1)\tau}, \tag{4.1}$$

and the best predictor of $\tilde{I}_{k+1}^{pre}$ is $\hat{I}_k$ with the prediction MSE given by (see Appendix F)

$$\begin{aligned} \Delta_{pre}^2 &= E\left((\tilde{I}_{k+1}^{pre} - \hat{I}_k)^2 | \hat{I}_k\right) \\ &= (\tfrac{k}{k+1})^2 \Delta_k^2 + \Phi_k^2 - \tfrac{2k}{k+1}\Theta_k \\ &\quad + \tfrac{2h_k}{k(k+1)\tau^2}\sigma_V^2 + \tfrac{\sigma_U^2}{(k+1)^2\tau^2} \end{aligned} \tag{4.2}$$

where Δ_k^2, Θ_k, Φ_k^2, h_k are given in Equation 3.21, 3.22, 3.23, 3.24 respectively.

Thus to decide whether the input signal i changed between time $k\tau$ and $(k+1)\tau$, we compare $\tilde{I}_{k+1} = \frac{Q_{k+1} - wQ_0}{(k+1)\tau}$ with $\hat{I}_k$. A simple decision rule would be to declare that motion has occurred if

$$|\tilde{I}_{k+1} - \hat{I}_k| \geq m\Delta_{pre}, \tag{4.3}$$

and to use $\hat{I}_k$ as the final estimate of i, otherwise to use $\tilde{I}_{k+1}$ to update the estimate of i, *i.e.*, $\hat{I}_{k+1}$. The constant $m > 0$ is chosen to achieve the desired trade-off between SNR and motion blur. The higher m the more motion blur if i changes with time, but also the higher the SNR if i is a constant, and vice versa.

One potential problem with this "hard" decision rule is that gradual drift in i can cause accumulation of estimation error resulting in undesired motion blur. To address this problem we propose the following "soft" decision rule.

Motion detection algorithm: For each pixel, after the $(k+1)$st capture:

1. If $|\tilde{I}_{k+1} - \hat{I}_k| \leq m_1\Delta_{pre}$, then declare that *no motion detected*. Use $\tilde{I}_{k+1}$ to update $\hat{I}_{k+1}$ and set $L^+ = 0$, $L^- = 0$.

2. If $|\tilde{I}_{k+1} - \hat{I}_k| \geq m_2\Delta_{pre}$, $L^+ = l_{max}$, or $L^- = l_{max}$, then declare that *motion detected*. Use $\hat{I}_k$ as the final estimate of i.

3. If $m_1\Delta_{pre} < \tilde{I}_{k+1} - \hat{I}_k < m_2\Delta_{pre}$, then *defer the decision* and set $L^+ = L^+ + 1$, $L^- = 0$.

4. If $-m_2\Delta_{pre} < \tilde{I}_{k+1} - \hat{I}_k < -m_1\Delta_{pre}$, then *defer the decision* and set $L^- = L^- + 1$, $L^+ = 0$.

The counters L^+, L^- record the number of times the decision is deferred, and $0 < m_1 < m_2$ and l_{max} are chosen to trade-off SNR with motion blur.

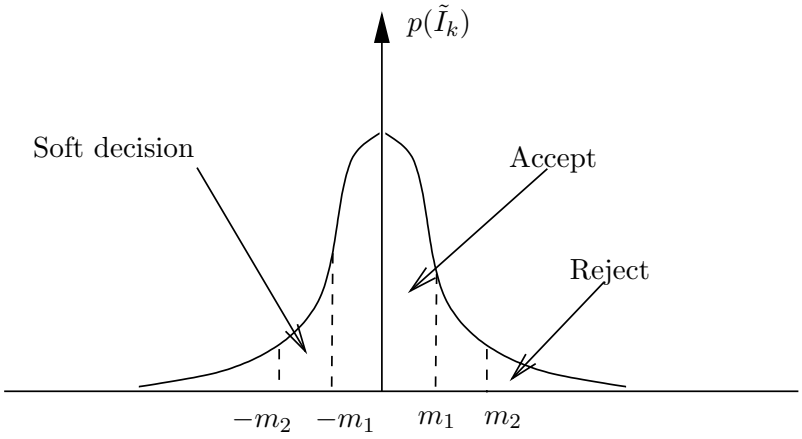


Figure 4.8: Soft-decision Motion Detection.

4.1.2 Trade-off between SNR and motion blur distortion

To illustrate the trade-off between SNR and motion blur distortion, we consider the case of a linearly varying photocurrent

$$i(t) = i_0(1 + \rho t). \tag{4.4}$$

Here $i_0 = i(0)$ is the photocurrent at the beginning of exposure, $0 \leq t \leq T$ is time during exposure, and $\rho \geq -1/T$ is the rate of photocurrent change.

To simplify the analysis we assume that photocurrent is estimated by the most recent sample $\tilde{I}_k$. In this case we can express the MSE as the sum of two components

$$\text{MSE} = \Delta_1^2 + \Delta_2^2, \tag{4.5}$$

where

$$\Delta_1^2 = (\frac{1}{2}\rho i_0 t)^2, \tag{4.6}$$

is the MSE due to motion distortion and

$$\Delta_2^2 = \frac{\sigma_V^2}{t^2} + \frac{qi_0}{t} + \frac{1}{2}q\rho i_0, \tag{4.7}$$

is the estimation MSE. Note that Δ_1^2 increases with time, since the deviation from constant current due to motion increases with t, while Δ_2^2 decreases with time, since estimation becomes more accurate as t increases (see Figure 4.9). The parameters m_1, m_2, L^-, L^+ in our motion detection algorithm can be set to achieve the desired trade-off between SNR and motion blur distortion.

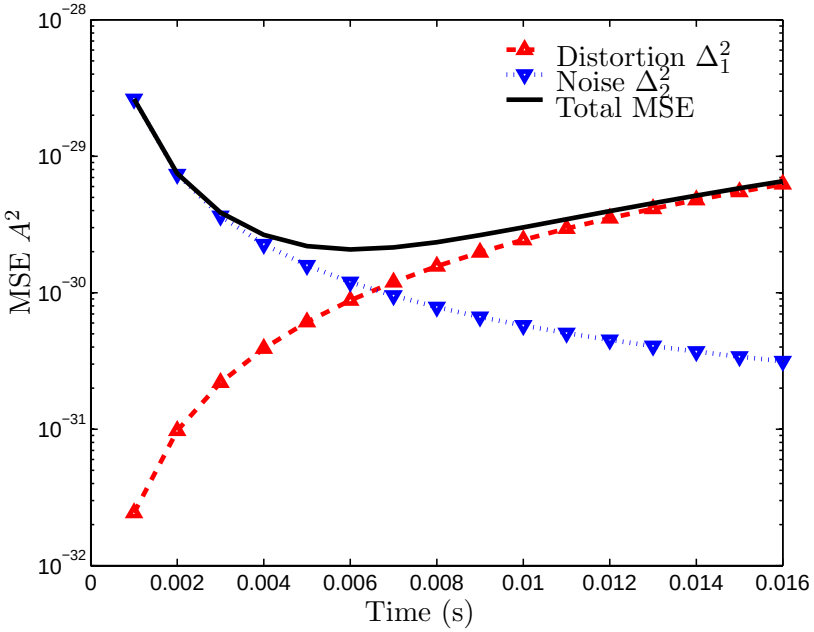


Figure 4.9: Optimal integration time under motion.

4.2 Experimental results

To verify the algorithms described in this chapter and Chapter 3, we designed and prototyped an experimental PC-based high speed CMOS imaging system around the

10,000 frames/s CMOS Digital Pixel Sensor (DPS) chip described in Chapter 2.

4.2.1 Experimental High Speed CMOS Image Sensor System

The experimental system comprises a PCB interfaced to a PC via three 20MHz 32-bit National Instrument I/O cards supported by an easy to use software environment. We decided to use three I/O cards instead of one or two higher speed ones for simplicity, robustness and maximum interface flexibility of the design, while achieving high enough frame rate for the intended applications. The PCB we designed houses the DPS chip and provides the analog and digital signals needed to operate it and interface it's 64-bit wide output bus to the I/O cards. Front end optics is provided by attaching a metal box with a standard C-mount lens to the PCB. The system is fully software programmable through a Matlab interface. It is capable of continuous image acquisition at rates of up to 1,300 frames/s, which, although slower than the maximum frame rate of the chip, is high enough for the intended applications.

4.2.2 Image Synthesis from Multiple Captures

The high dynamic range scene used in the experiment comprised a doll house under direct illumination from above and a rotating model airplane propeller. We captured 65 frames of the scene at 1,000 frames/s non-destructively and uniformly spaced over a 64ms exposure time. Figure 4.10 shows some of the images captured. Note that as exposure time increases, the details in the shadow area (such as the word "Stanford") begin to appear while the high illumination area suffers from saturation and the area where the propeller is rotating suffers from significant motion blur.

We first applied the Last Sample Before Saturation algorithm [102] to the 65 images to obtain the high dynamic range image in Figure 4.11. While the image indeed contains many of the details in the low and illumination areas, it suffers from motion blur and is quite noisy in the dark areas. Figure 4.12 shows the high dynamic range, motion blur free image synthesized from the 65 captures using the algorithm discussed in this paper. Note that the dark background is much smoother due to

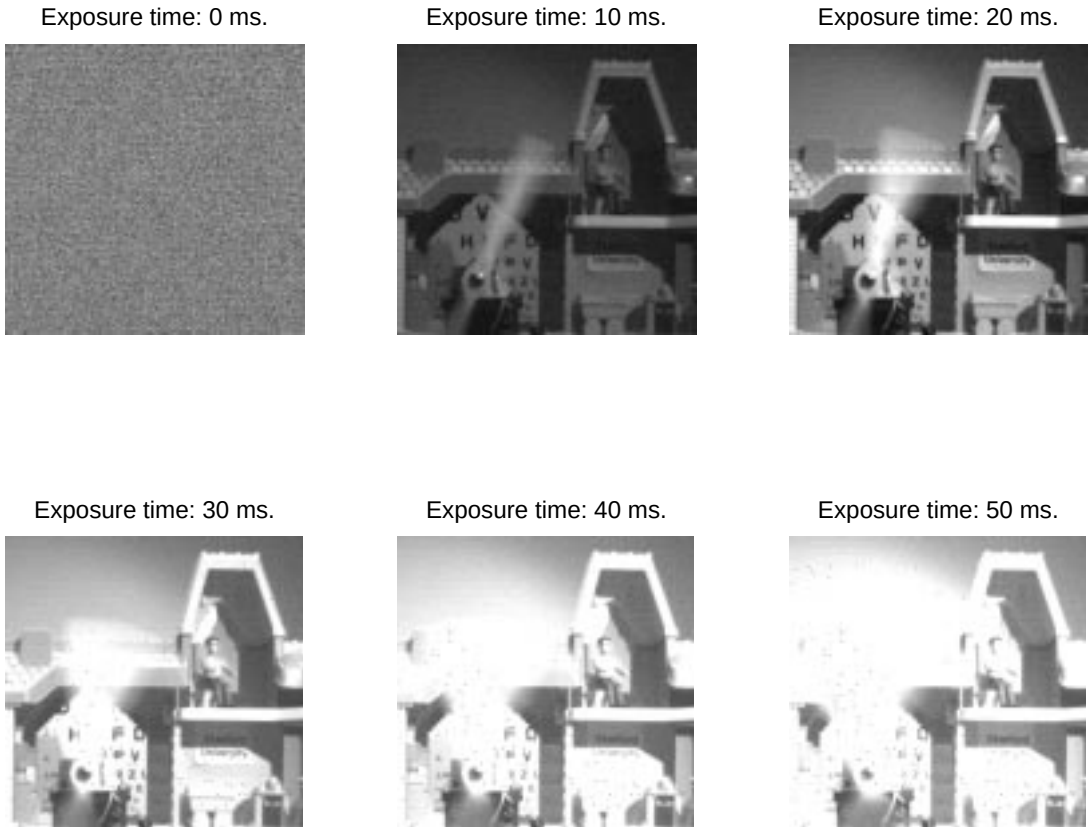


Figure 4.10: Six of the 65 images of the high dynamic scene captured non-destructively at 1,000 frames/s.

reduction in readout and FPN, and the motion blur caused by the rotating propeller in Figure 4.11 is almost completely eliminated.

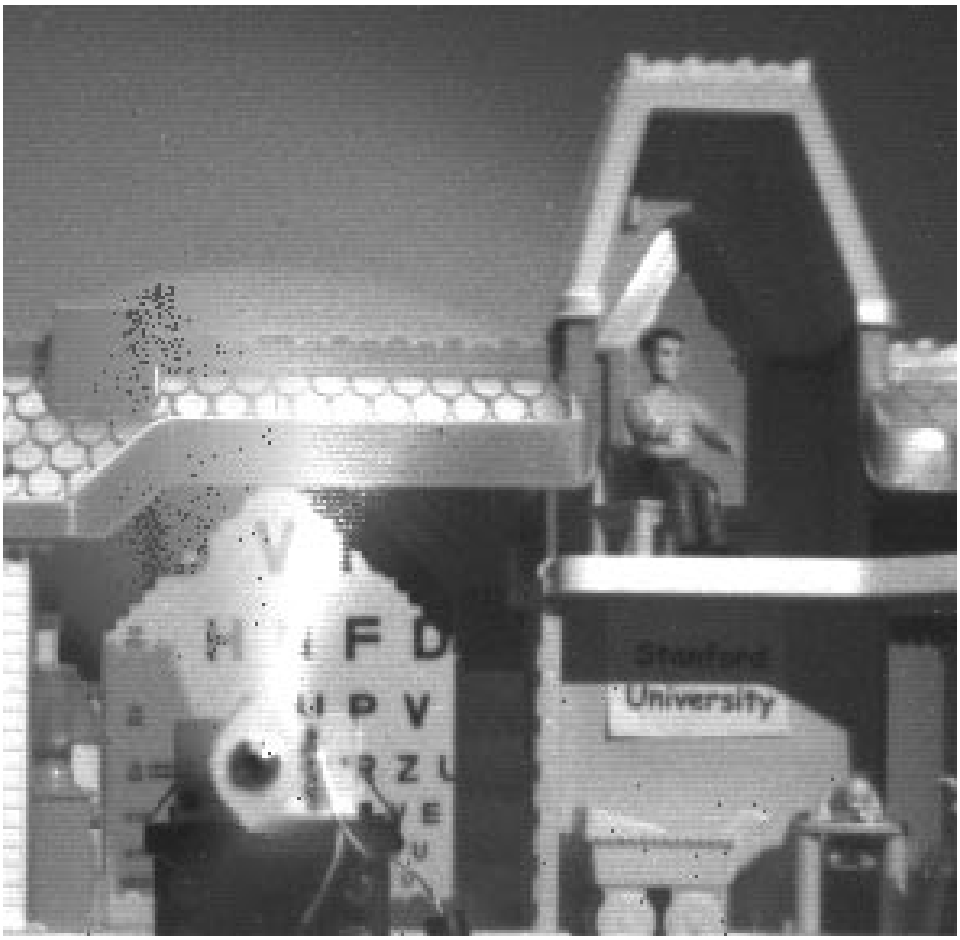


Figure 4.11: High dynamic range image synthesized using the Last Sample Before Saturation algorithm.

To illustrate the operation of our algorithm, in Figure 4.13 we plot the sampled and estimated photocurrents for three pixels under different illumination levels. Note how motion blur is prevented in the third pixel using the motion detection algorithm. In Figure 4.14, we plot the "adapted" exposure time for each pixel in the final image. It clearly demonstrated the effectiveness of our motion/saturation detection algorithm.

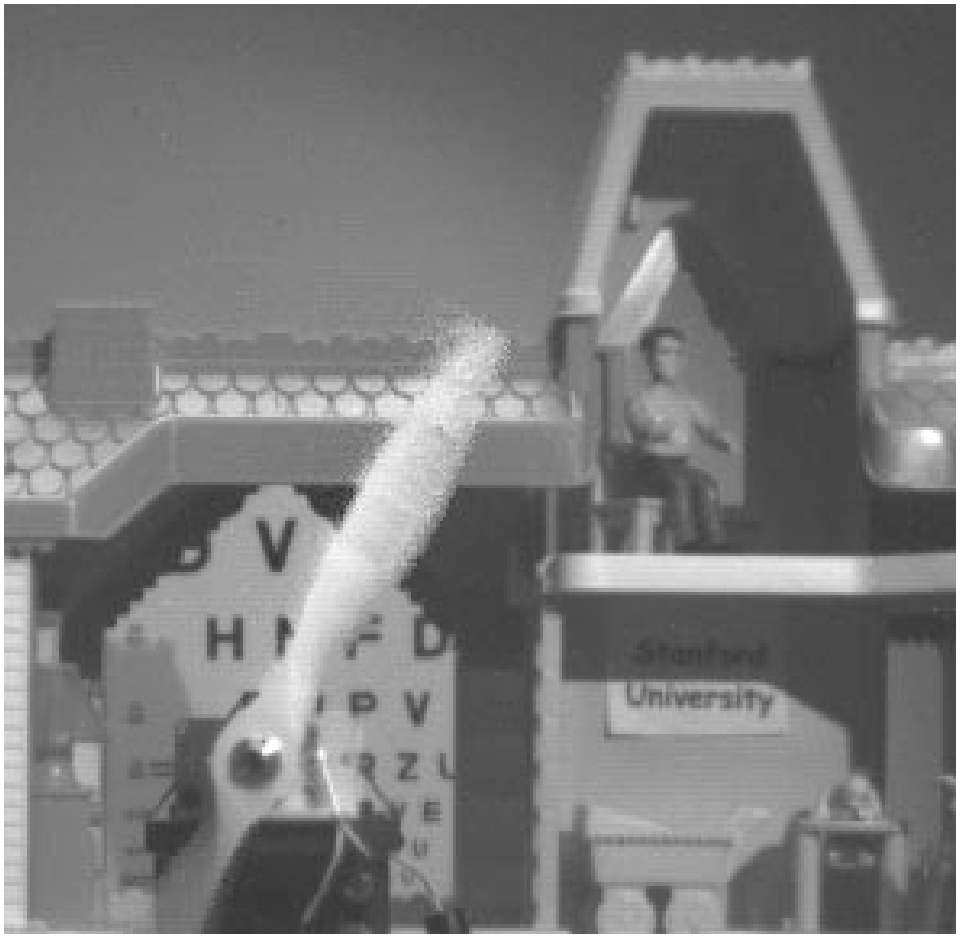


Figure 4.12: The high dynamic range, motion blur free image synthesized from the 65 images.

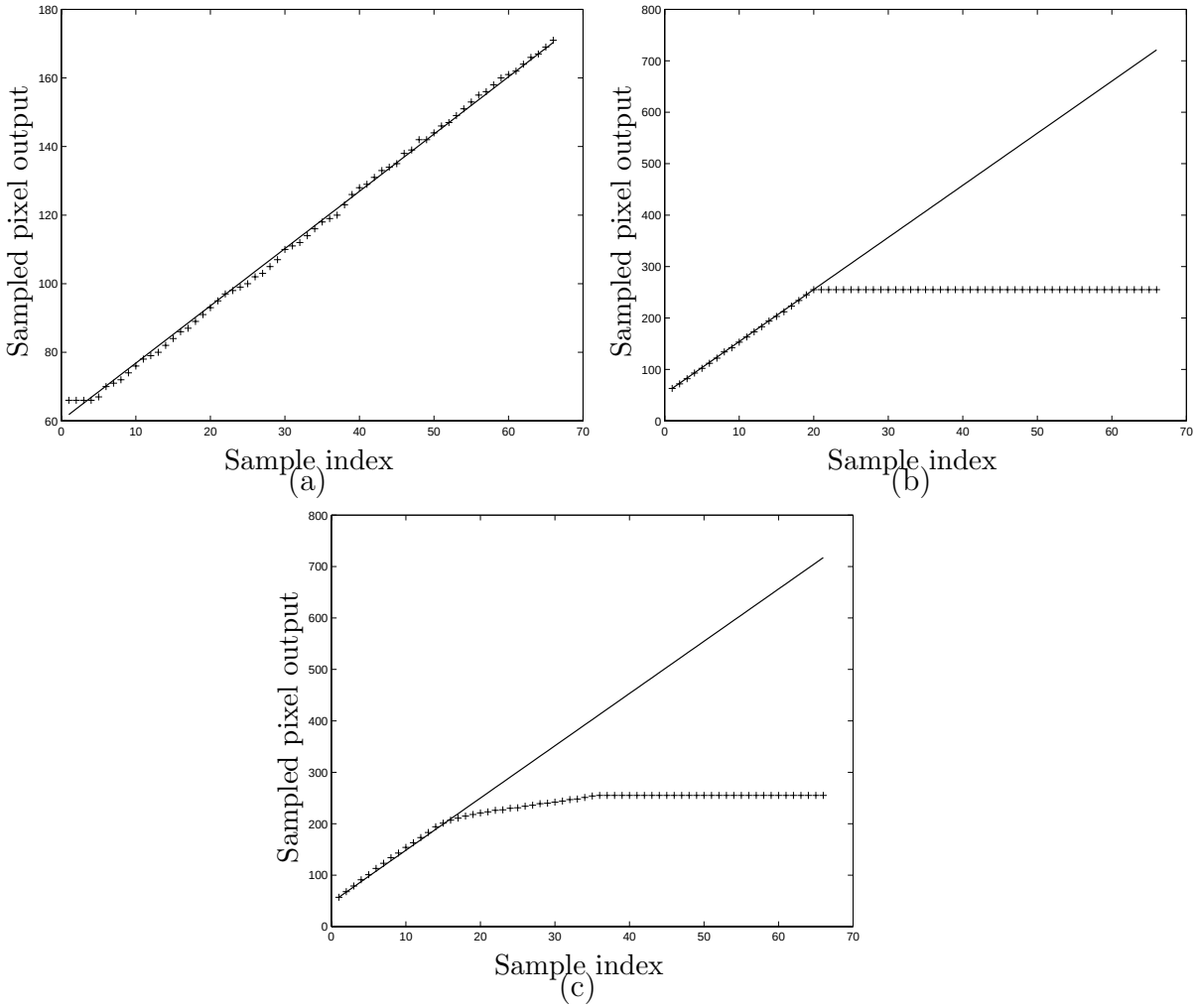


Figure 4.13: Readout values (marked by '+' and estimated values (solid lines) for (a) pixel in the dark area, (b) pixel in bright area, and (c) pixel with varying illumination due to motion.

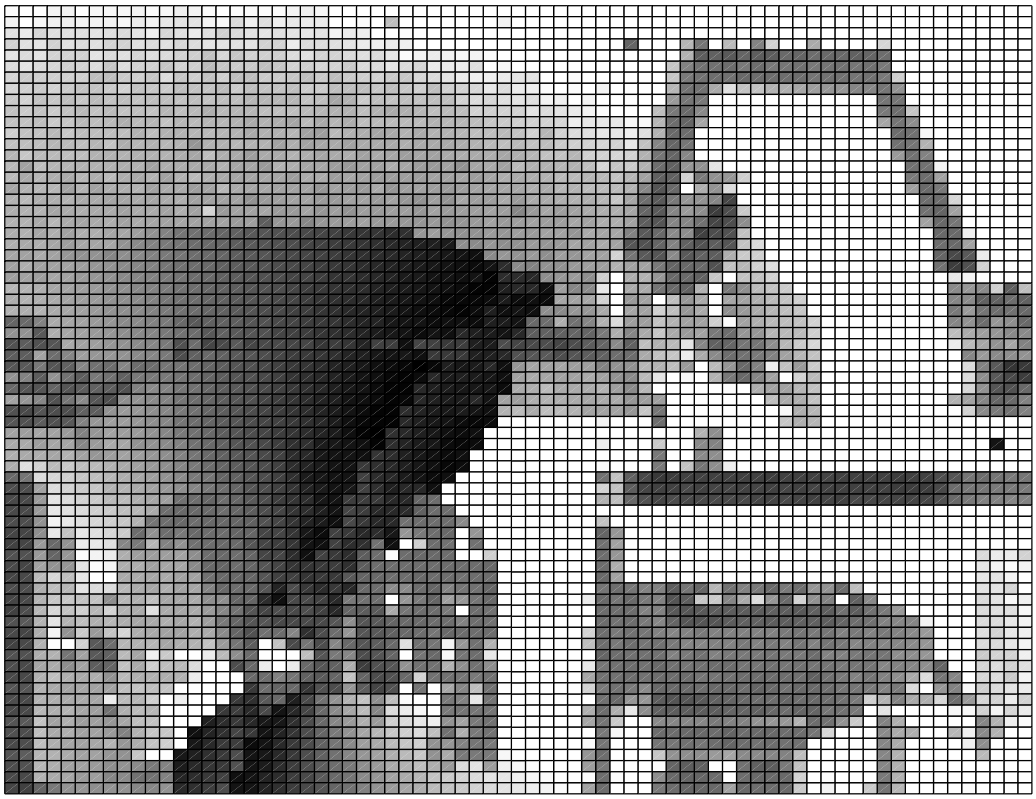


Figure 4.14: The "adapted" exposure time for each pixel in the final image, where the level of shade represents time (darker means shorter time).

4.3 Summary

In this chapter, we first presented the motion/saturation detection algorithm that is an integral part of our high dynamic range motion blur free image synthesis method. We presented two decision rules — "hard" decision and "soft" decision. "Soft" decision rule effectively prevents the accumulation of estimation error due to slow motion and also provides the freedom in achieving the desired trade-off between SNR and motion blur distortion.

We then described our high speed imaging system using the $10,000$ frames/s DPS test chip described in Chapter 2. By applying our method to a 65-frame sequence captured using this system, we are able to get the final high dynamic range, motion blur free image that clearly demonstrates the success of the algorithm.

Chapter 5

A Self-Reset Digital Pixel Sensor

With the need to reduce pixel size and integrate more functionality with the sensor, CMOS image sensors need to follow the CMOS technology scaling trend. Well capacity, however, decreases with technology scaling as pixel size and supply voltages are reduced. As a result, SNR decreases potentially to the point where even peak SNR is inadequate. In this chapter, we propose a self-reset pixel architecture, which when combined with multiple non-destructive captures can increase peak SNR as well as enhance dynamic range. Under high illumination, self-resetting "recycles" the well during integration resulting in higher effective well capacity, and thus higher SNR. A recursive photocurrent estimation algorithm that takes into consideration the additional noise due to self-resetting is described. Simulation results demonstrate the SNR increase throughout the enhanced photocurrent range with 10dB increase in peak SNR using 32 captures.

5.1 Introduction

With the need to reduce pixel size and integrate more functionality with the sensor, CMOS image sensors continue to follow the CMOS technology scaling trend [19].

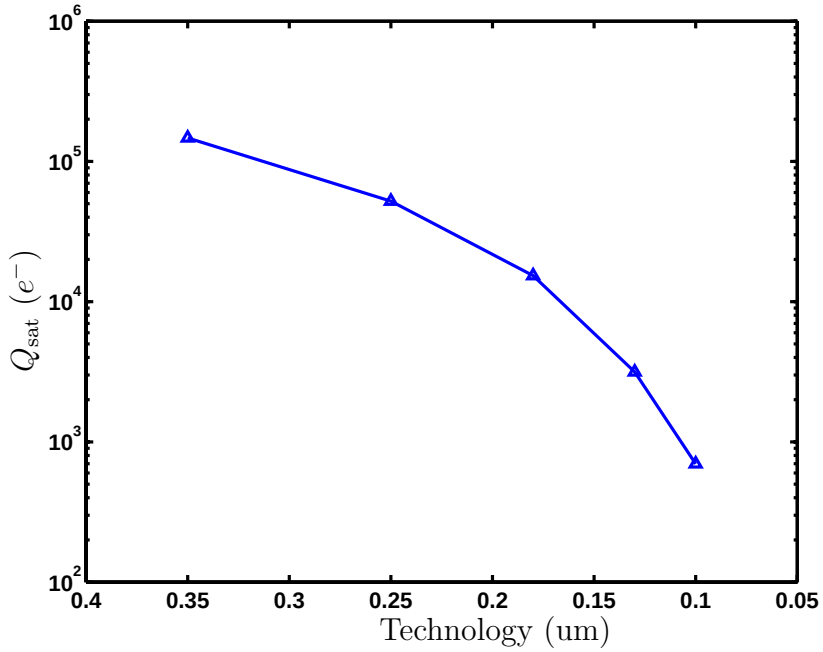


Figure 5.1: Projected pixel well capacity as a function of technology scaling

Well capacity, however, decreases with technology scaling. For a sensor operating in direct integration, well capacity can be expressed as

$$Q_{\text{sat}} = V_{\text{swing}} \times C_{\text{sense}}. \tag{5.1}$$

where V_{swing} is the voltage swing and C_{sense} is the integration capacitance. Both V_{swing} and C_{sense} decrease as technology scales. Adopting the principal device technology and electrical characteristics from the widely accepted SIA roadmap [19], and assuming no special transistors and major process modification are used in the sensor fabrication, we project the well capacity at each technology generation as shown in Figure 5.1.

The sensor dynamic range and peak SNR are directly proportional to its well capacity. The peak SNR can be expressed as

$$SNR_{peak} = \frac{(Q_{sat} - i_{dc}T)^2}{qQ_{sat} + \sigma_V^2 + \sigma_C^2} \approx \frac{Q_{sat}}{q}, \tag{5.2}$$

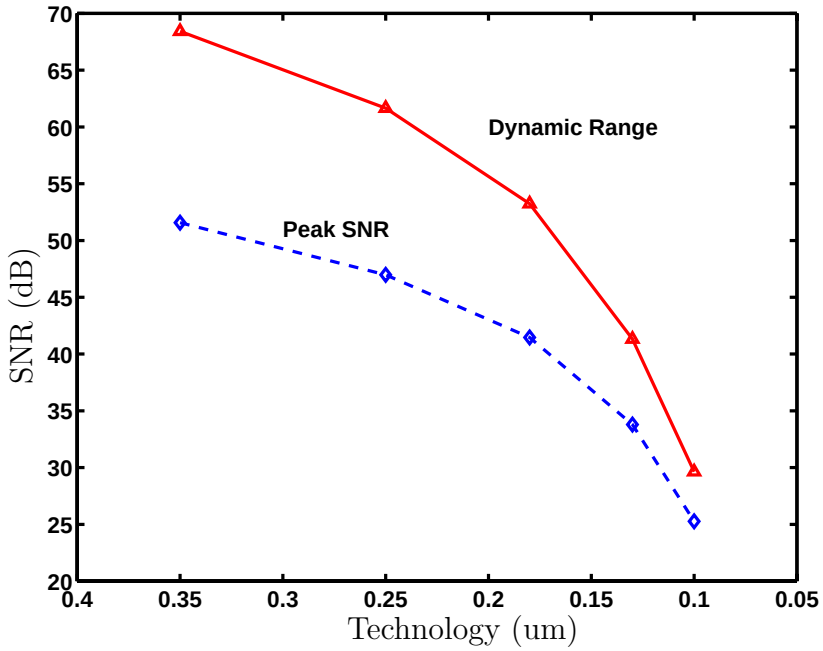


Figure 5.2: Projected peak SNR and dynamic range as a function of technology scaling

where i_{dc} is the dark current, and σ_V^2 is the read noise and σ_C^2 is the reset noise. The approximation is valid when the shot noise term in the denominator is much larger than the read and reset noise terms, which is the case under high illumination. Figure 5.2 plots both the projected pixel dynamic range and peak SNR as a function technology scaling. Notice that at 0.13μm technology, the projected peak SNR is less than 30dB, which is inadequate.

In this chapter, we propose a method for extending sensor peak SNR by combining a self-reset pixel architecture with multiple non-destructive image captures. Under high illumination, self resetting "recycles" the well during integration resulting in higher effective well capacity, and thus higher SNR. We extend the photocurrent estimation algorithm in Chapter 3 to take into consideration the additional noise due to self-resetting.

The rest of the chapter is organized as follows. In section 5.2 we describe the proposed self-reset pixel architecture. In section 5.3 we formulate the photocurrent

estimation problem for the self-reset pixel architecture and present a recursive estimation algorithm. Finally, we present simulation results that demonstrate the dynamic range and SNR improvements using our algorithm.

5.2 Self-reset Digital Pixel Sensor

The motivation for proposing the self-reset pixel architecture is to be able to increase the well capacity by reusing the small physical well several times during integration. Assuming a maximum of m self-resets, the well capacity becomes

$$Q_{\text{total}} = m \times Q_{\text{sat}}, \tag{5.3}$$

resulting in peak SNR of

$$\text{SNR}_{\text{peak}} \approx \frac{mQ_{\text{sat}}}{q}, \tag{5.4}$$

an m-fold increase in peak SNR.

The proposed self-reset pixel architecture is based on our latest Digital Pixel Sensor (DPS) design as described in Chapter 2. As shown in Figure 5.3, each pixel contains a photodiode, a comparator, a feedback loop and 8-bit memory. The design of the comparator and the memory has been described in Chapter 2. The feedback loop consisting of transistors M1, M2, and M3 performs the self-reset function. The circuit has two modes of operation: multiple pixel sampling by means of A/D conversion and saturation monitoring. As shown in Figure 5.4, the operation alternates between these two modes during exposure.

During A/D conversion, which we assume to be performed at regular time interval, the V_{enable} signal is set low, and the feedback loop is off. Single-slope A/D conversion is performed by ramping V_{ref} from V_{max} to V_{min} and digitally ramping *Bitline* from 0 to 255. The digital ramp is assumed to be generated by an on-chip counter and globally distributed to all pixels. The 8-bit memory cell latches the digital count corresponding to V_{in}'s value. The memory readout is performed during the following

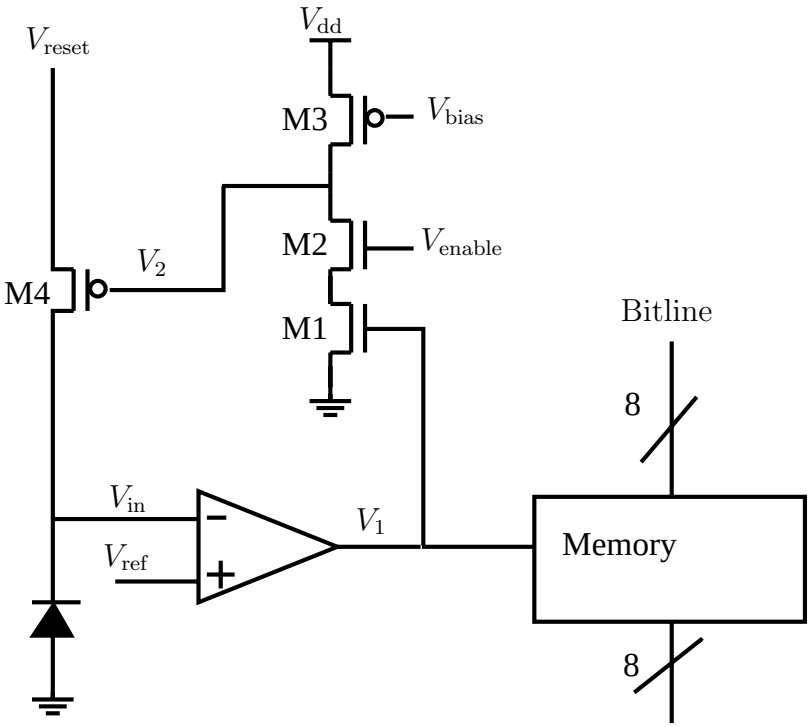


Figure 5.3: Self-reset Digital Pixel Sensor circuit.

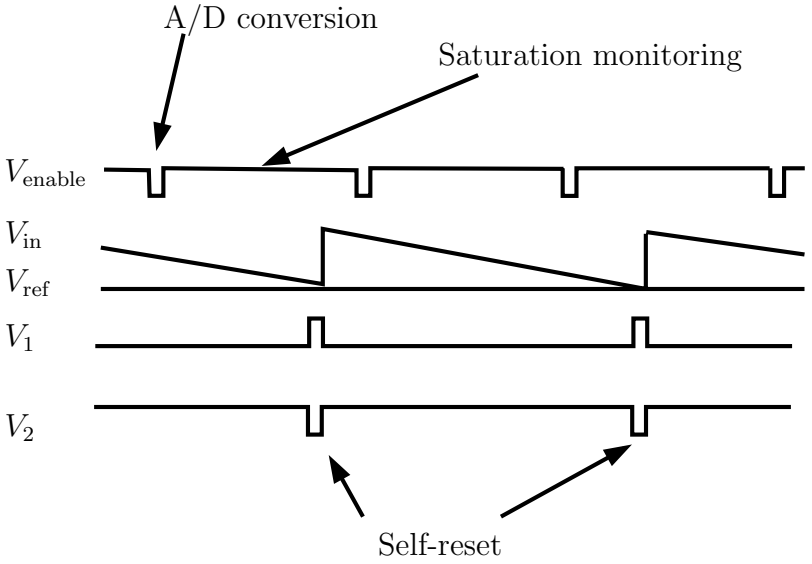


Figure 5.4: Self-reset Digital Pixel Sensor timing diagram.

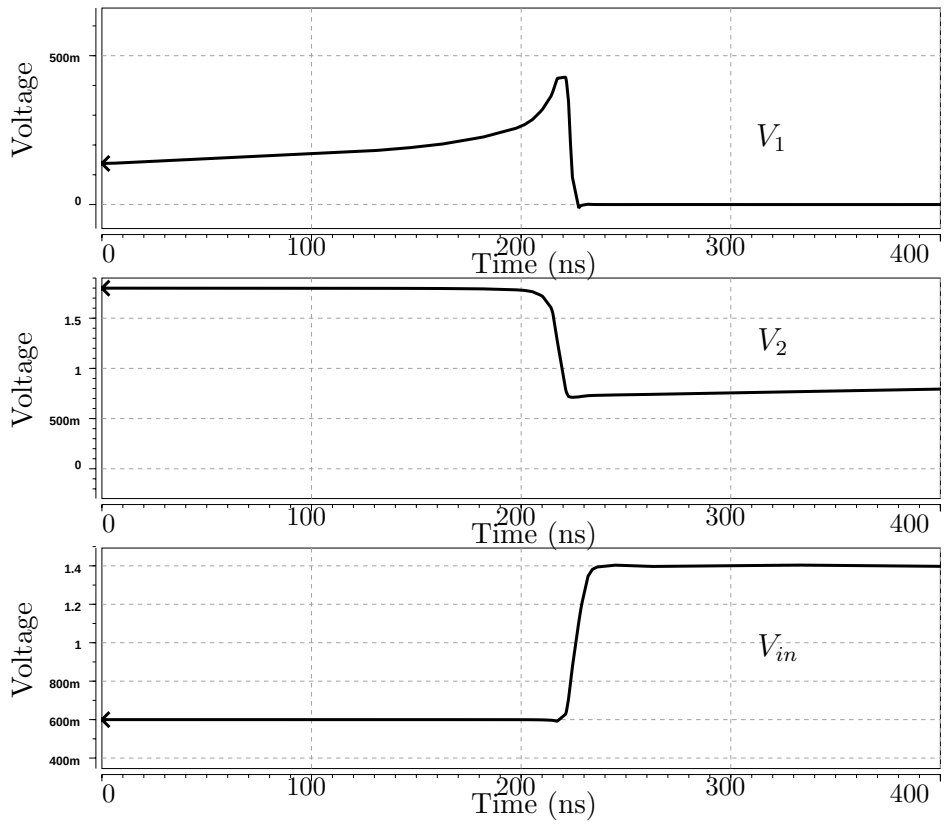


Figure 5.5: HSPICE wave forms of V_1, V_2 and V_{in} during self resetting for the pixel circuit implemented in a standard 0.18μm CMOS technology. The diode voltage V_{in} is reset from 0.6V to 1.4V in less than 90ns.

saturation monitoring mode.

During saturation monitoring, V_{enable} is high and V_{ref} is set at V_{min}. Light induced photocurrent discharges the diode capacitance and V_{in} continuously decrease till it reaches V_{min}, which causes the comparator to flip and its output V_1 to go high. This consequently turns on transistor M1 and V_2 goes low, which turns on M4 and resets the diode to V_{max}. After reset, V_1 becomes low again and M1 turns off. The very weakly biased transistor M3 gradually pulls up V_2 and finishes the self-reset.

Figure 5.5 shows HSPICE wave forms during self-resetting for the pixel circuit implemented in a standard 0.18μm CMOS technology using a comparator with gain

bandwidth of 2.9GHz. Since self-resetting occurs asynchronously with A/D conversion, it may be interrupted by the A/D conversion before it is completed. Note that in our simulations the self-reset circuit loop delay is around 90ns and the ADC time is around 25μs. So, as long as the saturation monitoring period is much longer than 25μs, the probability of incomplete self-reset is quite low.

Note that self-resetting can be detected for a pixel provided that its photocurrent is constant during exposure time and the readout sampling rate is fast enough so that at least one sample is read out between every two consecutive self-resets. The multiple capture sampling rate, thus, sets an upper bound on the maximum detectable photocurrent.

5.3 Photocurrent estimation algorithm

In Chapter 3, we described a linear MSE estimation algorithm for estimating photocurrent from multiple pixel samples. In this section we modify the signal and noise model used in Chapter 3 and use it to derive a recursive estimation algorithm suited to the self-reset architecture.

Figure 5.6 provides an example of the integrated photocharge as a function of time for the self-reset pixel where self-resetting happens twice during integration time $[0, T_{int}]$. The image capture times, marked by the dashed lines, are uniformly spaced at time $t = 0, \tau, 2\tau, \ldots,$ and T_{int}.

With the proposed self-reset scheme, reset noise and Fixed Pattern Noise (FPN) accumulate as self-resetting occurs. Assuming $n+1$ captures at times $0, \tau, \ldots, T_{\text{int}}$, we denote the pixel charge sample at time $k\tau$ and after m self-resets by $Q_{k,m}$.

With the accumulated reset noise and FPN components taken into consideration, $Q_{k,m}$ is given by:

$$\begin{aligned} Q_{0,0} &= V_0 + G_0 + F, \text{ the initial sample,} \\ Q_{k,m} &= ik\tau + \sum_{j=1}^{k} U_j + V_k + \sum_{j=0}^{m} G_j + (m+1)F, \end{aligned}$$

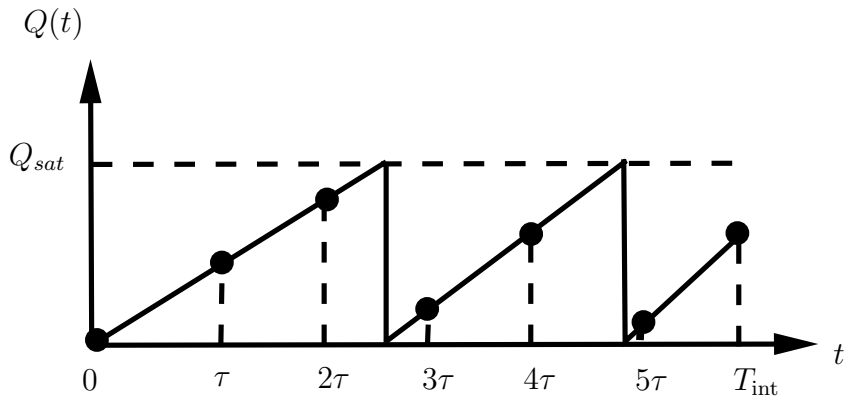


Figure 5.6: Photocharge as a function of time for the self-reset pixel where self-resetting happens twice during integration time $[0, T_{int}]$.

$$0 < k \leq n,\ 0 \leq m < k-1,$$

where V_k is the readout noise of the kth sample, U_j is the shot noise generated during the time interval $((j-1)\tau, j\tau]$, G_j is the reset noise generated during the jth self-reset , and F is the offset FPN. The U_j, V_k, G_j, F are independent zero mean random variables with

$$E(V_k^2) = \sigma_V^2 > 0, \text{ for } 0 \leq k \leq n,$$

$$E(U_j^2) = \sigma_U^2 = qi\tau, \text{ for } 1 \leq j \leq k, \text{ and}$$

$$E(G_j^2) = \sigma_G^2 > 0, \text{ for } 0 \leq j \leq m.$$

We also assume that $F >> G_j$, *i.e.*, that FPN is much larger than reset noise, and thus performing CDS is close to optimal, and define the photocurrent sample $\tilde{I}_k$ at time $k\tau$ as:

$$\begin{aligned}
\tilde{I}_{k,m} &= \frac{Q_{k,m} - (m+1)Q_{0,0}}{k\tau} \\
&= \frac{(ik\tau + \sum_{j=1}^{k} U_j + V_k + \sum_{j=0}^{m} G_j + (m+1)F) - (m+1)(V_0 + G_0 + F)}{k\tau} \\
&= i + \frac{1}{k\tau}\sum_{j=1}^{k} U_j + \frac{1}{k\tau}(V_k - (m+1)V_0) + \frac{1}{k\tau}(\sum_{j=1}^{m} G_j - mG_0), \text{ for } 1 \le k \le n.
\end{aligned}$$

The photocurrent linear estimation problem can be formulated as follows:

Find the best unbiased linear mean square estimate of the parameter i given $\{\tilde{I}_{1,0}, \tilde{I}_{2,0}, \ldots, \tilde{I}_{n,m}\}$, i.e., *coefficients $a_1, a_2, \ldots, a_n$ such that*

$$\hat{I}_n = \sum_{j=1}^{n} a_j \tilde{I}_{j,m},$$

minimizes

$$\Phi_n^2 = E(\hat{I}_n - i)^2,$$

subject to

$$E(\hat{I}_n) = i.$$

In order to reduce the computational complexity and memory requirements of the estimation algorithm, we restrict ourselves to recursive estimates, *i.e.*, estimates that can be recursively updated after each sample. So the problem can be reformulated as:

At time $k\tau$, find

$$\hat{I}_k = \hat{I}_{k-1} + a_k(\tilde{I}_{k,m} - \hat{I}_{k-1}),\ for\ 2 \leq k \leq n,$$

minimizes

$$\Phi_k^2 = E(\hat{I}_k - i)^2,$$

subject to

$$E(\hat{I}_k) = i.$$

The coefficient a_k can be found by solving the equations

$$\begin{aligned} \frac{d\,\Phi_k^2}{d\,a_k} &= \frac{d\,E(\hat{I}_k - i)^2}{d\,a_k} = 0, \text{ and} \\ E(\hat{I}_k) &= i. \end{aligned}$$

Define the MSE of $\tilde{I}_{k,m}$ as

$$\begin{aligned} \Delta_k^2 &= E(\tilde{I}_{k,m} - i)^2 \\ &= \frac{1}{k^2\tau^2}(k\sigma_U^2 + (m^2 + 2m + 2)\sigma_V^2 + (m^2 + m)\sigma_G^2), \end{aligned}$$

and the covariance between $\tilde{I}_{k,m}$ and $\hat{I}_k$ as

$$\begin{aligned}\Theta_k &= E(\tilde{I}_{k,m} - i)(\hat{I}_k - i) \\ &= (1 - a_k)E(\tilde{I}_{k,m} - i)(\hat{I}_{k-1} - i) + a_k\Delta_k^2.\end{aligned}$$

To derive the expression for Θ_k, we need to consider whether self-resetting has occurred before the current sample, *i.e.*, to represent $\tilde{I}_{k,m}$ using $\tilde{I}_{k-1,m}$ or $\tilde{I}_{k-1,m-1}$.

Thus we have:

$$\Theta_k = \begin{cases} (1 - a_k)\frac{k-1}{k}\Theta_{k-1} - \frac{(1-a_k)a_{k-1}}{k(k-1)\tau^2}\sigma_V^2 + a_k\Delta_k^2, \\ \text{for } m \text{ self-resets} \\ \\ (1 - a_k)\frac{k-1}{k}\Theta_{k-1} - \frac{(1-a_k)(m+a_{k-1})}{k(k-1)\tau^2}\sigma_V^2 + \frac{(1-a_k)(m-1)}{k(k-1)\tau^2}\sigma_G^2 + a_k\Delta_k^2, \\ \text{for } m-1 \text{ self-resets.} \end{cases}$$

The MSE of $\hat{I}_k$ can be expressed in terms of Δ_k^2 and Θ_k as

$$\Phi_k^2 = (1 - a_k)^2\Phi_{k-1}^2 + {a_k}^2\Delta_k^2 + 2(1 - a_k)a_k\Psi_k,$$

where

$$\begin{aligned}\Psi_k &= E(\hat{I}_{k-1} - i)(\tilde{I}_{k,m} - i) \\ &= \begin{cases} \frac{(k-1)}{k}\Theta_{k-1} - \frac{a_{k-1}}{k(k-1)\tau^2}\sigma_V^2 \\ \text{for } m \text{ self-resets} \\ \\ \frac{(k-1)}{k}\Theta_{k-1} - \frac{(m+a_{k-1})}{k(k-1)\tau^2}\sigma_V^2 - \frac{(m-1)}{k(k-1)\tau^2}\sigma_G^2 \\ \text{for } m-1 \text{ self-resets.} \end{cases}\end{aligned}$$

To minimize the MSE, we require that

$$\frac{d\,\Phi_k^2}{d\,a_k} = 0,$$

which gives

$$a_k = \frac{\Phi_{k-1}^2 - \Psi_k}{\Phi_{k-1}^2 + \Delta_k^2 - 2\Psi_k}.$$

Note that a_k, Θ_k and Ψ_k can all be recursively updated.

To summarize, the recursive algorithm is as follows.

- Compute initial parameter values:

$$\begin{aligned} a_1 &= 1, \\ \tilde{I}_{1,0} &= \frac{(Q_1 - Q_0)}{\tau}, \\ \hat{I}_1 &= \tilde{I}_1, \\ \Delta_1^2 &= \frac{\sigma_U^2 + 2\sigma_V^2}{\tau^2}, \\ \Phi_1^2 &= \Delta_1^2, \\ \Theta_1 &= \Delta_1^2. \end{aligned}$$

- At each iteration, update the parameter values:

$$\tilde{I}_{k,m} = \frac{Q_{k,m} - (m+1)Q_{0,0}}{k\tau},$$

$$\Delta_k^2 = \frac{1}{k^2\tau^2}(k\sigma_U^2 + (m^2+2m+2)\sigma_V^2 + (m^2+m)\sigma_G^2),$$

$$\Psi_k = \begin{cases} \frac{(k-1)}{k}\Theta_{k-1} - \frac{a_{k-1}}{k(k-1)\tau^2}\sigma_V^2 & \text{for} \quad m \text{ self-resets} \\ \frac{(k-1)}{k}\Theta_{k-1} - \frac{(m+a_{k-1})}{k(k-1)\tau^2}\sigma_V^2 - \frac{(m-1)}{k(k-1)\tau^2}\sigma_G^2 & \text{for} \quad m-1 \text{ self-resets} \end{cases}$$

$$
\begin{aligned}
a_k &= \frac{\Phi_{k-1}^2 - \Psi_k}{\Phi_{k-1}^2 + \Delta_k^2 - 2\Psi_k}, \\
\Theta_k &= \begin{cases} (1-a_k)\frac{k-1}{k}\Theta_{k-1} - \frac{(1-a_k)a_{k-1}}{k(k-1)\tau^2}\sigma_V^2 + a_k\Delta_k^2 \\ \text{for } m \text{ self-resets} \\ \\ (1-a_k)\frac{k-1}{k}\Theta_{k-1} - \frac{(1-a_k)(m+a_{k-1})}{k(k-1)\tau^2}\sigma_V^2 + \frac{(1-a_k)(m-1)}{k(k-1)\tau^2}\sigma_G^2 + a_k\Delta_k^2 \\ \text{for } m-1 \text{ self-resets} \end{cases} \\
\Phi_k^2 &= (1-a_k)^2\Phi_{k-1}^2 + {a_k}^2\Delta_k^2 + 2(1-a_k)a_k\Psi_k, \\
\hat{I}_k &= \hat{I}_{k-1} + a_k(\tilde{I}_{k,m} - \hat{I}_{k-1}).
\end{aligned}
$$

Note that to find the new estimate $\hat{I}_k$, only three parameters, a_k, Φ_k and Θ_k, the old estimate $\hat{I}_{k-1}$ and the new sample value $\tilde{I}_{k,m}$ are needed. Thus only a small fixed amount of memory per pixel independent of the number of captures is required.

Figure 5.7 compares SNR for a conventional sensor, a sensor using multiple capture and MSE estimation, and a self-reset sensor. The conventional sensor has dynamic range of 44dB and peak SNR of 36dB. Using linear estimation and saturation detection as described in Chapter 3 dynamic range is extended to 76dB — 8dB gain at the low illumination end and 24dB at the high illumination end. SNR is enhanced at low illumination but peak SNR remains the same. Now, using the proposed self-reset pixel architecture and in combination with the modified estimation algorithm, we can achieve the 76dB dynamic range, enhance SNR at the low illumination end, as well enhance peak SNR by 10dB. Note that the enhanced SNR is very close to the theoretical (and un-achievable) upper bound of 50dB for a sensor with infinite well capacity. The difference in SNR is due to the accumulation of reset noise due to the multiple resets.

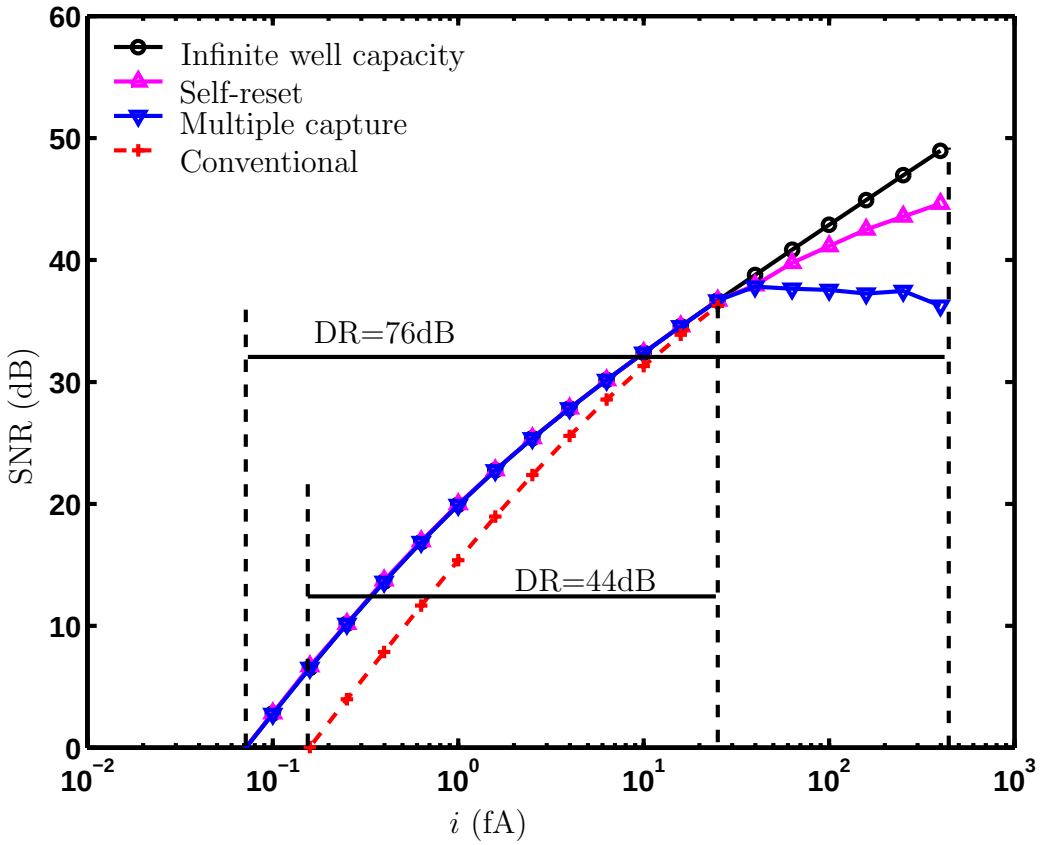


Figure 5.7: SNR and dynamic range comparison with well capacity $Q_{\text{sat}} = 6250e^-$, readout noise of $30e^-$, reset noise of $8e^-$ and total 32 multiple captures. The circled line is a sensor with infinite well capacity serving as a theoretical upper bound.

5.4 Summary

CMOS image sensors can benefit from technology scaling by reducing pixel size, increasing fill factor, reducing power consumption, and integrating more functionality on the same chip. However, sensor SNR deteriorates as technology scales due to the reduction in well capacity. This chapter described a self-reset DPS architecture that solves this problem by reusing the well several times during exposure time. The sensor is read out multiple times during exposure to detect the self-resets. We described a recursive estimation algorithm that uses the multiple capture to further enhance SNR by reducing the accumulated reset and readout noise. Simulation results using self-resetting and recursive estimation demonstrated enhanced peak SNR that is close to the ideal case of unbounded well capacity.

The self-reset architecture we described has several other side benefits including: (i) the possibility of further reduction in pixel size and fill factor since large well capacity is no longer necessary, (ii) more relaxed ADC design requirements due to the large effective signal swing, and (iii) eliminating the need for an anti-blooming device in each pixel.

Chapter 6

Conclusion

6.1 Summary

The continuous scaling of CMOS technology, together with the progress in the design of mixed-signal CMOS circuits, enables the possibility of system-on-a-chip integration. This integration will result in great reduction in system cost, size and power consumption. CMOS image sensors, therefore, will gradually replace CCDs in future digital cameras and other integrated imaging devices. Current generation of CMOS image sensors, however, generally suffer from lower SNR and dynamic range than CCDs due to their high read noise and non-uniformity. Moreover, as sensor design follows CMOS technology scaling, well capacity will continue to decrease, potentially resulting in unacceptably low SNR.

In this dissertation, we first presented a 352×288 CMOS Digital Pixel Sensor chip that demonstrated the high speed, non-destructive readout advantage of CMOS image sensors. Fabricated in a standard 0.18μm process, this chip is the first ever published that has a single slope ADC and 8-bit digital memory per pixel. It achieves an ultra high frame rate of $10,000$ frames/s while at a much lower cost than similar high speed CCD image sensors.

To enhance the sensor SNR and dynamic range, an algorithm based on statistical signal processing techniques is developed in this research. Making fully use of the high speed non-destructive readout advantage of CMOS image sensors, this algorithm synthesizes a high dynamic range, high SNR, and motion blur free image from multiple image captures. The algorithm consists of two main procedures — photocurrent estimation and motion/saturation detection. Photocurrent estimation is used to reduce read noise and thus to enhance dynamic range at the low illumination end. Saturation/motion detection is used to enhance dynamic range at the high illumination end and prevent the potential blur caused by motion. This detection also makes it possible to extend exposure time and to capture more images, which in turn can be used to further enhance dynamic range at the low illumination end.

Finally, to solve the problem with CMOS technology scaling and further enhance sensor SNR, a self-reset Digital Pixel Sensor (DPS) architecture is presented. In this architecture, each pixel resets itself one or more times during exposure as a function of its illumination level, resulting in higher effective well capacity and thus higher SNR. The photocurrent estimation and saturation/motion detection algorithm is then extended to take new noise components into consideration, and simulation results demonstrate significant dynamic range and SNR improvements.

The algorithm and architecture proposed in this research operates completely locally and recursively, thus significantly reduces the computation complexity and memory requirement. This modest computation and storage requirements make the algorithm well suited for single chip digital camera implementation.

6.2 Recommendation for future work

At present, most digital cameras still use CCD image sensors. It is hoped that the algorithm and approach we are studying will provide the basis for the integration of a high dynamic range and high SNR camera on a chip with the most advanced CMOS technology. However, to develop a CMOS image sensor with the optimal performance and yet the minimum cost, a number of issues are yet to be addressed. Below is a

summary of some of the issues that await exploration.

The test chip described in Chapter 2 has relatively low quantum efficiency and high dark current. These are due to the use of advanced digital process that are aggressively scaled for transistor switching speed. In general, sensors fabricated with advanced processes have inferior performance than those using old generation processes [19]. The superior photodetector characteristics of CCDs are the result of long time research and advancement, and the same performance is expected from CMOS image sensors given certain research efforts. In fact, active studies in improving sensor quantum efficiency and reducing dark current are under way, and some results are very promising [113]. The critical question is how to minimize the required modifications to the standard CMOS process so that the sensor can achieve CCD performance while still enjoys the cost advantage of CMOS technology.

The algorithm proposed in this dissertation requires 50 operations per pixel per capture with a dedicated hardware MAC. Assuming a sensor with 1000×1000 pixels and each output frame is synthesized from 32 multiple samples captured within 32ms (equivalent 1000 frames/s), the total computation required for each output frame is 1.6 billion operations. For video imaging applications, the number of captures per output frame (thus the total computation requirement) can be reduced due to the low SNR requirement in video.

There are different architectures for on-chip implementation of this algorithm, the processor core can be integrated at pixel level, column level or chip level. A pixel level implementation has the advantages of the dramatically reduced processing speed requirement, scaling well with array size and frame rate, local memory access and no need to shift out the intermediate captures from pixel array. The area occupied by the processor implemented with current technology, however, maybe much bigger than the pixel area, therefore is not practical at present. However, as CMOS technology scales, the area occupied by the transistors will decrease while pixel size may keep the same due to optical requirement. Moreover, new technologies such as vertical integration of multiple transistor layers may provide the possibility for new sensor design with pixel level processing.

In [68], Lim *et. al.* , proposed a single chip imaging system architecture where

multiple column level SIMD processor are integrated together with the sensor array. Each processor processes the data from single column or multiple columns of pixels, and all the processors are running simultaneously under one controller. Figure 6.1 shows the proposed system architecture.

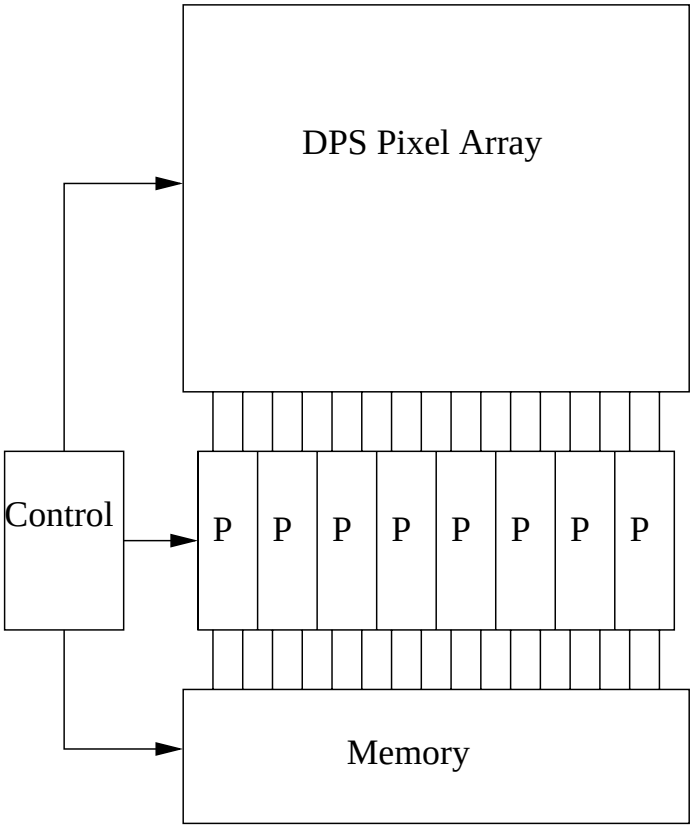


Figure 6.1: Proposed a single chip imaging system architecture with column level processors in [68].

At current technology, column processing seems a good candidate. Since our algorithm is pixel-wise and recursive, a customized instruction set and processor architecture can potentially increase the processing speed significantly. Further study on the processor architecture and optimal memory arrangement is needed.

Appendix A

Recursive solution

To see Equation 3.9 has a recursive solution, first the condition

$$\frac{\partial F}{\partial a_l^{(k)}} = 0 \text{ for } 1 \leq l \leq k$$

can be expanded to the following equations by bringing Equation 3.7 into Equation 3.8 and performing the partial derivative with respect to $a_1^{(k)}$, $a_{j-1}^{(k)}$, $a_j^{(k)}$, respectively:

$$(\sum_{m=1}^{k} \frac{a_m^{(k)}}{m})\frac{\sigma_U^2}{\tau^2} + a_1^{(k)}\frac{\sigma_V^2}{\tau^2} + \frac{\lambda}{2} = 0 \tag{A.1}$$

$$\sum_{l=1}^{j-1}(\sum_{m=l}^{k} \frac{a_m^{(k)}}{m})\frac{\sigma_U^2}{\tau^2} + \frac{a_{j-1}^{(k)}}{(j-1)}\frac{\sigma_V^2}{\tau^2} + \frac{(j-1)\lambda}{2} = 0 \tag{A.2}$$

$$\sum_{l=1}^{j}(\sum_{m=l}^{k} \frac{a_m^{(k)}}{m})\frac{\sigma_U^2}{\tau^2} + \frac{a_j^{(k)}}{j}\frac{\sigma_V^2}{\tau^2} + \frac{j\lambda}{2} = 0 \tag{A.3}$$

The above equation A.3 can be rearranged as:

$$\begin{aligned}&\textstyle\sum_{l=1}^{j-1}(\sum_{m=l}^{k}\frac{a_m^{(k)}}{m})\frac{\sigma_U^2}{\tau^2}+(\sum_{m=1}^{k}\frac{a_m^{(k)}}{m})\frac{\sigma_U^2}{\tau^2}\\&-(\textstyle\sum_{m=1}^{j-1}\frac{a_m^{(k)}}{m})\frac{\sigma_U^2}{\tau^2}+\frac{a_j^{(k)}}{j}\frac{\sigma_V^2}{\tau^2}+\frac{j\lambda}{2}=0\end{aligned}\tag{A.4}$$

where the first two terms can be found in Equation A.2 and A.1, respectively. Bring Equation A.1 and A.2 into A.4, then we will have:

$$\begin{aligned}&(-\tfrac{a_{j-1}^{(k)}}{j-1}\tfrac{\sigma_V^2}{\tau^2}-\tfrac{(j-1)\lambda}{2})+(-a_1^{(k)}\tfrac{\sigma_V^2}{\tau^2}-\tfrac{\lambda}{2})-(\textstyle\sum_{m=1}^{j-1}\frac{a_m^{(k)}}{m})\frac{\sigma_U^2}{\tau^2}\\&+\tfrac{a_j^{(k)}}{j}\tfrac{\sigma_V^2}{\tau^2}+\tfrac{j\lambda}{2}=0\end{aligned}$$

or:

$$a_j^{(k)}=ja_1^{(k)}+\frac{j}{j-1}a_{j-1}^{(k)}+\frac{j\sigma_U^2}{\sigma_V^2}(\sum_{m=1}^{j-1}\frac{a_m^{(k)}}{m})\tag{A.5}$$

which is Equation 3.10 in Chapter 3.1.1.

The above solution implies that when the total of k captures used in the estimation, the coefficient used for the jth sample, $a_j^{(k)}$, can be represented by the coefficients used for the previous captures, $\{a_1^{(k)}, a_2^{(k)}, \ldots, a_{j-1}^{(k)}\}$. This suggests a recursive relationship for the coefficients. Under this recursive form, coefficients $\{a_2^{(k)}, a_3^{(k)}, \ldots, a_k^{(k)}\}$ all can be represented by $a_1^{(k)}$, which in turn can be solved by applying the unbiased estimation constrain, *i.e.*,

$$\sum_{j=1}^{k}a_j^{(k)}=1.$$

Therefore, we solved the optimal coefficients for the photocurrent estimation with total k captures, where $1 \leq k \leq n$. However, as new capture added into the estimation each time, *i.e.*, now with total of $k+1$ captures, those coefficients need to be calculated

again since $a_j^{(k)} \neq a_j^{(k+1)}$ for $1 \leq j \leq k$.

To derive the optimal estimate in a recursive form, we define the set of weights b_j, such that:

$$\begin{cases} b_1 &= 1, \\ b_j &= jb_1 + \frac{j}{j-1}b_{j-1} + \frac{j\sigma_U^2}{\sigma_V^2}(\sum_{l=1}^{j-1}\frac{b_l}{l}) \text{ for } j \geq 2. \end{cases} \tag{A.6}$$

Note that while $a_j^{(k)}$ changes with k, b_j can be calculated recursively since b_1 is fixed; b_j does not need to be re-calculated as k increases to $k+1$. The relationship between $a_j^{(k)}$ and b_j is:

$$a_j^{(k)} = \frac{b_j}{\sum_{l=1}^{k} b_l} \text{ for } 1 \leq j \leq k,$$

i.e., the $a_j^{(k)}$s are the normalized versions of the b_js.

With the introduction of coefficient set b_j $(1 \leq j \leq k)$, the estimated photocurrent with total k captures is:

$$\begin{aligned} \hat{I}_k &= \sum_{j=1}^{k} a_j^{(k)} \tilde{I}_j \\ &= \sum_{j=1}^{k} \frac{b_j}{g_k} \tilde{I}_j \end{aligned}$$

where

$$g_k = \sum_{l=1}^{k} b_l$$

The estimated photocurrent with total $k+1$ measurements is:

$$\hat{I}_{k+1} = \sum_{j=1}^{k+1} a_j^{(k+1)} \tilde{I}_j$$

$$\begin{aligned} &= \sum_{j=1}^{k+1} \frac{b_j}{g_{k+1}} \tilde{I}_j \\ &= \sum_{j=1}^{k} \frac{b_j}{g_{k+1}} \tilde{I}_j + \frac{b_{k+1}}{g_{k+1}} \tilde{I}_{k+1} \\ &= (1 - \frac{b_{k+1}}{g_{k+1}}) \hat{I}_k + \frac{b_{k+1}}{g_{k+1}} \tilde{I}_{k+1} \\ &= \hat{I}_k + \frac{b_{k+1}}{g_{k+1}} (\tilde{I}_{k+1} - \hat{I}_k) \end{aligned}$$

Define:

$$h_{k+1} = \frac{b_{k+1}}{g_{k+1}}$$

Then the above equation becomes:

$$\hat{I}_{k+1} = \hat{I}_k + h_{k+1}(\tilde{I}_{k+1} - \hat{I}_k)$$

Which is the photocurrent estimate in a recursive form.

The MSE of estimation, as shown in Equation 3.7, can also be calculated recursively as following. First,

$$\begin{aligned} \Phi_k^2 &= \textstyle\sum_{j=1}^{k} ((\sum_{l=j}^{k} \frac{a_l^{(k)}}{l})^2 \frac{\sigma_U^2}{\tau^2} + (\frac{a_j^{(k)}}{j})^2 \frac{\sigma_V^2}{\tau^2}) \\ &= \textstyle\frac{1}{g_k^2} (\sum_{j=1}^{k} (\sum_{l=j}^{k} \frac{b_l}{l})^2 \frac{\sigma_U^2}{\tau^2} + \sum_{l=1}^{k} (\frac{b_l}{l})^2 \frac{\sigma_V^2}{\tau^2}) \end{aligned} \tag{A.7}$$

The MSE with with total $k+1$ captures is:

$$\begin{aligned}
\Phi^2_{k+1} &= \frac{1}{g^2_{k+1}}(\sum_{j=1}^{k+1}(\sum_{l=j}^{k+1}\frac{b_l}{l})^2\frac{\sigma^2_U}{\tau^2} + \sum_{l=1}^{k+1}(\frac{b_l}{l})^2\frac{\sigma^2_V}{\tau^2}) \\
&= \frac{1}{g^2_{k+1}}(\sum_{j=1}^{k}(\sum_{l=j}^{k+1}\frac{b_l}{l})^2\frac{\sigma^2_U}{\tau^2} + \sum_{l=1}^{k}(\frac{b_l}{l})^2\frac{\sigma^2_V}{\tau^2} \\
&\quad +2\sum_{j=1}^{k}\sum_{l=j}^{k}\frac{b_l}{l}\frac{b_{k+1}}{k+1}\frac{\sigma^2_U}{\tau^2} + \frac{k}{k+1}b_{k+1}\frac{\sigma^2_U}{\tau} \\
&\quad +(\frac{b_{k+1}}{k+1})^2(\frac{\sigma^2_U}{\tau^2} + \frac{\sigma^2_V}{\tau^2}))
\end{aligned} \tag{A.8}$$

Again, note that the first two terms in Equation A.8 are contained in Equation A.7. Thus by bringing A.7 into A.8, we have:

$$\begin{aligned}
\Phi^2_{k+1} &= \frac{g^2_k}{g^2_{k+1}}\Phi^2_k + \frac{1}{g^2_{k+1}}((2b_{k+1}g_k + b^2_{k+1})\frac{\sigma^2_U}{(k+1)\tau^2} \\
&\quad +b^2_{k+1}\frac{\sigma^2_V}{(k+1)^2\tau^2})
\end{aligned} \tag{A.9}$$

So, MSE Φ^2_k can be calculated recursively, as well.

Appendix B

Weighted CDS

Given that

$$Q_k = ik\tau + \sum_{j=1}^{k} U_j + V_k + C \text{ for } 0 \leq k \leq n$$

the best estimator of photocurrent i can be written as:

$$\hat{I}_k = \sum_{j=0}^{k} a_j Q_j \tag{B.1}$$

The MSE of this estimator is:

$$\begin{aligned}
\Phi_k^2 &= E(\hat{I}_k - i)^2 \\
&= E(\textstyle\sum_{j=0}^{k} a_j Q_j - i)^2 \\
&= E(a_0(V_0 + C) + a_1(i\tau + U_1 + V_1 + C) + \ldots - i)^2 \\
&= E(a_0 V_0 + \textstyle\sum_{j=0}^{k} a_j C + \sum_{j=1}^{k}(\sum_{m=j}^{k} a_m)U_j + \sum_{j=1}^{k}(a_j V_j))^2 \\
&= a_0^2\sigma_V^2 + (\textstyle\sum_{j=0}^{k} a_j)^2\sigma_C^2 + \sum_{j=1}^{k}(\sum_{m=j}^{k} a_m)^2\sigma_U^2 + \sum_{j=1}^{k} a_j^2\sigma_V^2
\end{aligned} \tag{B.2}$$

To minimize the MSE, we need:

$$\frac{\partial \Phi_k^2}{\partial a_0} = 2a_0\sigma_V^2 + 2(\sum_{j=0}^{k} a_j)\sigma_C^2 = 0$$

Define

$$w = \frac{\sigma_C^2}{\sigma_C^2 + \sigma_V^2}$$

then we have

$$a_0 = -w(\sum_{j=1}^{k} a_j) \tag{B.3}$$

bring this into equation B.1, we have:

$$\begin{aligned} \hat{I}_k &= \textstyle\sum_{j=0}^{k} a_j Q_j \\ &= \textstyle\sum_{j=1}^{k} a_j Q_j - w(\sum_{j=1}^{k} a_j) Q_0 \qquad \text{(B.4)} \\ &= \textstyle\sum_{j=1}^{k} a_j (Q_j - wQ_0). \end{aligned}$$

so we see here w is the coefficient for the weighted CDS.

Appendix C

Non-recursive solution

Since

$$Q_k = ik\tau + \sum_{j=1}^{k} U_j + V_k + C \text{ for } 0 \leq k \leq n$$

we have

$$\tilde{I}_k = \frac{Q_k - wQ_0}{k\tau} = i + \frac{\sum_{j=1}^{k} U_j}{k\tau} + \frac{V_k}{k\tau} + \frac{(1-w)C}{k\tau} - \frac{wV_0}{k\tau}$$

With

$$\hat{I}_k = \mathbf{A}_k \tilde{\mathbf{I}}_k,$$

where

$$\mathbf{A}_k = [a_1^{(k)}\ a_2^{(k)}\ \ldots\ a_2^{(k)}], \text{ and}$$

$$\tilde{\mathbf{I}}_k = [\tilde{I}_1\ \tilde{I}_2\ \ldots\ \tilde{I}_k]^T.$$

The mean square error (MSE) Φ_k^2 of $\hat{I}_k$ is given by

$$\begin{aligned}
\Phi_k^2 &= E(\hat{I}_k - i)^2 \\
&= E(\textstyle\sum_{j=1}^{k} a_j^{(k)} (\frac{\sum_{l=1}^{j} U_l + V_j + (1-w)C - wV_0}{k\tau}))^2 \\
&= (\textstyle\sum_{j=1}^{k} (\sum_{l=j}^{k} \frac{a_l^{(k)}}{l})^2) \frac{\sigma_U^2}{\tau^2} + \sum_{j=1}^{k} (\frac{a_j^{(k)}}{j})^2 \frac{\sigma_V^2}{\tau^2} + \\
&\quad w^2 (\textstyle\sum_{j=1}^{k} a_j^{(k)})^2 \frac{\sigma_V^2}{(k\tau)^2} + (1-w)^2 (\sum_{j=1}^{k} a_j^{(k)})^2 \frac{\sigma_C^2}{(k\tau)^2} \\
&= (\textstyle\sum_{j=1}^{k} (\sum_{l=j}^{k} \frac{a_l^{(k)}}{l})^2) \frac{\sigma_U^2}{\tau^2} + \sum_{j=1}^{k} (\frac{a_j^{(k)}}{j})^2 \frac{\sigma_V^2}{\tau^2} + \\
&\quad w (\textstyle\sum_{j=1}^{k} a_j^{(k)})^2 \frac{\sigma_V^2}{(k\tau)^2}.
\end{aligned} \tag{C.1}$$

This is a convex optimization problem with a linear constraint as in (3.6). To solve it, we define the Lagrangian

$$F(a_1^{(k)}, a_2^{(k)}, \ldots, a_k^{(k)}) = \Phi_k^2 + \lambda(\sum_{j=1}^{k} a_j^{(k)} - 1) \tag{C.2}$$

where λ is the Lagrange multiplier.

The optimal weights can be found using the conditions:

$$\begin{cases}
\bigtriangledown F &= \left[\begin{array}{cccc} \frac{\partial F}{\partial a_1^{(k)}} & \frac{\partial F}{\partial a_2^{(k)}} & \cdots & \frac{\partial F}{\partial a_k^{(k)}} \end{array} \right]^T = 0, \\
\sum_{j=1}^{k} a_j^{(k)} &= 1.
\end{cases} \tag{C.3}$$

By carrying on the partial derivative, the above equation can be expanded. The

jth equation has the form as:

$$\sum_{l=1}^{j}(\sum_{m=l}^{k}\frac{a_m^{(k)}}{m})\frac{\sigma_U^2}{\tau^2}+\frac{a_j^{(k)}}{j}\frac{\sigma_V^2}{\tau^2}+w(\sum_{m=1}^{k}\frac{a_m^{(k)}}{m})\frac{\sigma_V^2}{\tau^2}+\frac{j\lambda}{2}=0 \tag{C.4}$$

or in a matrix format:

$$(M_k\frac{\sigma_U^2}{\tau^2}+D_k\frac{\sigma_V^2}{\tau^2})\mathbf{A}_k+\frac{\lambda}{2}L_k=0 \tag{C.5}$$

where

$$M_k=\begin{bmatrix}1 & \frac{1}{2} & \dots & \frac{1}{k}\\ 1 & 1 & \dots & \frac{2}{k}\\ \dots & & & \\ 1 & 1 & \dots & 1\end{bmatrix},\ L_k=\begin{bmatrix}1\\2\\\vdots\\k\end{bmatrix},$$

$$D_k=\begin{bmatrix}2w & \frac{w}{2} & \frac{w}{3} & \dots & \frac{w}{k}\\ w & w & \frac{w}{3} & \dots & \frac{w}{k}\\ w & \frac{w}{2} & \frac{2w}{3} & \dots & \frac{3}{k}\\ \dots & & & & \\ w & \frac{w}{2} & \frac{w}{3} & \dots & \frac{2w}{k}\end{bmatrix}.$$

And the coefficients vector $\mathbf{A_k}$ can be solved using matrix inversion as:

$$\mathbf{A}_k=-(M_k\frac{\sigma_U^2}{\tau^2}+D_k\frac{\sigma_V^2}{\tau^2})^{-1}\frac{\lambda}{2}L_k \tag{C.6}$$

Appendix D

Recursive condition

For the estimation algorithm to be running recursively, recall:

$$\begin{aligned}\hat{I}_{k+1} &= \hat{I}_k + a_{k+1}^{(k+1)}(\tilde{I}_{k+1} - \hat{I}_k) \\ &= (1 - a_{k+1}^{(k+1)}) \sum_{j=1}^{k} a_j^{(k)} \tilde{I}_j + a_{k+1}^{(k+1)} \tilde{I}_{k+1}\end{aligned}$$

but $\hat{I}_{k+1}$ is also

$$\hat{I}_{k+1} = \sum_{j=1}^{k+1} a_j^{(k+1)} \tilde{I}_j$$

So, we have:

$$a_j^{(k+1)} = (1 - a_{k+1}^{(k+1)}) a_j^{(k)}, \text{ for } 1 \leq j \leq k,$$

or in another format:

$$\frac{a_1^{(k+1)}}{a_1^{(k)}} = \frac{a_2^{(k+1)}}{a_2^{(k)}} = \ldots = \frac{a_k^{(k+1)}}{a_k^{(k)}} = 1 - a_{k+1}^{(k+1)} \tag{D.1}$$

With total k samples, the first two equations of equation array C.4, *i.e.*, $j = 1, j =$

2, respectively, are:

$$\begin{aligned}
&(\textstyle\sum_{m=1}^{k} \frac{a_m^{(k)}}{m})\frac{\sigma_U^2+w\sigma_V^2}{\tau^2} + a_1^{(k)}\frac{\sigma_V^2}{\tau^2} + \frac{\lambda^{(k)}}{2} = 0 \\
&(\textstyle\sum_{m=1}^{k} \frac{a_m^{(k)}}{m})\frac{\sigma_U^2+w\sigma_V^2}{\tau^2} + (\sum_{m=2}^{k} \frac{a_m^{(k)}}{m})\frac{\sigma_U^2}{\tau^2} + \frac{a_2^{(k)}}{2}\frac{\sigma_V^2}{\tau^2} + \frac{2\lambda^{(k)}}{2} = 0
\end{aligned} \tag{D.2}$$

with total $k+1$ samples, the first two equations of equation array C.4, *i.e.*, $j = 1, j = 2$, respectively, are:

$$\begin{aligned}
&(\textstyle\sum_{m=1}^{k+1} \frac{a_m^{(k+1)}}{m})\frac{\sigma_U^2+w\sigma_V^2}{\tau^2} + a_1^{(k+1)}\frac{\sigma_V^2}{\tau^2} + \frac{\lambda^{(k+1)}}{2} = 0 \\
&(\textstyle\sum_{m=1}^{k+1} \frac{a_m^{(k+1)}}{m})\frac{\sigma_U^2+w\sigma_V^2}{\tau^2} + (\sum_{m=2}^{k+1} \frac{a_m^{(k+1)}}{m})\frac{\sigma_U^2}{\tau^2} + \frac{a_2^{(k+1)}}{2}\frac{\sigma_V^2}{\tau^2} + \frac{2\lambda^{(k+1)}}{2} = 0
\end{aligned} \tag{D.3}$$

Assuming that recursive relationship solution exist, using the relationship in equation D.1, equation D.3 becomes:

$$\begin{aligned}
&(1 - a_{k+1}^{(k+1)})((\textstyle\sum_{m=1}^{k} \frac{a_m^{(k)}}{m})\frac{\sigma_U^2+w\sigma_V^2}{\tau^2} + a_1^{(k)}\frac{\sigma_V^2}{\tau^2}) \\
&+\frac{a_{k+1}^{(k+1)}}{k+1}\frac{\sigma_U^2+w\sigma_V^2}{\tau^2} = -\frac{\lambda^{(k+1)}}{2} \\
&(1 - a_{k+1}^{(k+1)})((\textstyle\sum_{m=1}^{k} \frac{a_m^{(k)}}{m})\frac{\sigma_U^2+w\sigma_V^2}{\tau^2} + (\sum_{m=2}^{k} \frac{a_m^{(k)}}{m})\frac{\sigma_U^2}{\tau^2} + \frac{a_2^{(k)}}{2}\frac{\sigma_V^2}{\tau^2}) \\
&+\frac{a_{k+1}^{(k+1)}}{k+1}\frac{2\sigma_U^2+w\sigma_V^2}{\tau^2} = -\frac{2\lambda^{(k+1)}}{2}
\end{aligned} \tag{D.4}$$

bring D.2 into above equations, we then have:

$$\frac{a_{k+1}^{(k+1)}}{k+1}\frac{\sigma_U^2+w\sigma_V^2}{\tau^2} = (1-a_{k+1}^{(k+1)})\frac{\lambda^{(k)}}{2} - \frac{\lambda^{(k+1)}}{2}$$

$$\frac{a_{k+1}^{(k+1)}}{k+1}\frac{2\sigma_U^2+w\sigma_V^2}{\tau^2} = (1-a_{k+1}^{(k+1)})\frac{2\lambda^{(k)}}{2} - \frac{2\lambda^{(k+1)}}{2}$$

i.e.,

$$\frac{\sigma_V^2}{\tau^2} = 0 \tag{D.5}$$

Which is contradictory. On the other hand, it proves that the recursive exist if we neglect the read noise when sampling the initial offset value.

Appendix E

Suboptimal recursive solution

Given

$$\begin{aligned} \tilde{I}_{k-1} &= i + \frac{\sum_{j=1}^{k-1} U_j}{(k-1)\tau} + \frac{V_{k-1}}{(k-1)\tau} - \frac{wV_0}{(k-1)\tau} + \frac{(1-w)C}{(k-1)\tau} \\ \tilde{I}_k &= i + \frac{\sum_{j=1}^{k} U_j}{k\tau} + \frac{V_k}{k\tau} - \frac{wV_0}{k\tau} + \frac{(1-w)C}{k\tau} \end{aligned} \tag{E.1}$$

So we have the following relationship between $\tilde{I}_{k-1}$ and $\tilde{I}_k$:

$$\tilde{I}_k = \frac{k-1}{k}\tilde{I}_{k-1} + \frac{i}{k} + \frac{U_k}{k\tau} + \frac{V_k}{k\tau} - \frac{V_{k-1}}{(k-1)\tau} \tag{E.2}$$

The MSE of $\tilde{I}_k$ is:

$$\begin{aligned}
\Delta_k^2 &= E(\tilde{I}_k - i)^2 \\
&= E(\tfrac{\sum_{j=1}^{k} U_j}{k\tau} + \tfrac{V_k}{k\tau} + \tfrac{(1-w)C}{k\tau} - \tfrac{wV_0}{k\tau})^2 \\
&= \tfrac{1}{k^2\tau^2}(k\sigma_U^2 + (1+w^2)\sigma_V^2 + (1-w)^2\sigma_C^2) \\
&= \tfrac{1}{k^2\tau^2}(k\sigma_U^2 + (1+w)\sigma_V^2)
\end{aligned} \tag{E.3}$$

We first calculate the recursive relation between covariance $\Theta_k = cov(\hat{I}_k, \tilde{I}_k)$ and $\Theta_{k-1} = cov(\hat{I}_{k-1}, \tilde{I}_{k-1})$ as follows:

$$\begin{aligned}
\Theta_k &= E((\hat{I}_k - i)(\tilde{I}_k - i)) \\
&= E((\hat{I}_{k-1} + h_k(\tilde{I}_k - \hat{I}_{k-1}) - i)(\tilde{I}_k - i)) \\
&= (1-h_k)E((\hat{I}_{k-1} - i)(\tilde{I}_k - i)) + h_k E(\tilde{I}_k - i)^2 \\
&= (1-h_k)E((\hat{I}_{k-1} - i)(\tfrac{k-1}{k}\tilde{I}_{k-1} + \tfrac{i}{k} + \tfrac{U_k}{k\tau} + \tfrac{V_k}{k\tau} \\
&\quad -\tfrac{V_{k-1}}{(k-1)\tau} - i)) + h_k\Delta_k^2 \\
&= (1-h_k)\tfrac{k-1}{k}E((\hat{I}_{k-1} - i)(\tilde{I}_{k-1} - i)) \\
&\quad -\tfrac{(1-h_k)}{k\tau}E((\hat{I}_{k-1} - i)V_{k-1}) + h_k\Delta_k^2 \\
&= (1-h_k)\tfrac{k-1}{k}\Theta_{k-1} - \tfrac{(1-h_k)h_{k-1}}{k(k-1)\tau}\sigma_V^2 + h_k\Delta_k^2
\end{aligned} \tag{E.4}$$

We want to find h_k such that the estimate MSE $\Phi_k^2 = E(\hat{I}_k - i)^2$ is minimized. Φ_k^2

is given by:

$$\begin{aligned}
\Phi_k^2 &= E(\hat{I}_k - i)^2 \\
&= E(\hat{I}_{k-1} + h_k(\tilde{I}_k - \hat{I}_{k-1}) - i)^2 \\
&= E((1-h_k)(\hat{I}_{k-1} - i) + h_k(\tilde{I}_k - i))^2 \\
&= (1-h_k)^2\Phi_{k-1}^2 + h_k^2\Delta_k^2 \\
&\quad +2h_k(1-h_k)E((\hat{I}_{k-1} - i)(\tilde{I}_k - i))
\end{aligned} \tag{E.5}$$

where the last term in the above equation can be written as:

$$\begin{aligned}
&E((\hat{I}_{k-1} - i)(\tilde{I}_k - i)) \\
&= E(\tfrac{\hat{I}_k - h_k\tilde{I}_k}{1-h_k} - i)(\tilde{I}_k - i) \\
&= \tfrac{1}{1-h_k}\Theta_k - \tfrac{h_k}{1-h_k}\Delta_k^2
\end{aligned} \tag{E.6}$$

Thus Equation E.5 becomes:

$$\Phi_k^2 = (1-h_k)^2\Phi_{k-1}^2 + 2h_k\Theta_k - {h_k}^2\Delta_k^2 \tag{E.7}$$

Bring Equation E.4 into Equation E.7, we get:

$$\begin{aligned}
\Phi_k^2 &= (1-h_k)^2\Phi_{k-1}^2 + \tfrac{2(k-1)(1-h_k)h_k}{k}\Theta_k \\
&\quad -\tfrac{2h_{k-1}(1-h_k)h_k}{k(k-1)\tau}\sigma_V^2 + {h_k}^2\Delta_k^2
\end{aligned} \tag{E.8}$$

To minimize the MSE, we require that

$$\frac{d\,\Phi_k^2}{d\,h_k} = 0,$$

Which gives

$$h_k = \frac{\Phi_{k-1}^2 - \frac{(k-1)}{k}\Theta_{k-1} + \frac{h_{k-1}\sigma_V^2}{k(k-1)\tau^2}}{\Phi_{k-1}^2 - \frac{2(k-1)}{k}\Theta_{k-1} + \frac{2h_{k-1}\sigma_V^2}{k(k-1)\tau^2} + \Delta_k^2} \tag{E.9}$$

Appendix F

Prediction error

The prediction error of next sample $\tilde{I}_{k+1}$ using $\hat{I}_k$ is:

$$\begin{aligned}
\Delta^2_{pre} &= E(\tilde{I}^{pre}_{k+1} - \hat{I}_k|\hat{I}_k)^2 \\
&= E(\tfrac{k}{k+1}\tilde{I}_k + \tfrac{i}{k+1} + \tfrac{U_{k+1}}{(k+1)\tau} + \tfrac{V_{k+1}}{(k+1)\tau} - \tfrac{V_k}{(k+1)\tau} - \hat{I}_k)^2 \\
&= E(\tfrac{k}{k+1}(\tilde{I}_k - i) - (\hat{I}_k - i) + \tfrac{U_{k+1}}{(k+1)\tau} + \tfrac{V_{k+1}}{(k+1)\tau} - \tfrac{V_k}{(k+1)\tau})^2 \qquad \text{(F.1)} \\
&= (\tfrac{k}{k+1})^2\Delta^2_k + \Phi^2_k - \tfrac{2k}{k+1}\Theta_k \\
&\quad + \tfrac{\sigma^2_U}{(k+1)^2\tau^2} + \tfrac{2h_k}{k(k+1)\tau^2}\sigma^2_V
\end{aligned}$$

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