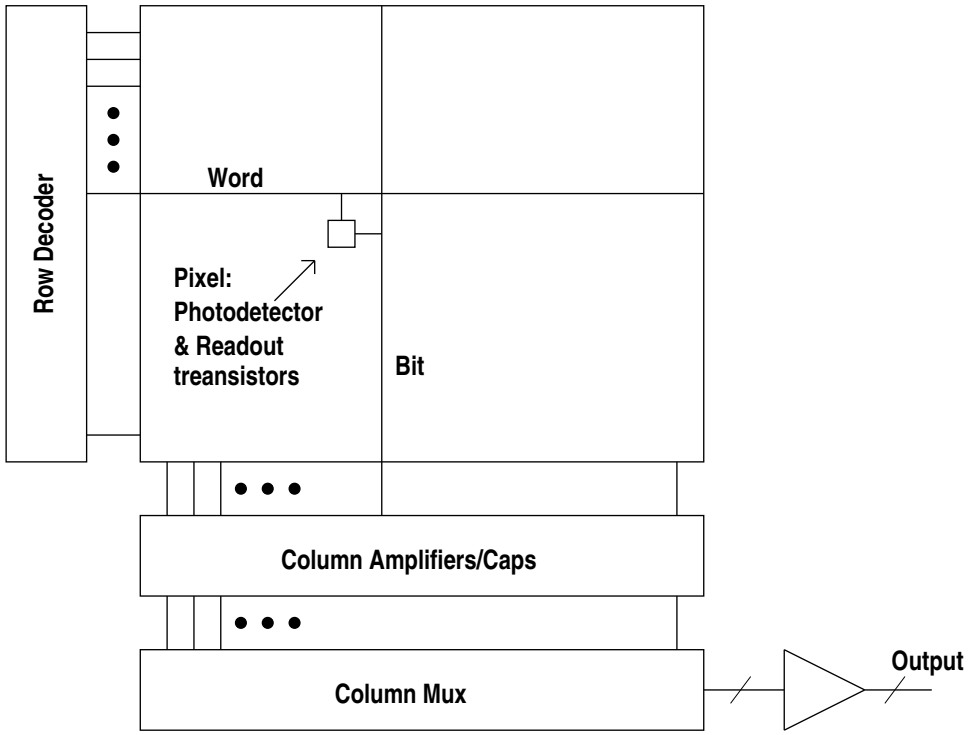
Lecture Notes 4
CMOS Image Sensors

- CMOS Passive Pixel Sensor (PPS)
  - Basic operation
  - Charge to output voltage transfer function
  - Readout speed
- CMOS Photodiode Active Pixel Sensor (APS)
  - Basic operation
  - Charge to output voltage transfer function
  - Readout speed
- Photogate and Pinned Diode APS
- Multiplexed APS

Introduction

- CMOS image sensors are fabricated in "standard" CMOS technologies
- Their main advantage over CCDs is the ability to integrate analog and digital circuits with the sensor
  - Less chips used in imaging system
  - Lower power dissipation
  - Faster readout speeds
  - More programmability
  - New functionalities (high dynamic range, biometric, etc)
- But they generally have lower perofrmance than CCDs:
  - Standard CMOS technologies are not optimized for imaging
  - More circuits result in more noise and fixed pattern noise
- In this lecture notes we discuss various CMOS imager architectures
- In the following lecture notes we discuss fabrication and layout issues

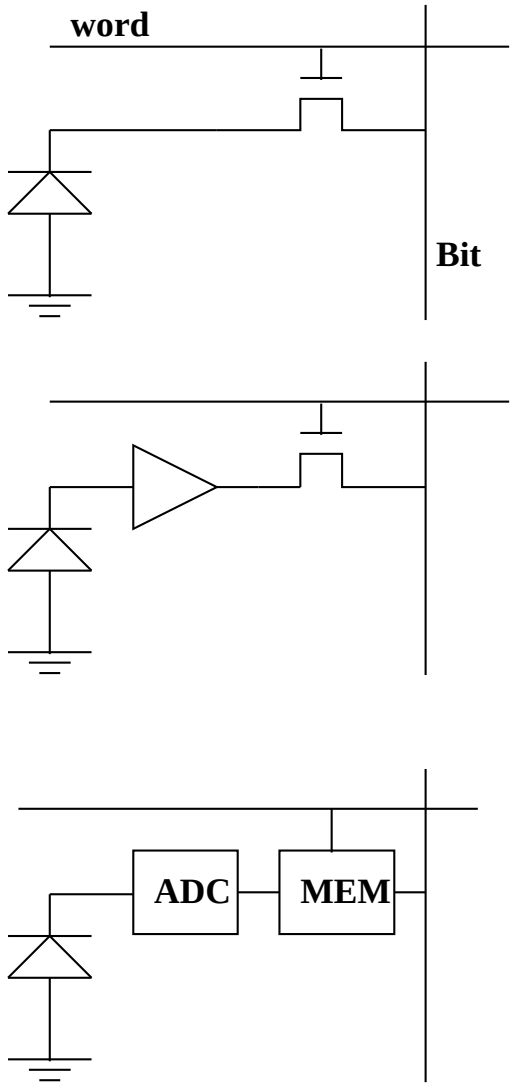
CMOS Image Sensor Architecture



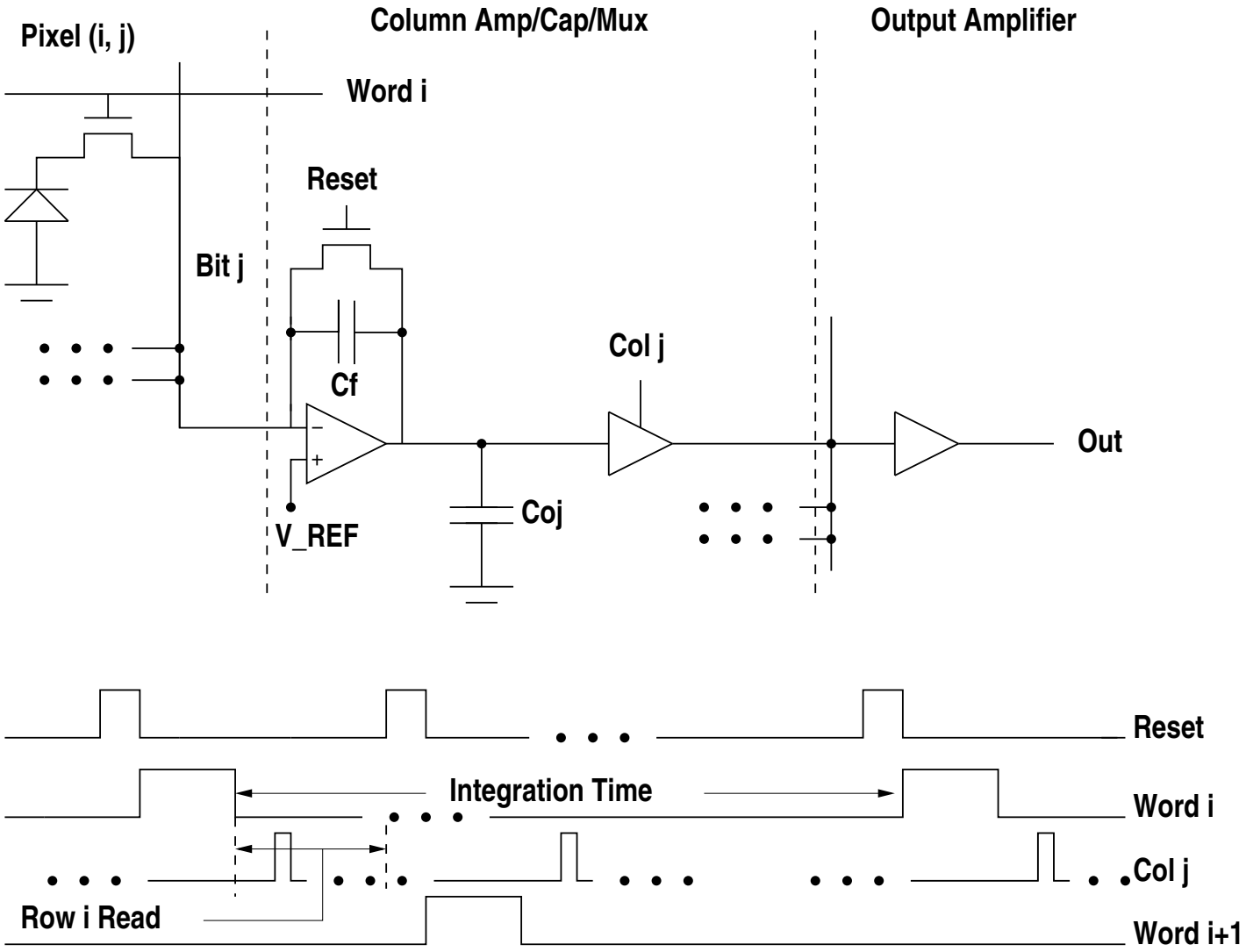
- Readout performed by transferring one row at a time to the column storage capacitors, then reading out the row, one (or more) pixel at a time, using the column decoder and multiplexer
- In many CMOS image sensor architectures, row integration times are *staggerred* by the row/column readout time (scrolling shutter)

CMOS Image Sensor Pixel Architectures

- Passive pixel (PPS)
  - 1 transistor per pixel
  - small pixel, large fill factor
  - slow, low SNR
- Active pixel (APS)
  - 1.5-4 transistors per pixel
  - faster, higher SNR
  - larger pixel, lower fill factor
  - current technology of choice
- Digital pixel (DPS)
  - 5+ transistors per pixel
  - scales well with technology
  - very fast, no column noise or FPN
  - larger pixel, complex implementation

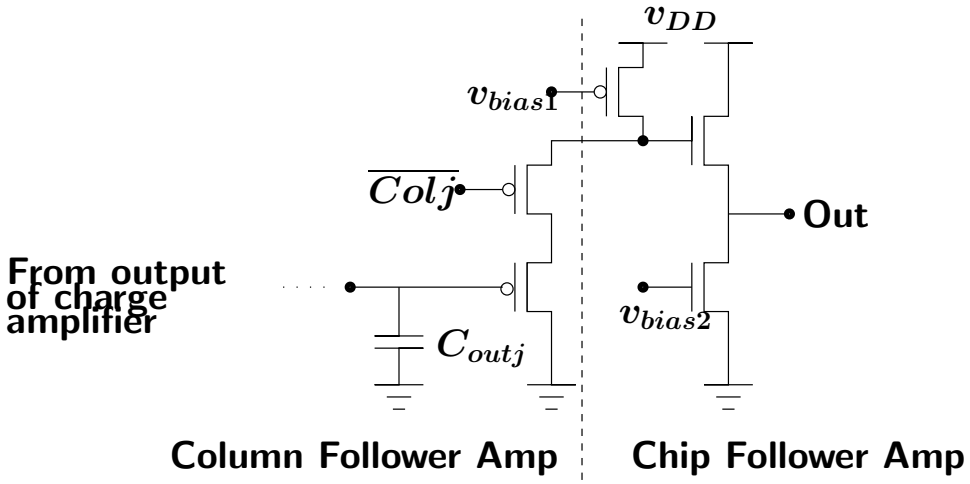


Passive Pixel Sensor (PPS)



Comments on Operation

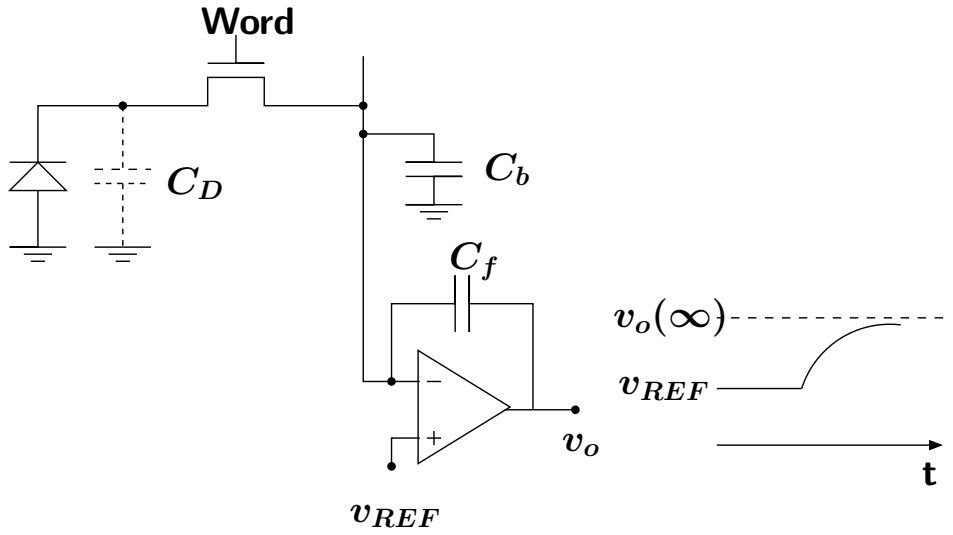
- Charge is read out via a column charge amplifier (also referred to as Capacitive Trans-impedence Amplifier (CTIA))
- Reading is destructive (much like a DRAM)
- Vertical charge binning is very easy to implement
- Diode reverse bias voltage at end of reading $\approx v_{REF}$
- Column and chip amplifiers are simple follower amplifiers



- Depending on the design, frame readout time can be limited either by the row transfer time or by the column readout time

PPS Charge to Output Voltage Transfer Function

- Consider the PPS column read circuit



- In steady state, assuming charge Q_{sig} (electrons) accumulated on the photodiode at the end of integration (and ignoring "feedthrough" voltage added when the reset transistor is turned off and opamp offset voltage), the output voltage

$$v_o = v_{REF} + \frac{qQ_{sig}}{C_f}$$

Thus the sensor conversion gain is $\frac{q}{C_f}$ V/electron

- Now let's find the sensor voltage swing v_s

  The minimum output voltage occurs when $Q_{sig} = 0$ and we obtain

  $$v_{omin} = v_{REF}$$

  The maximum output voltage occurs when the voltage on the diode reaches ground, which gives

  $$v_{omax} = v_{REF} + \frac{C_D}{C_f} v_{REF},$$

  provided that v_{omax} does not exceed the opamp maximum output voltage v_{Sat} (in this case $v_{omax} = v_{Sat}$)

  Thus the sensor voltage swing

  $$v_s = \min \left\{ \frac{C_D}{C_f} v_{REF},\, v_{Sat} - v_{REF} \right\}$$

- Note: Since the CTIA can be designed to have very high linearity, the output voltage (at the column) is quite linear in illumination (F_0) (this is not the case in APS as we shall see)

PPS Readout Speed

- Row readout is performed in two stages; first the row is transferred to the column capacitors, then the column decoder/multiplexer is used to serially read out the pixel values
- Row transfer time t_{row} is the time from Word going high to the time v_o is within ϵ of its final value $v_o(\infty)$
- For k bits of resolution we need to choose

$$\epsilon \leq \frac{v_s}{2 \times 2^k} \text{V},$$

  where v_s is the output voltage swing, e.g., for $k = 8$ bits,

$$\epsilon \leq \frac{v_s}{512}$$

- Worst transfer time occurs when $v_o(\infty)$ is maximum, i.e., equal to v_{omax}
- Example: consider a PPS with $n = 256$ rows, $C_D = C_f = 20$fF, and $C_b = n \times 2.6\text{fF} = 0.6656\text{pF}$, find the maximum row transfer time assuming $k = 8$ bits of resolution

To simplify the analysis we assume:

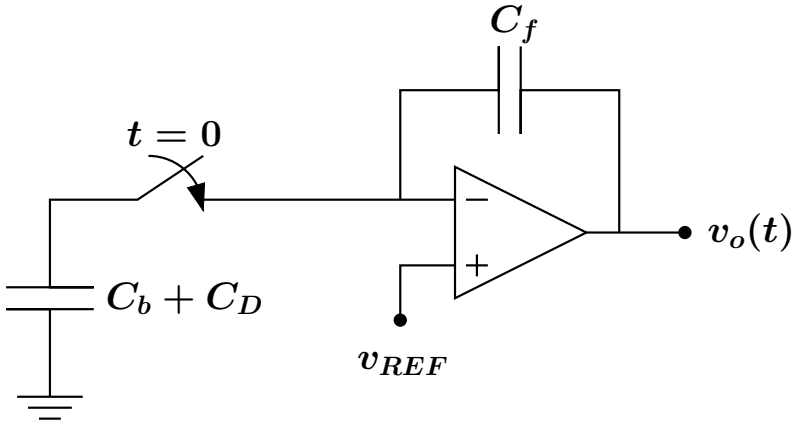
- Single-pole open-loop model for op-amp of charge amplifier, i.e.,

$$\frac{V_o(s)}{V_+(s) - V_-(s)} = A(s) = \frac{A}{1 + (\frac{s}{\omega_o})},$$

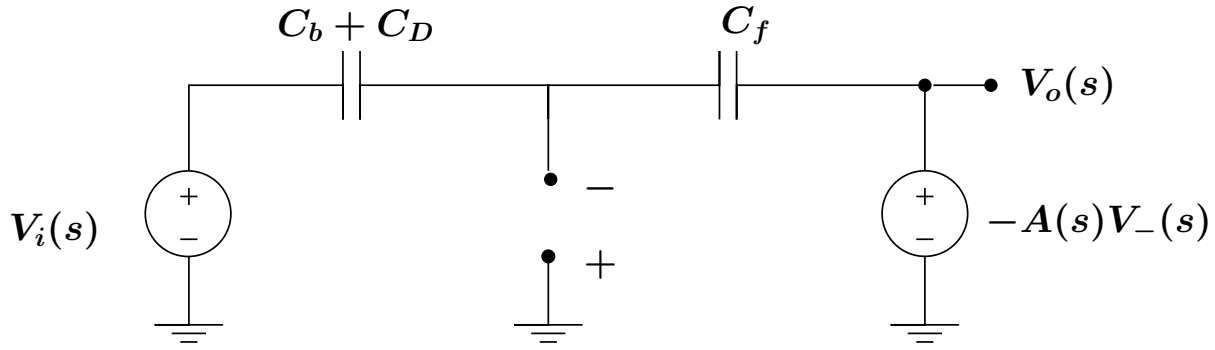
  with dc gain $A = 6 \times 10^4$ and 3dB bandwidth $\omega_o = 100$rad/s

- Access transistor has negligible ON resistance

To find the row transfer time t_{row}, we assume that the charge sharing between C_D and C_b occurs instantaneously (the access transistor treated as a short circuit) and use the equivalent circuit



To find the transfer time we substitute the single-pole opamp model to get



The transfer function is

$$\frac{V_o(s)}{V_i(s)} \approx -\frac{C_b + C_D}{C_f} \cdot \frac{1}{1 + \frac{s(C_b+C_D+C_f)}{A\omega_o C_f}}$$

Thus the circuit time constant is

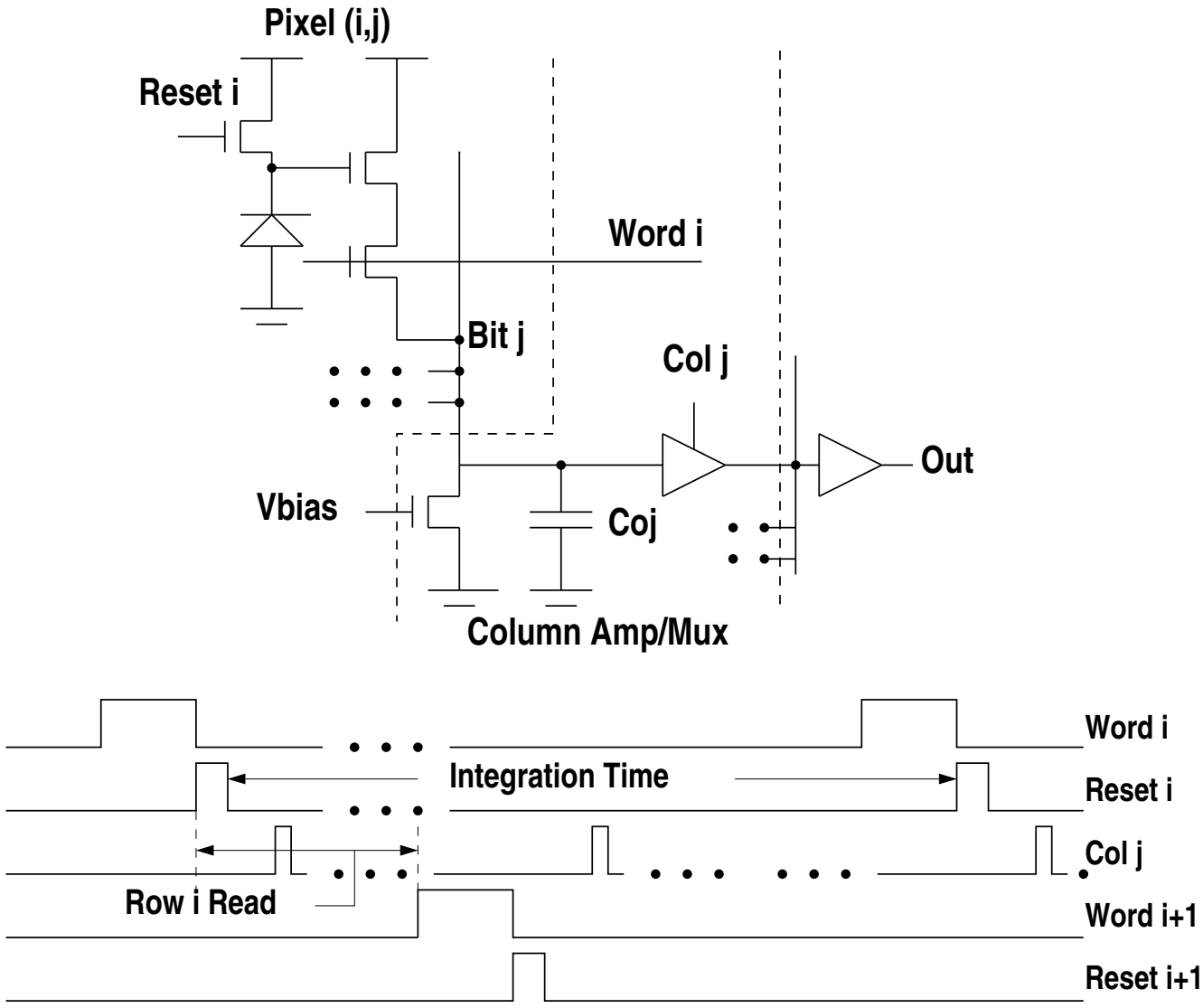
$$\tau = \frac{C_b + C_D + C_f}{A\omega_o C_f} = 5.88\mu\text{s},$$

and the worst case transfer time is given by

$$t_{row} = \tau \ln(256 \times 2) = 36.5\mu\text{s}$$

- Note that
  - Row transfer time increases almost linearly with C_b (and the number of rows)
  - If we try to achieve higher conversion gain by making C_f small, we increase row transfer time !
  - Readout time can be reduced by increasing the gain-bandwidth product of the opamp ($A\omega_o$), which would increase power consumption

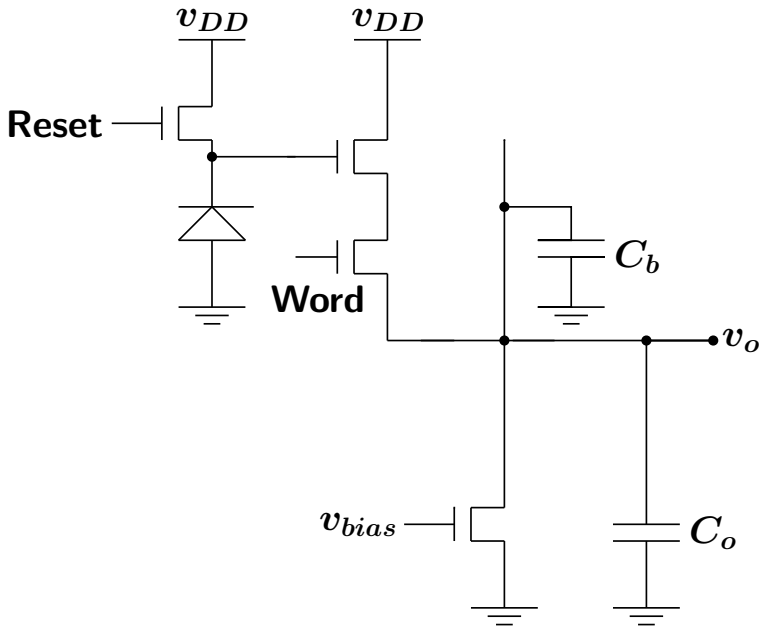
3-T Active Pixel Sensor (APS)



Comments on Operation

- Direct integration is used. Voltage is read out of the pixel
- Output of the photodiode is "buffered" using pixel level follower amplifier — reading is non-destructive and can be much faster than PPS
- Each row has a separate reset (used after reading)
- The photodiode reset voltage v_D depends on the type of reset used:
  - *Soft reset*: The reset gate is set to v_{DD} and $v_D = v_{DD} - v_{TR}$, where v_{TR} is the reset transistor threshold voltage (including body effect)
  - *Hard reset*: The reset gate is $> v_{DD} + v_{TR}$ and $v_D = v_{DD}$
- By setting the voltage on the reset gate $v_{Reset} \geq v_{TR}$ during integration (instead of ground), blooming can be controlled (reset transistor doubles as an anti-blooming device)
- Except for eliminating the charge amplifier, the column amplifier and decoder are identical to PPS

APS Charge to Output Voltage Transfer Function



- Assuming charge Q_{sig} is accumulated on the photodiode at the end of integration, soft reset is used, and ignoring the voltage drop across the access transistor, then in steady state, the output voltage

$$\begin{aligned} v_o &= v_D - \frac{qQ_{sig}}{C_D} - v_{GSF} \\ &= (v_{DD} - v_{TR}) - \frac{qQ_{sig}}{C_D} - v_{GSF}, \end{aligned}$$

where v_{GSF} is the follower transistor gate to source voltage and

The sensor conversion gain is thus $\frac{q}{C_D}\mu$V/electron

- Now, let's find the voltage swing v_s

  To keep the bias transistor in saturation we choose

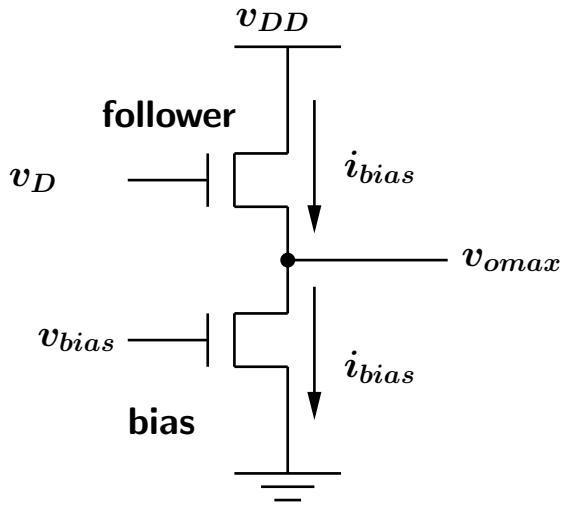
$$v_{omin} = v_{bias} - v_{TB},$$

  where v_{TB} is the bias transistor threshold voltage

  The maximum output voltage occurs when $Q_{sig} = 0$, thus

$$v_{omax} = v_{DD} - v_{TR} - v_{GSF}$$

- To find v_{GSF} consider the circuit (in steady state) (i_{bias} is column amp bias current)



Assuming the static first order MOS transistor model, we obtain

$$i_{bias} = \frac{k_n}{2} \cdot \frac{W_F}{L_F}(v_{GSF} - v_{TF})^2,$$

where W_F and L_F are the follower transistor width and length, k_n is its transconductance parameter (A/V^2), and v_{TF} is its threshold voltage
Thus

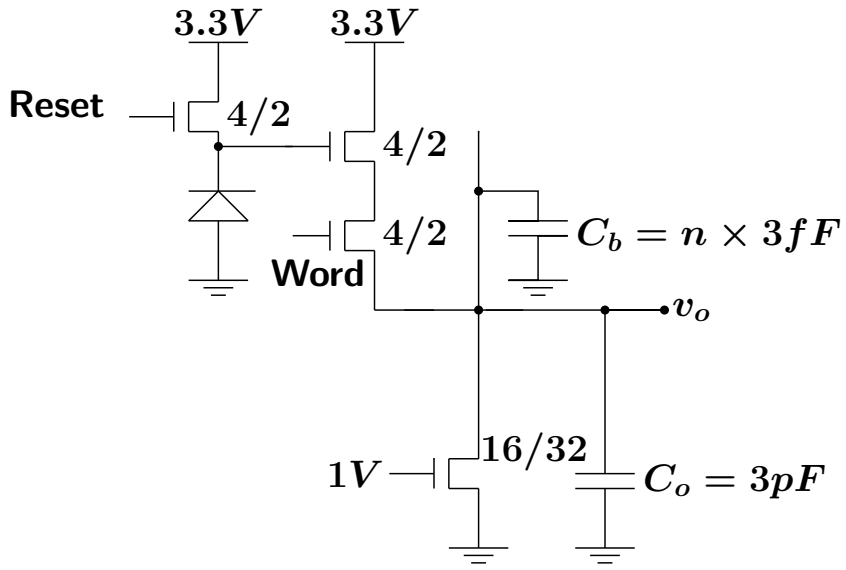
$$v_{GSF} = v_{TF} + \sqrt{\frac{2L_F}{k_n W_F} i_{bias}}$$

Thus the voltage swing is given by

$$v_s = v_{DD} - v_{TR} - v_{GSF} - v_{bias} + v_{TB}$$

- Remarks:
  - The available well capacity $qQ_{max} = v_D \times C_D$ cannot be fully utilized, since v_{omin} is achieved before the diode voltage drops to ground
  - The column output voltage is quite nonlinear in illumination (F_0)
    - The collected charge is converted to voltage using the diode capacitance
    - The follower nonlinearity due to backgate effect (body tied to ground) and channel length modulation

- Example: Consider an APS implemented in the 0.5μ CMOS technology described in Handout 4 with $n = 256$ rows, $v_{TF} = 0.9$V, $v_{TR} = 1.1$V, $v_{TB} = 0.8$V, and the parameters shown in the figure



Let's compute the output voltage swing v_s. The minimum output voltage $v_{omin} = v_{bias} - v_{TB} = 0.2$V
The bias current using $k_n = 188\mu$A/V^2 is $i_{bias} = 1.88\mu$A, and the maximum output voltage is

$$v_{omax} = v_{DD} - v_{TR} - v_{GSF} = 3.3 - 1.1 - 1.0 = 1.2\text{V}$$

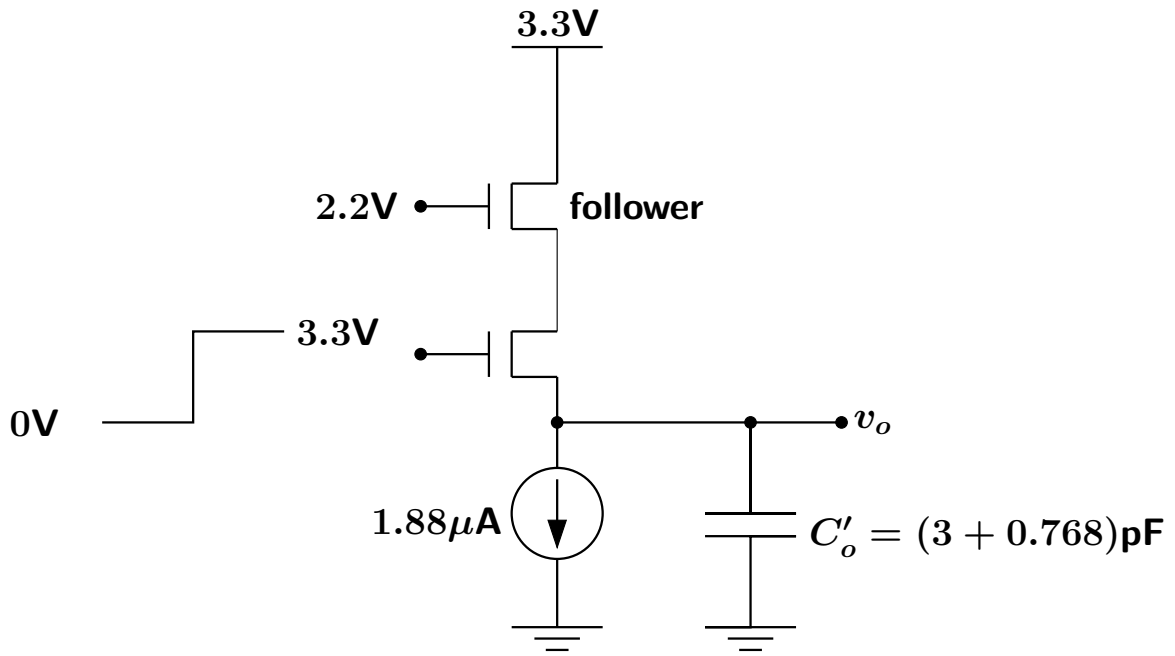
Thus the voltage swing

$$v_s = 1.0\text{V}$$

APS Readout Speed

- Readout time for a row is the sum of the time to transfer the row to the column capacitors and the time to read out the pixel values via the column multiplexer (column readout time)
- APS column readout time (and not row transfer time) is the real performance limiter if the sensor is read out serially (row readout time becomes the limiting factor for parallel/on-chip readout)
- Let's find the row transfer time assuming $k = 8$ bits of resolution for the example APS

  To find the worst case row transfer time, we use the following equivalent circuit



Define the *row transfer time* t_{row} as the time from the access transistor turning on to the output voltage v_o reaching to within half a bit of its steady state value, i.e.,

$$v_o(t_{row}) \geq v_o(\infty) - \frac{v_s}{2^{k+1}}$$

By KCL

$$1.88 \times 10^{-6} + C'_o \frac{dv_o}{dt} = 188 \times 10^{-6} \times (1.3 - v_o)^2$$

This differential equation can be solved analytically by separation of variables, and we obtain

$$t_{row} = \frac{C'_o}{2\sqrt{k_n i_{bias}}} \ln\left(\frac{(\beta+\rho)(\alpha-\rho)}{(\beta-\rho)(\alpha+\rho)}\right),$$

where

$$\begin{aligned}
\rho &= \sqrt{\frac{i_{bias}}{k_n}} \\
\alpha &= v_o(\infty) + \rho - v_o(0) \\
\beta &= v_o(\infty) + \rho - v_o(t_{row})
\end{aligned}$$

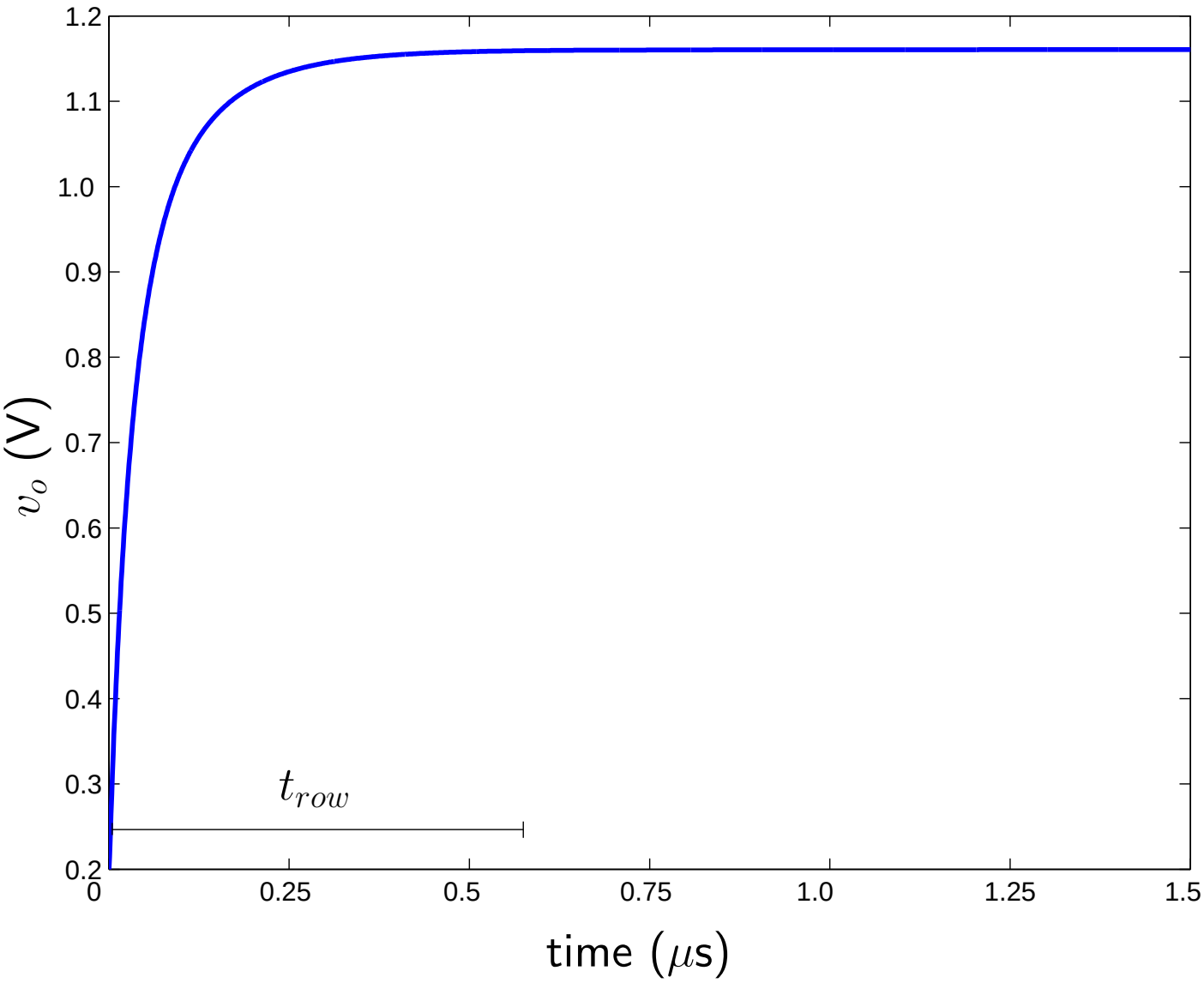
Using the previous parameter values and assuming $k = 8$bits, we have

- $v_o(0) = v_{omin} = 0.2$V
- $v_o(\infty) = v_{omax} = 1.2$V
- $v_o(t_{row}) = 1.198$V

Substituting, we obtain

$$t_{row} = 444 \text{ ns}$$

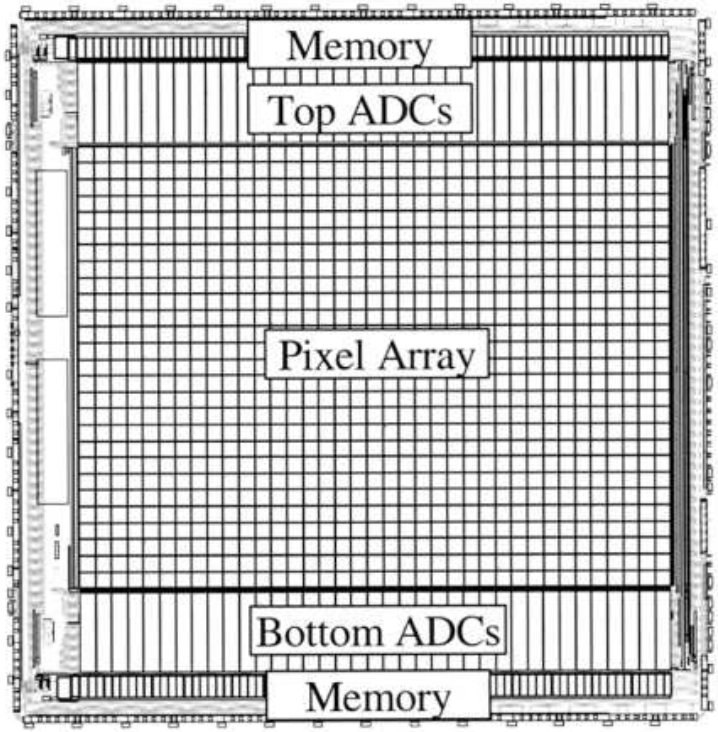
APS Readout Speed from HSPICE Simulation



Comments on APS Readout Speed

- The row transfer time increases linearly with C_b (same as PPS)
- It decreases with bias current i_{bias}. Reducing bias current also increases voltage swing and reduces power consumption
- It is considerably shorter than PPS. Our estimate, however, is somewhat optimistic as you can see from the HSPICE simulations, which gives around 570ns. This is because we made several simplifying assumptions including ignoring access transistor resistance, transistor channel modulation, and assuming quadratic current law. The effects of these nonidealities are discussed in [Salama' 03]
- The analysis we performed assumed that the bitline is reset after each row read. If the bitline is not reset and is allowed to be discharged through the bias current, the row transfer time becomes dominated by the discharge time
- PPS can be made as fast as APS by using a faster charge amplifier. However, readout power consumption becomes much higher than APS

4.1-Mpixel APS Example

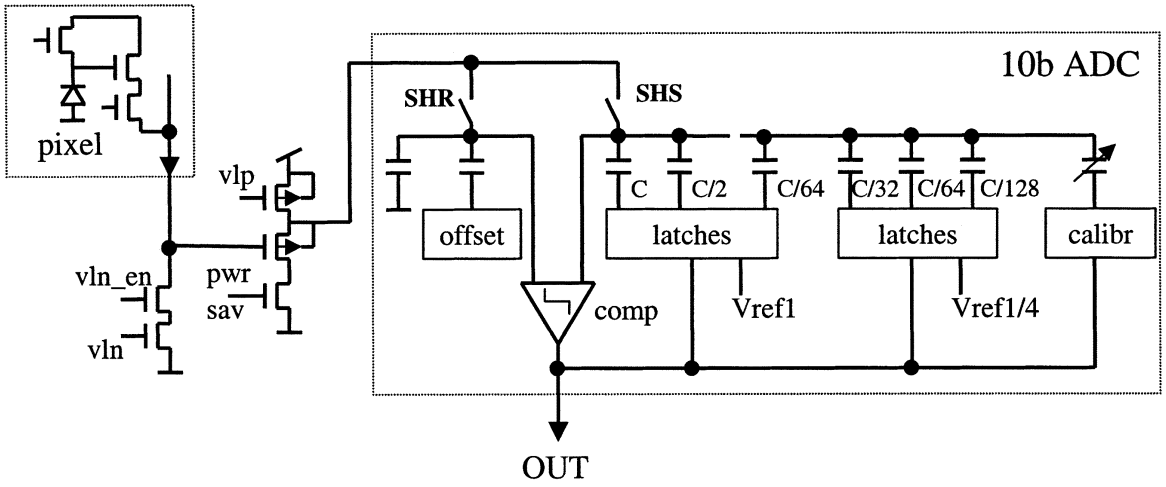


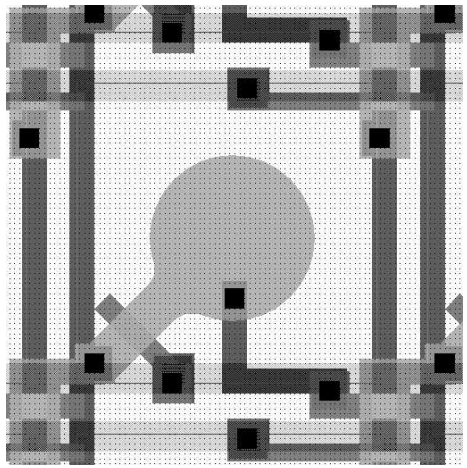
- 0.35 μm 2P3M process
- 2352(H)$\times$1728(V) pixels
- 240 Frames/sec
- 7μm $\times$ 7μm pixel
- 10 bit column ADC
- Conversion gain: 39 μV/e-
- Sensitivity @550nm: 2.5 V/Lux.sec

Krymski et al. "A High-Speed, 240-Frames/s, 4.1-Mpixel CMOS Sensor," IEEE Transactions on Electron Devices, vol. 50, pp. 130-135, January 2003

4.1-Mpixel APS Circuit and Layout

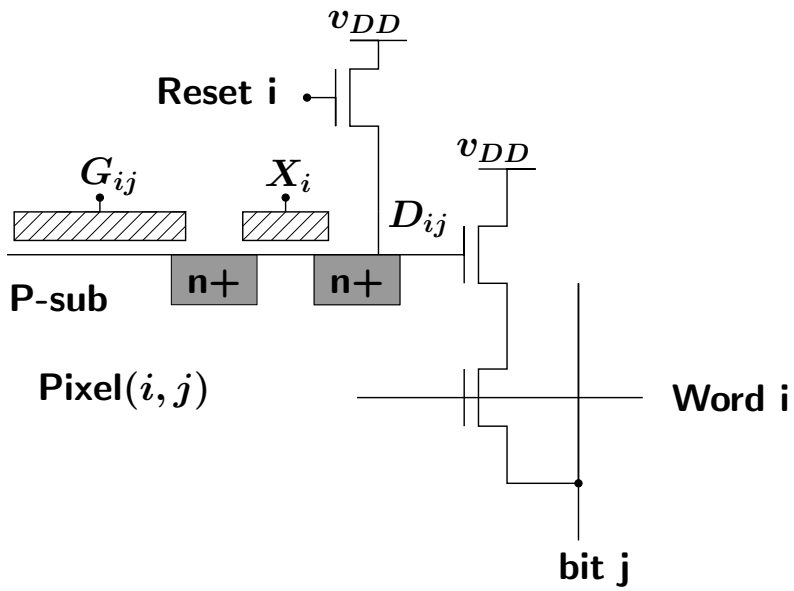
- APS readout circuit sampled and directly converted by per-column successive approximation ADC

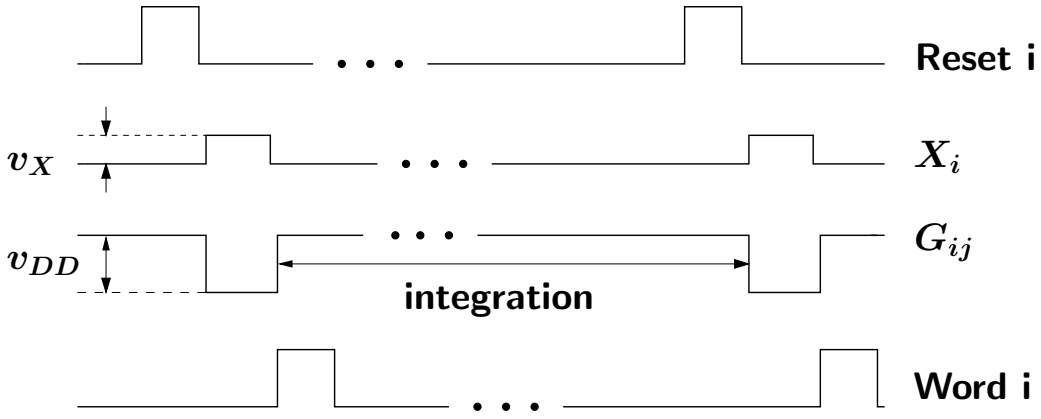




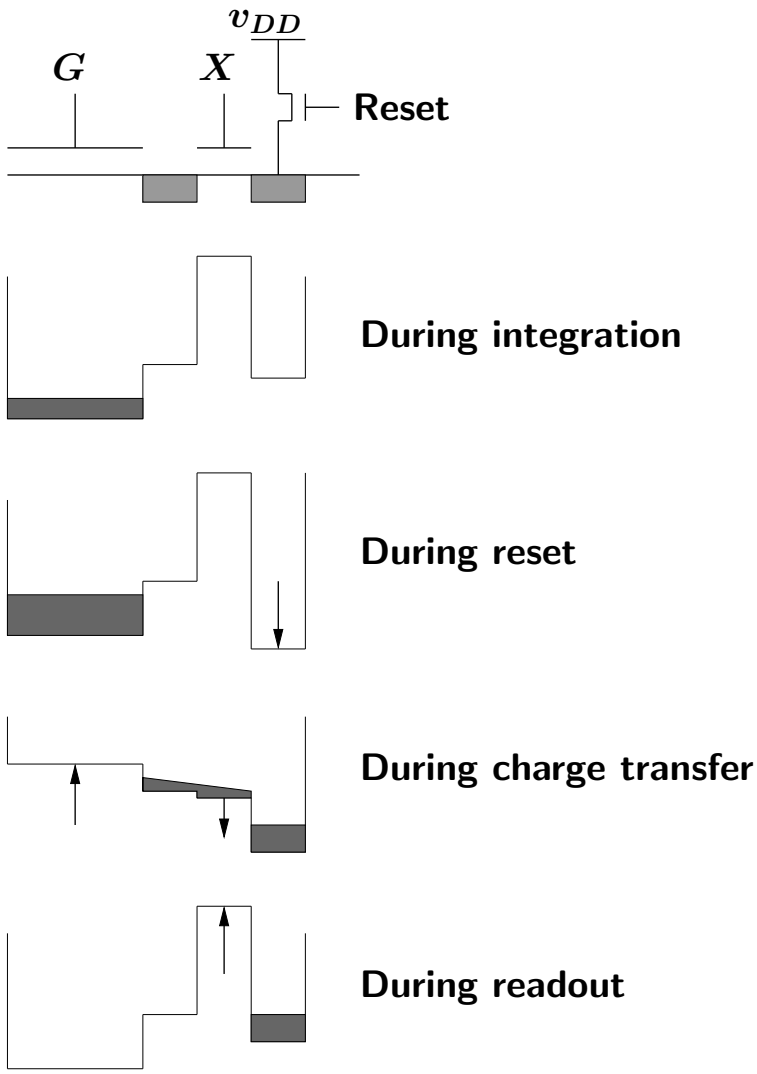
Krymski et al. "A High-Speed, 240-Frames/s, 4.1-Mpixel CMOS Sensor," IEEE Transactions on Electron Devices, vol. 50, pp. 130-135, January 2003

CMOS Photogate APS





Potential Well Diagram for Photogate APS



Comments on Operation

- Before reading a row
  - Floating node D_{ij} is reset
  - To transfer the accumulated charge on the photogate to the floating node D_{ij}, the transfer gate is turned to an intermediate voltage $v_X \leq \frac{v_{DD}}{2}$V and the gate voltage is lowered to 0V (CCD like operation)
- The transfer gate can also be kept at a constant intermediate voltage throughout to avoid blooming and to reduce switching noise
- Well capacity is determined by the voltage swing on the floating node and its capacitance C_d
- Column and chip circuits are identical to photodiode APS and the rest of readout operation is identical to photodiode APS
- The subcircuit consisting of the transfer gate, reset transistor and follower transistor is the same as the CCD output amplifier circuit

Advantages and Disadvantages of Photogate

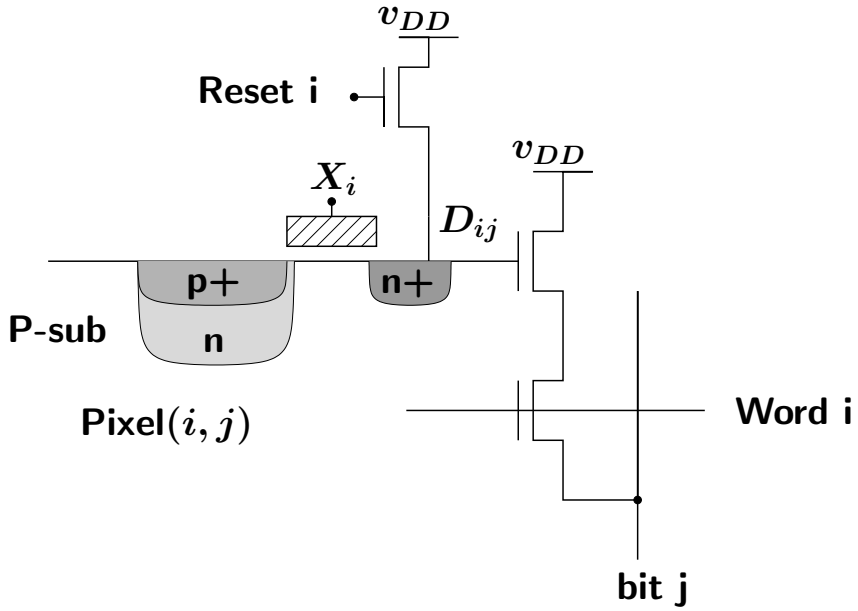
Advantages:

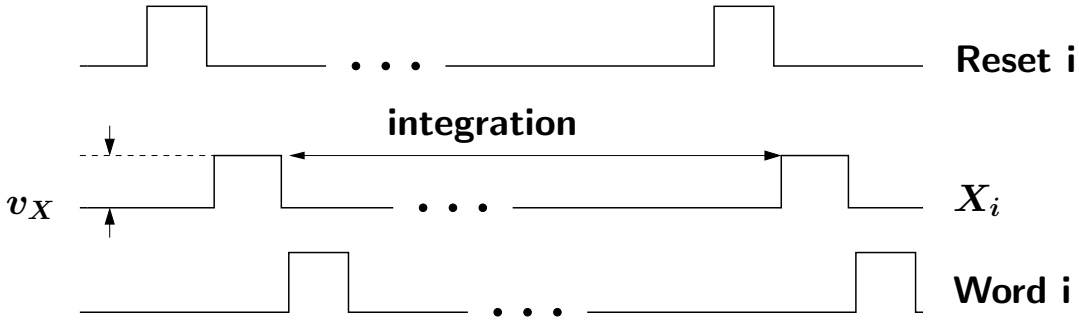
- Conversion gain $\frac{q}{C_d}$ is independent of photodetector, can achieve higher conversion gain than photodiode APS (lower QE, however)
- C_d very useful, can be used for
  - Providing "snap shot" operation by globally turning on all transfer gates (readout still performed one row at a time)
  - Performing true *correlated double sampling* (CDS)

Disadvantages:

- More devices (larger pixel or lower fill factor than photodiode)
- Lower QE, poor blue response
- Incomplete charge transfer due to the n+ drain of the transfer gate (we are assuming a standard CMOS process here)

Pinned Diode APS





Comments on Operation

- Operation similar to photogate APS
- Before reading a row
  - Floating node D_{ij} is reset to v_{DD}
  - The transfer gate is turned on to transfer the accumulated charge to the floating node D_{ij}
- "snap-shot" operation can be performed by globally turning on all transfer gates (readout performed one row at a time)
- Well capacity is determined by the voltage swing on the floating node and its capacitance C_d

Advantages and Disadvantages of Pinned Photodiode

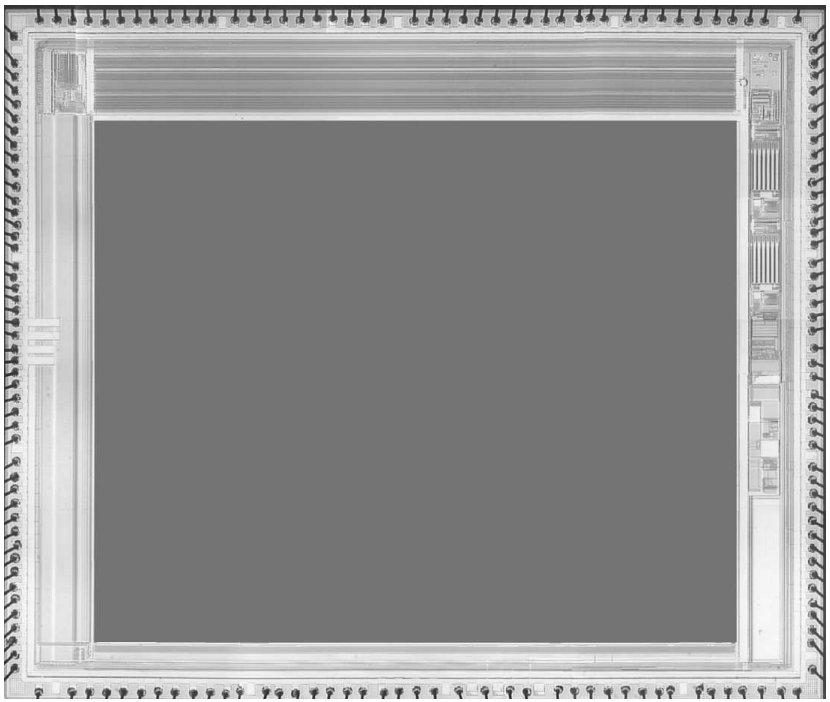
Advantages:

- Conversion gain $\frac{q}{C_d}$ is independent of photodiode capacitance and can be tailored for application (e.g., low-light sensitivity)
- Allows for true *correlated double sampling* (CDS)
- High QE in blue range
- Typically much lower dark current than standard nwell/psub diode
- Isolated floating diffusion allows for transistor sharing

Disadvantages:

- Requires significant modifications to standard CMOS process
- Higher reset voltage required for complete transfer
- Larger pixel required unless transistors are shared

1.3-Mpixel Pinned Diode APS Example

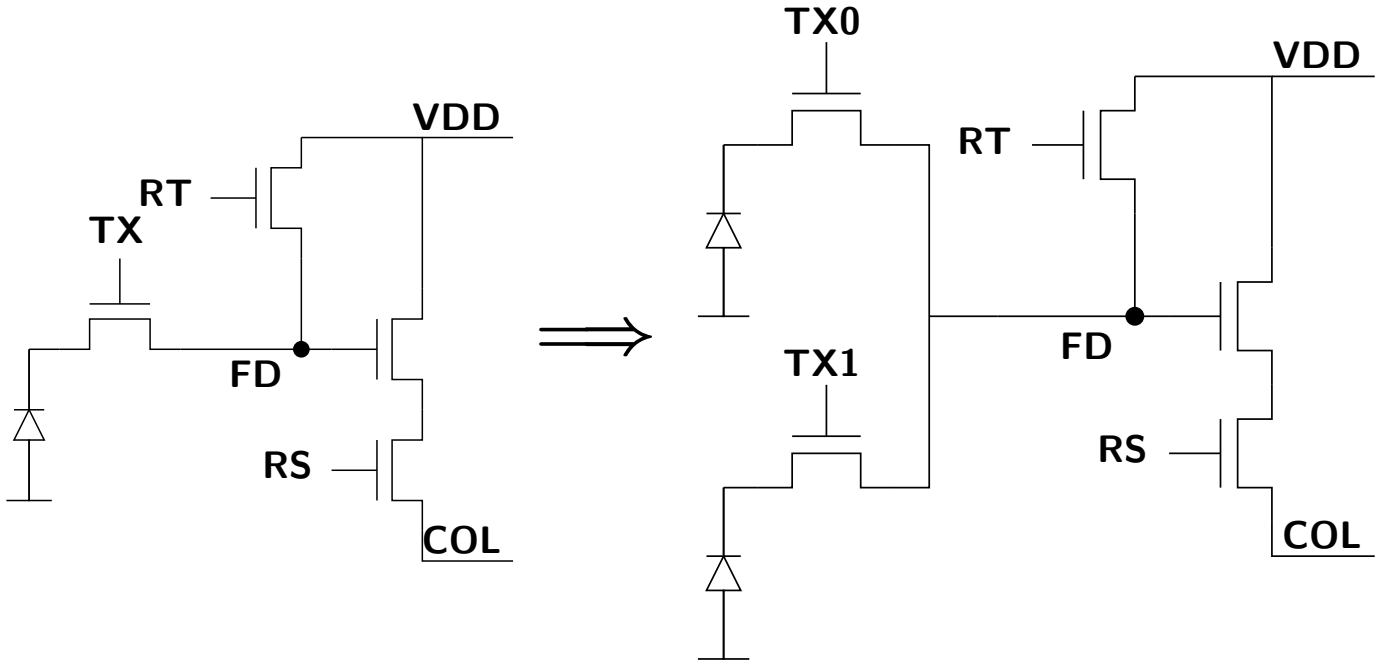


- 0.35 μm 1P3M CMOS process
- 1280(H)$\times$1024(V) pixels
- 30 Frames/sec
- 5.6 μm x 5.6 μm pixel
- 11 bit ADC
- Conversion gain: 26 μV/e-
- Sensitivity @550nm: 1.4 V/Lux-sec

Findlater et al. "SXGA Pinned Photodiode CMOS Image Sensor in 0.35μm Technology," IEEE International Solid-State Circuits Conference, 12.4, 2003

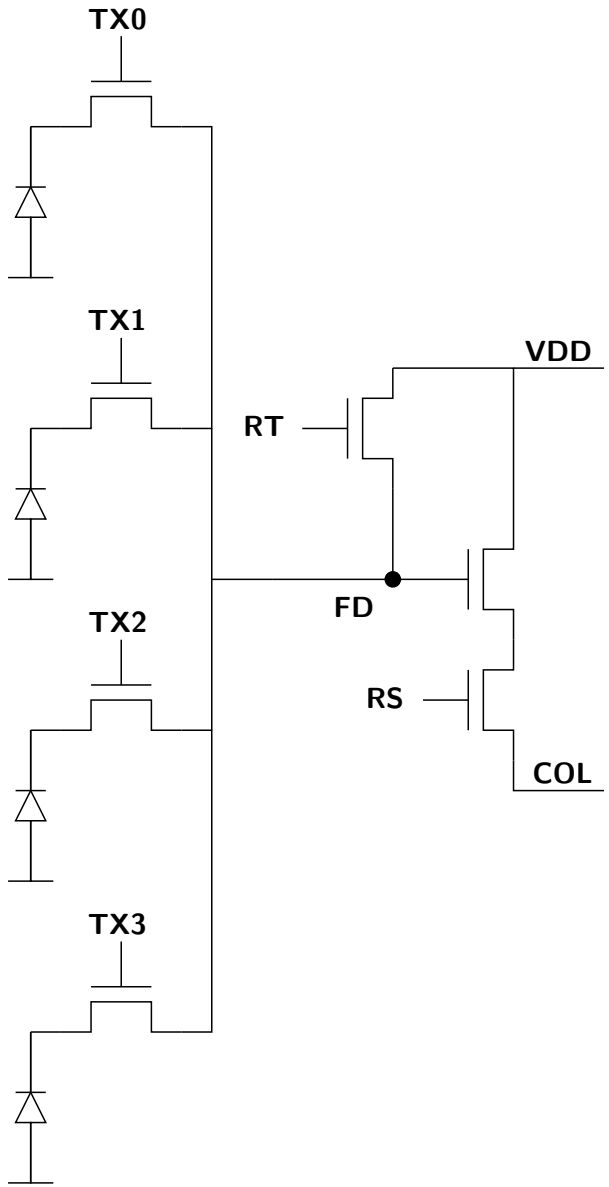
Multiplexed Pinned Diode APS

- Charge transfer devices may share readout transistors
  - The floating diffusion (FD) is common to multiple transfer gates
  - Less transistors per pixel – increased fill factor

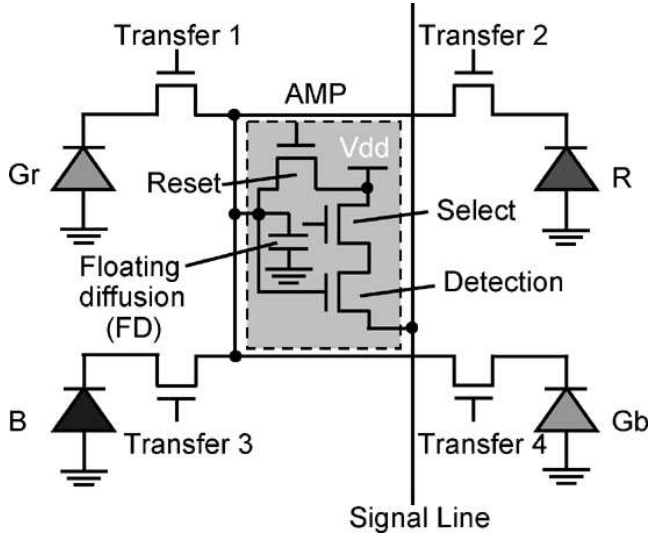


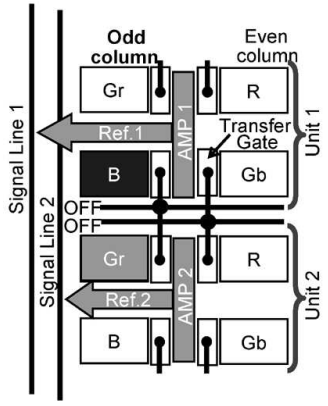
- Sharing is not possible with 3T type APS structure

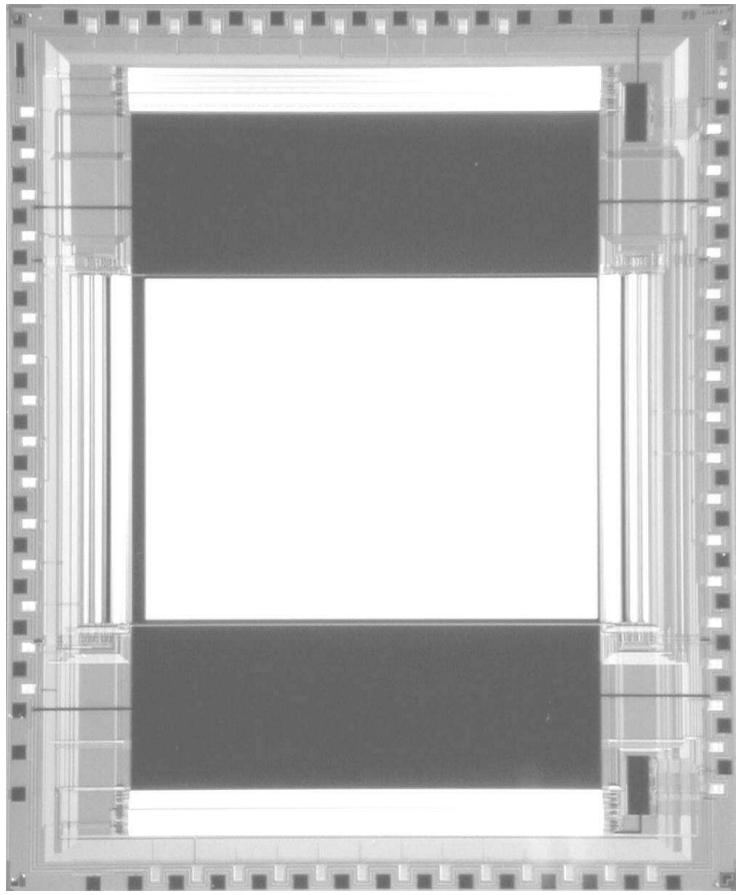
1.75 Transistors Per Pixel



1.75T Imager Example

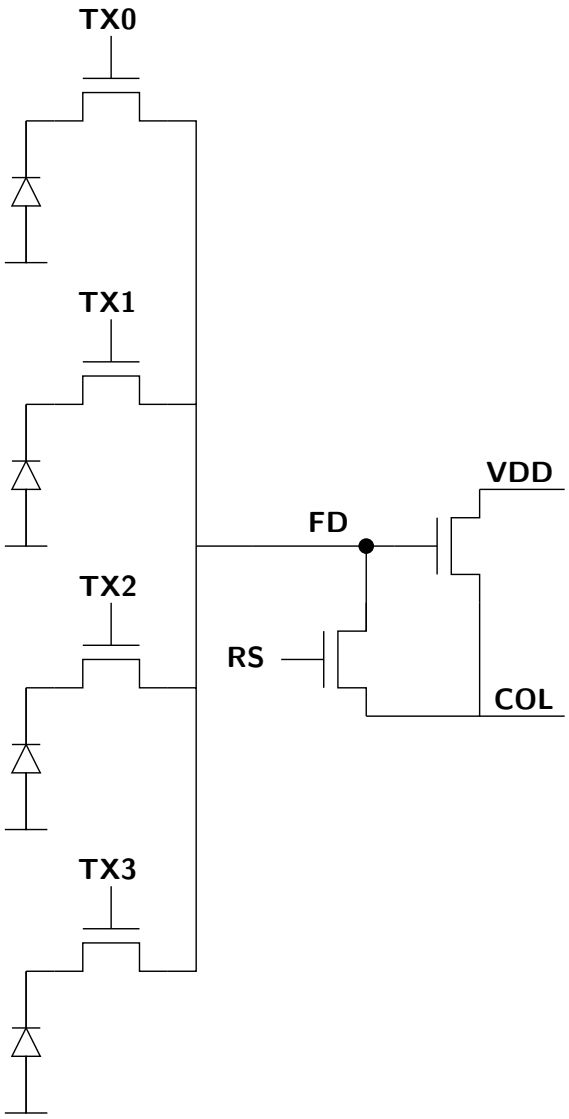


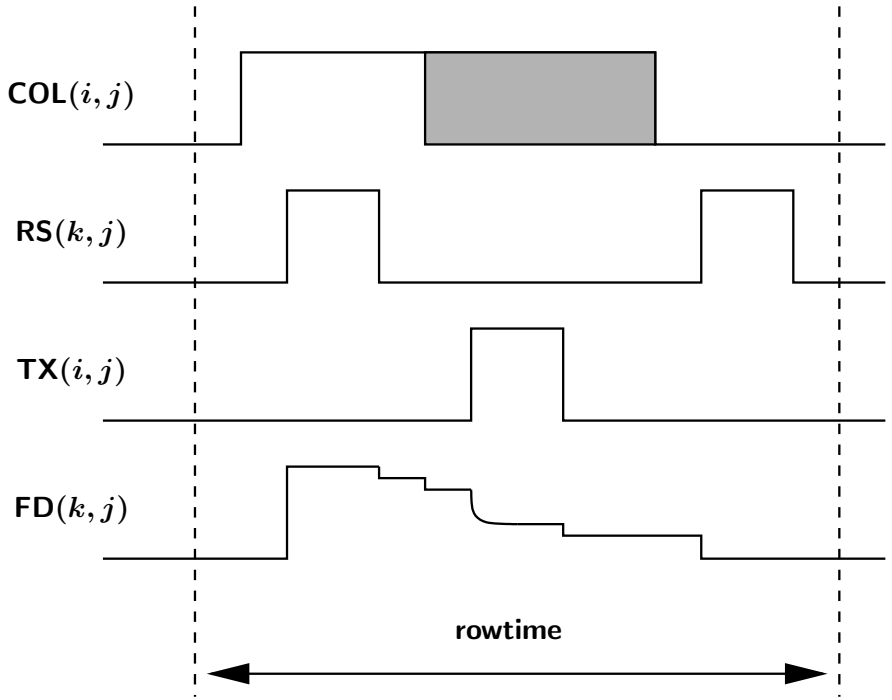




Mori et al. "1/4-Inch 2-Mpixel MOS Image Sensor With 1.75 Transistors/Pixel," IEEE Journal of Solid-State Circuits, vol. 39, pp 2426-2430, December 2004

1.5 Transistors Per Pixel

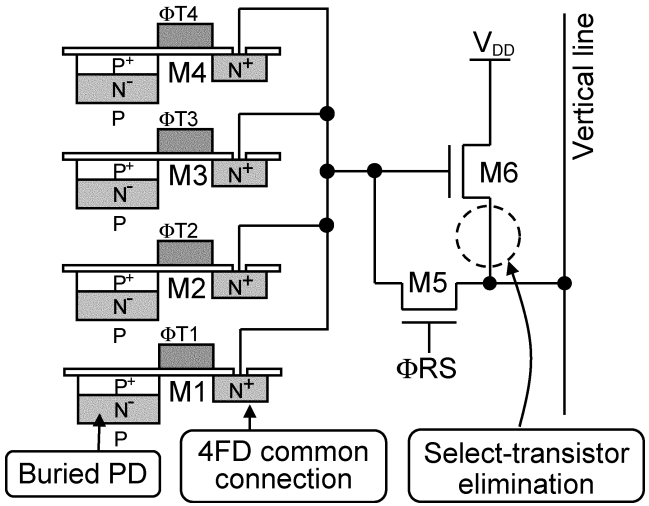


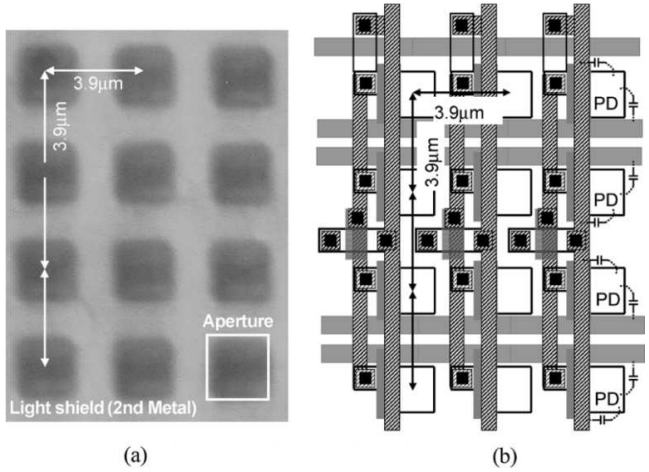


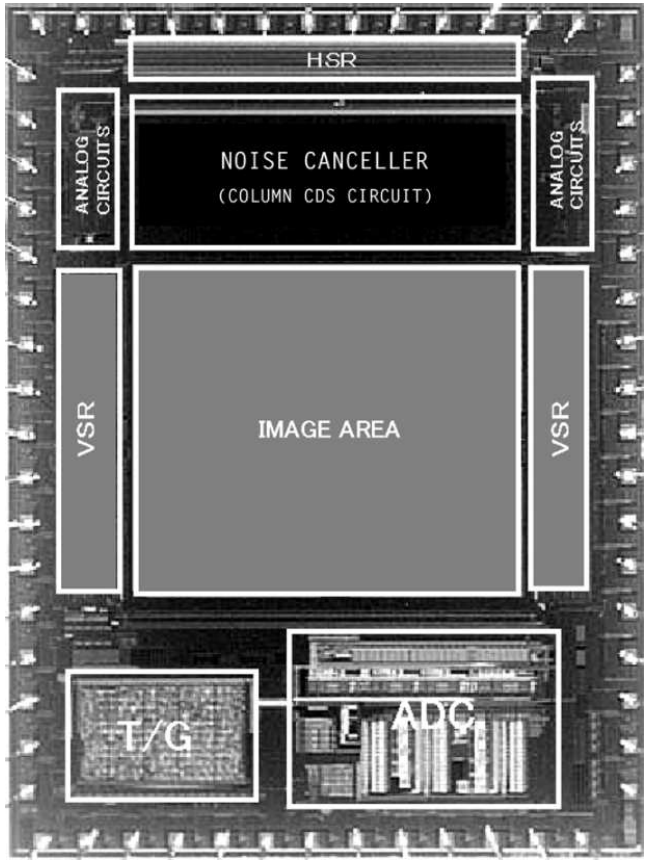
Comments on Operation

- Operation made possible by the inherent isolation between floating diffusion and photodiode during integration
- Works through "winner-take-all" nature of source follower:
    1. Reset the diffusion by pulling column line high and turning RS on
    2. Turn TX on to transfer, then read out
    3. Turn TX off, then RS on, while pulling column line low
        - This sets the floating diffusion low, which disables the source follower from acting on the column line until next selection

1.5T Imager Example







Takahashi et al. "A 3.9-μm Pixel Pitch VGA Format 10-b Digital Output Cmos Image Sensor With 1.5 Transistor/Pixel," IEEE Journal of Solid-State Circuits, vol. 39, pp 2417-2425, December 2004

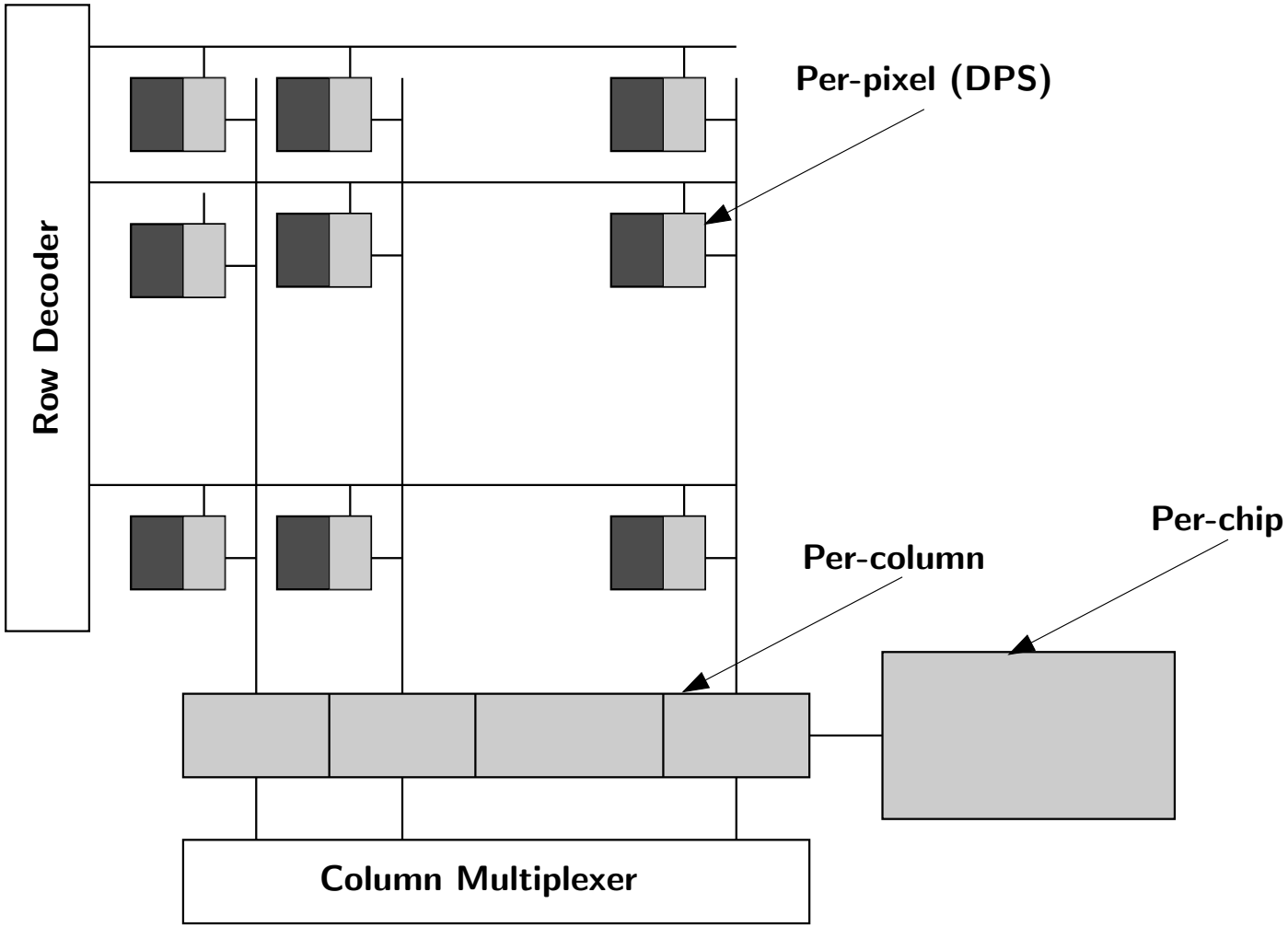
Disadvantages of Multiplexing

- Requires the use of pinned diode (or photogate)
- Longer array readout
- Introduces additional pixel nonuniformity due to layout asymmetry
    - Less of a problem when color filter array is used (high uniformity among groups of 2×2 pixels)
- More complex row readout operation

Digital Pixel Sensor (DPS)

- An important trend in digital imaging system design is the integration of CMOS image sensor with analog and digital processing down to the pixel level
- Such integration saves power and reduces system size
- More interestingly, it provides the ability to rethink the imaging system architecture
- An important example is where and how to perform the A/D conversion
- DPS integrates an ADC per pixel

ADC Integration Options



Per-Level ADC (DPS)

- Each pixel (or group of pixels) has an ADC, all ADCs operate in parallel
- Advantages:
  - High speed readout due to parallel conversion and digital readout
  - High signal swing
  - Eliminates column temporal noise and FPN (more on this later)
  - Process scalable – low speed ADCs using simple circuits
- Disadvantage:
  - Large pixel size (existing ADC implementations not feasible)
  - Limited ADC resolution (because of limited pixel size)
  - Complexity of implementation
- It is possible to perform A/D conversion with *very* few transistors per pixels, and
- Pixel size problem becomes less severe as technology scales

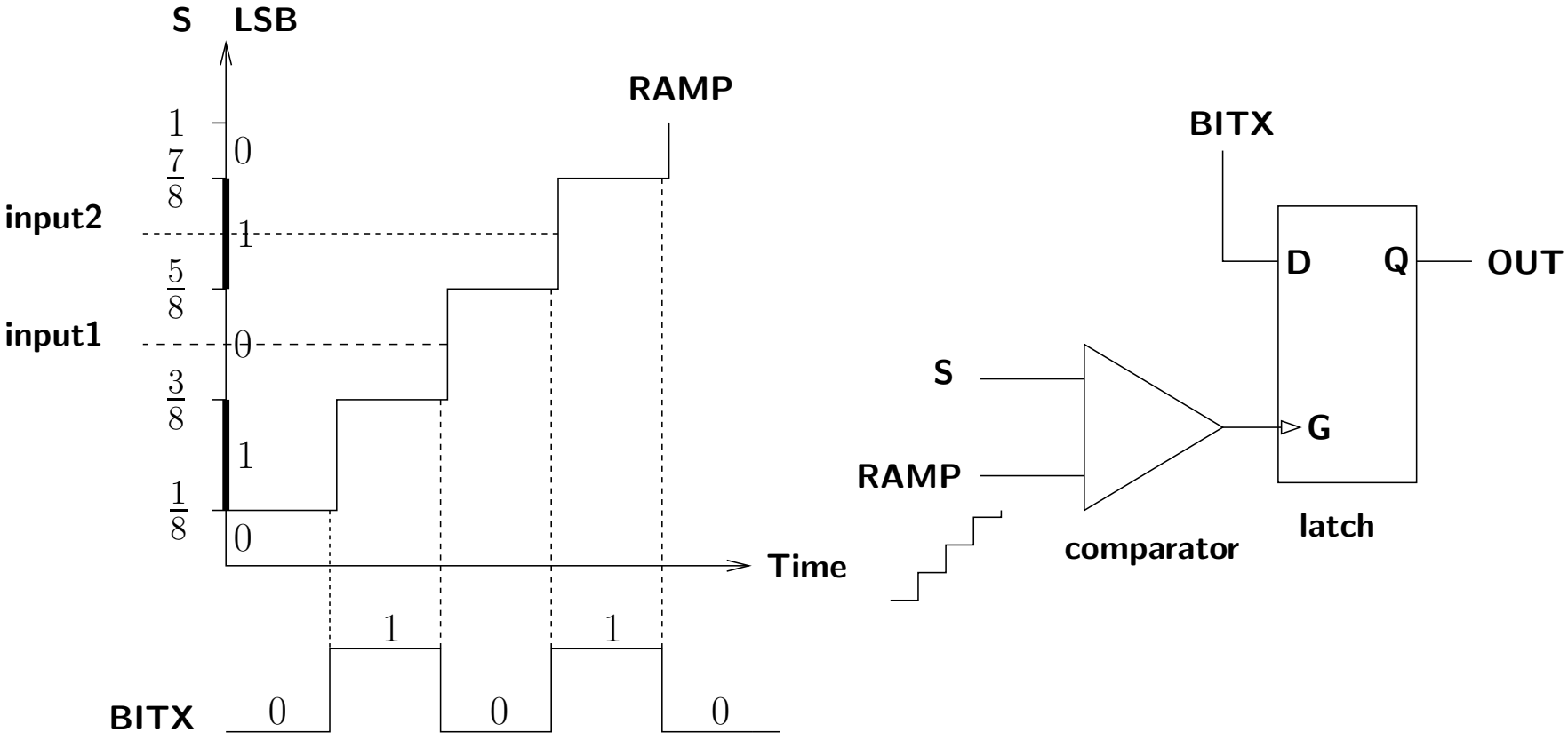
Multi-Channel Bit-Serial (MCBS) ADC [Yang' 99]

- ADC implements a quantization table

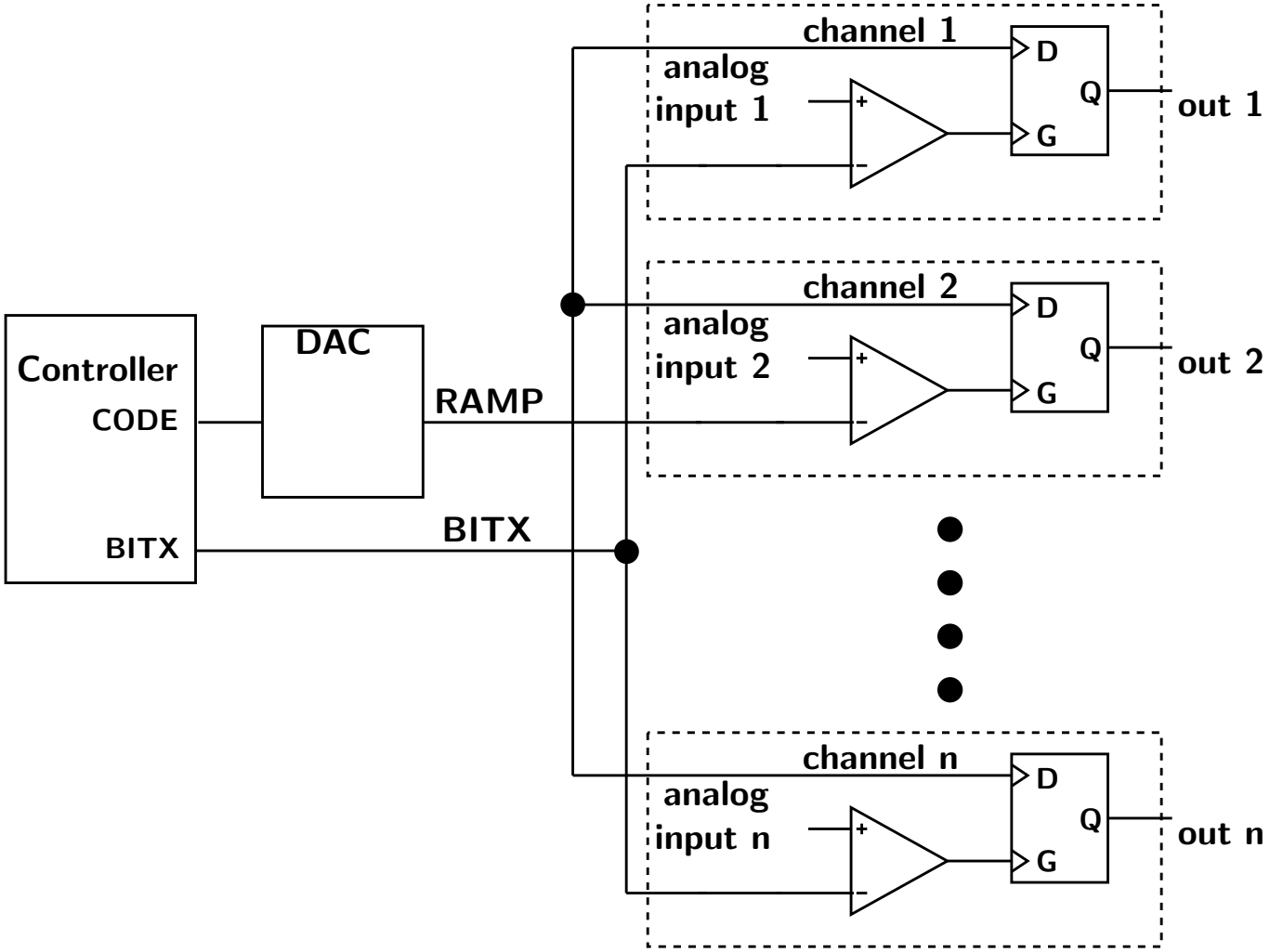
ADC Input	Gray Code
$0 - \frac{1}{8}$	0 0 0
$\frac{1}{8} - \frac{2}{8}$	0 0 1
$\frac{2}{8} - \frac{3}{8}$	0 1 1
$\frac{3}{8} - \frac{4}{8}$	0 1 0
$\frac{4}{8} - \frac{5}{8}$	1 1 0
$\frac{5}{8} - \frac{6}{8}$	1 1 1
$\frac{6}{8} - \frac{7}{8}$	1 0 1
$\frac{7}{8} - 1$	1 0 0

- Key Point: Each output bit can be separately generated (this is how flash ADC performs the conversion)

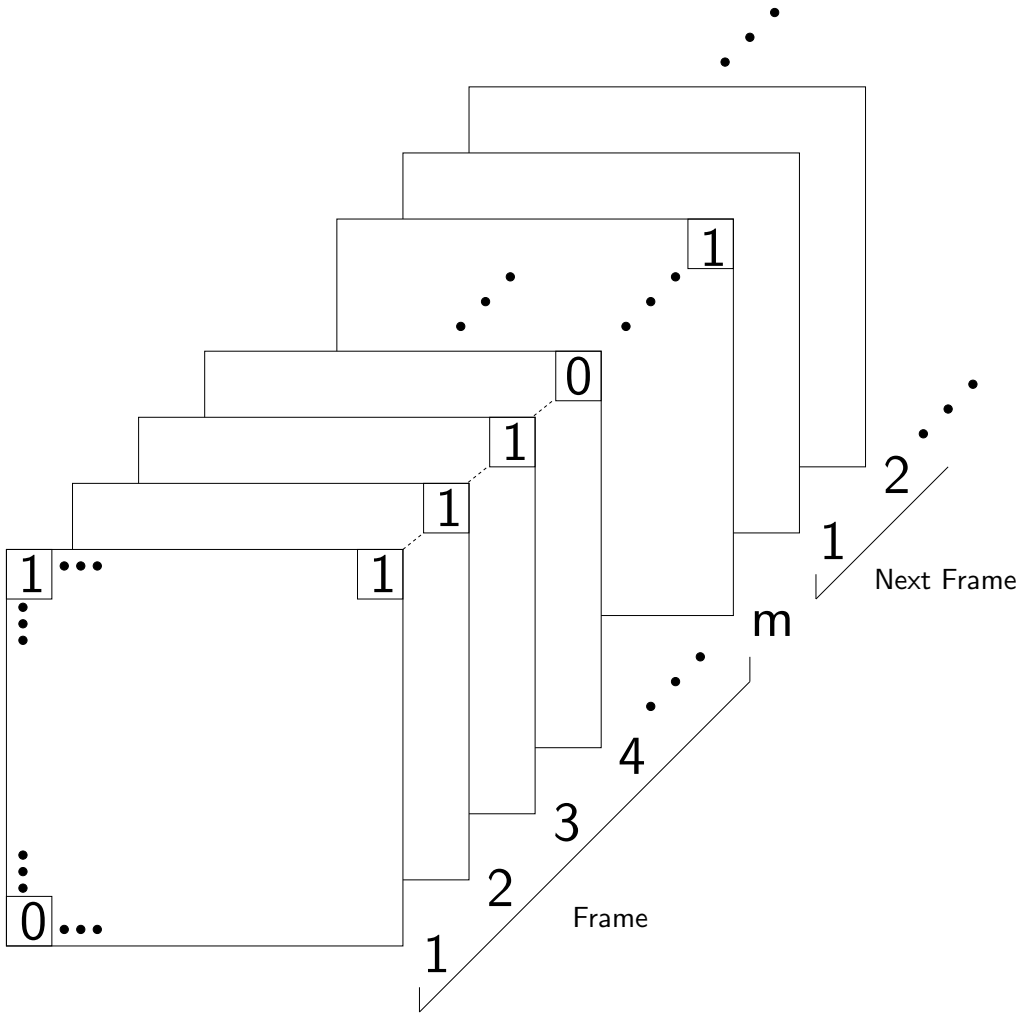
How 1-bit Comparator/Latch Works



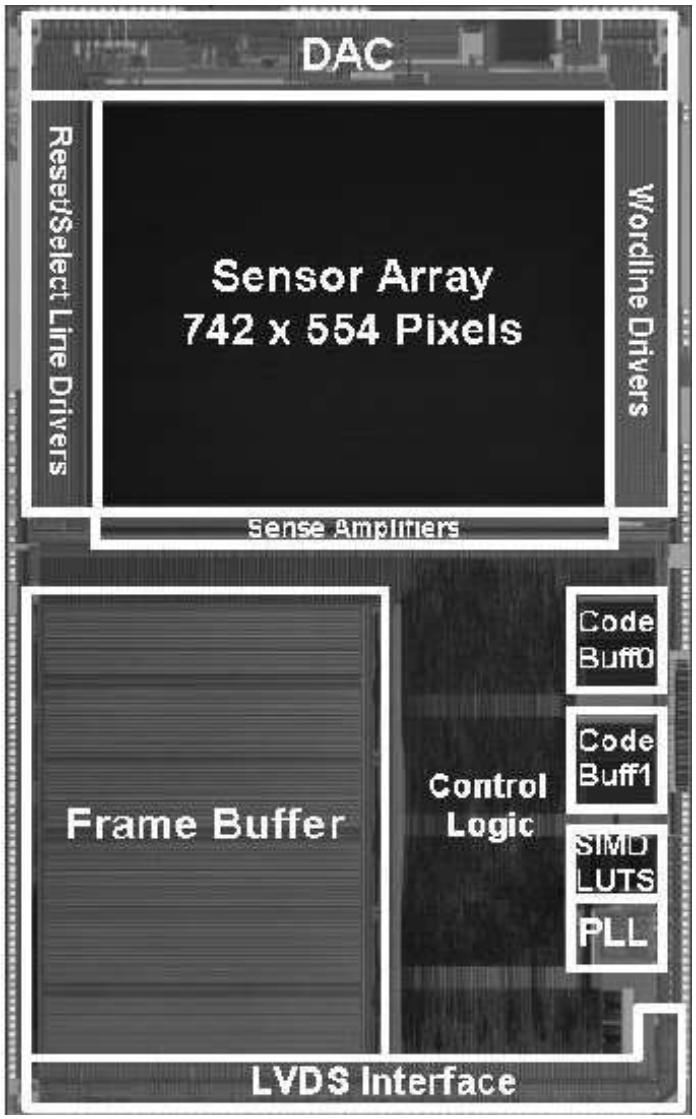
MCBS ADC – Block Diagram



Output Image Format

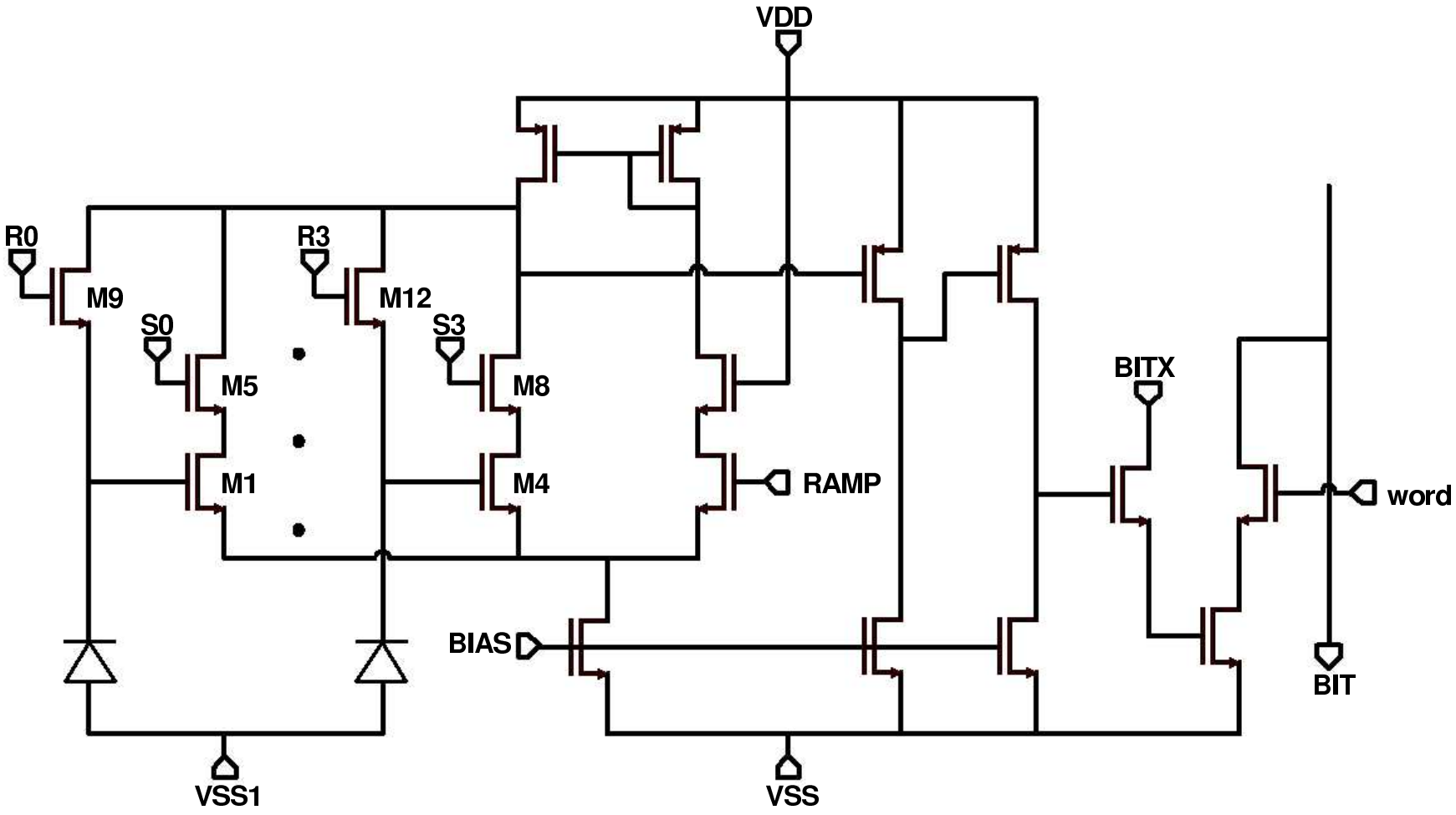


CCTV DPS Chip [Bidermann' 04]

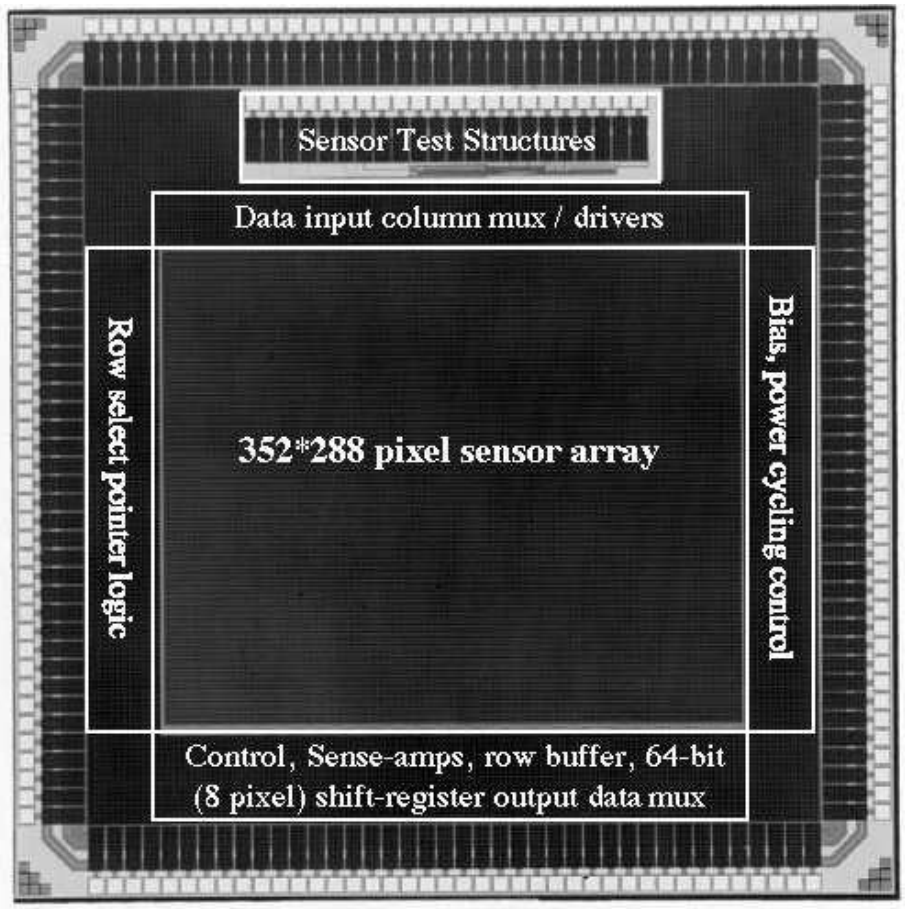


- 0.18μm CMOS technology
- 742×554 pixel array
- Per pixel-quad MCBS ADC
- $7\mu \times 7\mu$ pixels
- 5M-bit frame buffer
- Per-column DSP
- Micro-controller
- 500 frames/sec internal
- 60 frames/sec external
- 14-bit dynamic range

Multiplexed MCBS ADC Pixel Circuit [Bidermann' 04]

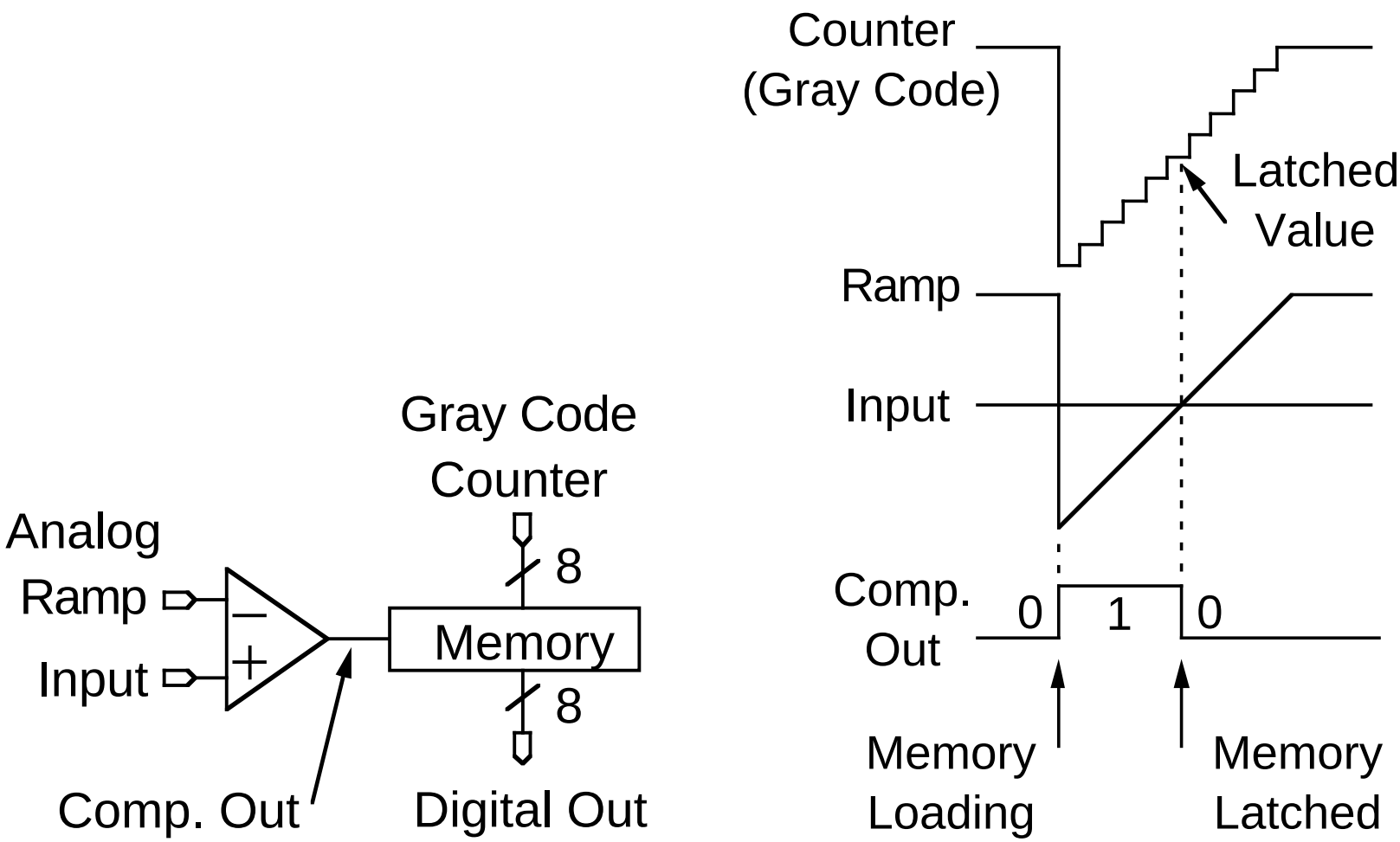


Single-Slope Based DPS [Kleinfelder' 01]

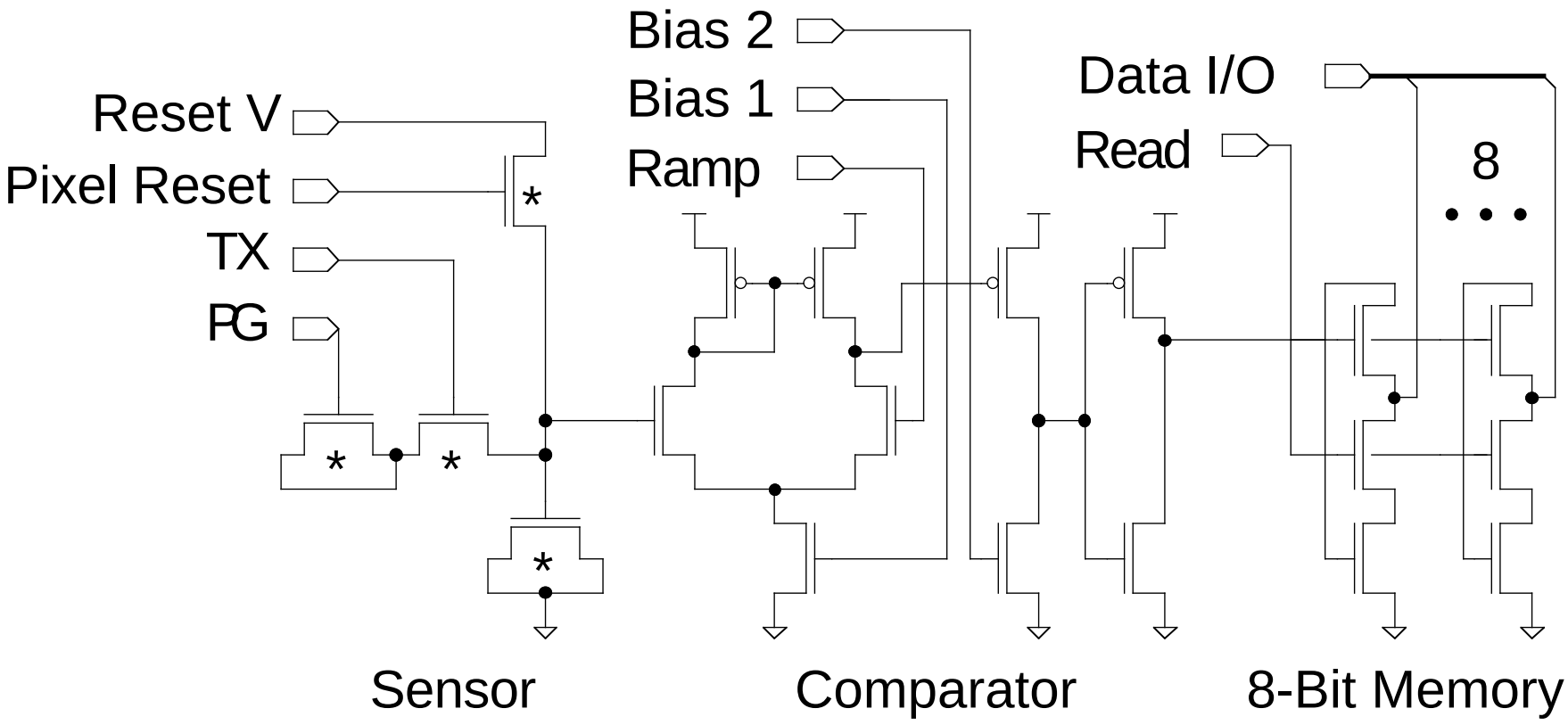


- 0.18μm CMOS technology
- 352×288 pixels (CIF)
- $9.4\mu \times 9.4\mu$ pixels
- 37 transistors/pixel
- 3.8 million transistors
- 8 bit single slope ADC and memory/ pixel
- 64 wide digital output bus at 167 MHz
- $> 10,000$ frames/s continuous imaging

ADC Operation



Pixel Schematic



Summary

- Described several CMOS image sensor architectures:
  - PPS
  - Photodiode APS
  - Photogate APS
  - Pinned-diode APS
  - Multiplexed pinned-diode APS
- Discussed their advantages and disadvantages
- Analyzed PPS and APS readout circuit:
  - Charge to voltage transfer function
  - Voltage swing
  - Readout speed

Architecture Comparsion

	PPS	3T APS	Photogate APS	Pinned-diode APS
Transistors/pixel	1	3	1.5–4	1.5–4
QE of blue	OK	OK	Bad	Very good
Reset	Before readout	After readout	Before readout	Before readout
Shutter	Scrolling	Scrolling	Snap-shot	Snap-shot
Transfer function Linearity	High	Low	Low	Low
Row transfer time	Slow	Fast	Fast	Fast