Lecture Notes 2

Charge-Coupled Devices (CCDs) – Part I

- Basic CCD Operation
- CCD Image Sensor Architectures
- Static and Dynamic Analysis
  - Charge Well Capacity
  - Buried channel CCD
  - Transfer Efficiency
  - Readout Speed

Preliminaries

- Two basic types of image sensors: CCD and CMOS
- Photodetector elements are similar
    - Photodiode
    - Photogate
    - Pinned-diode

  The photodiode and photogate operation were covered in Lecture Notes 1. We discuss the pinned diode in Part II of this lecture notes
- Main difference is the readout "circuitry" / mechanism
    - In CCDs, charge is shifted out
    - In CMOS image sensors, charge or voltage is read out using row and column decoders — similar to a random access memory

- The readout circuits (including in pixel devices) determine the sensor *conversion gain*, which is the output voltage per electron collected by the photodetector, in μV/electron

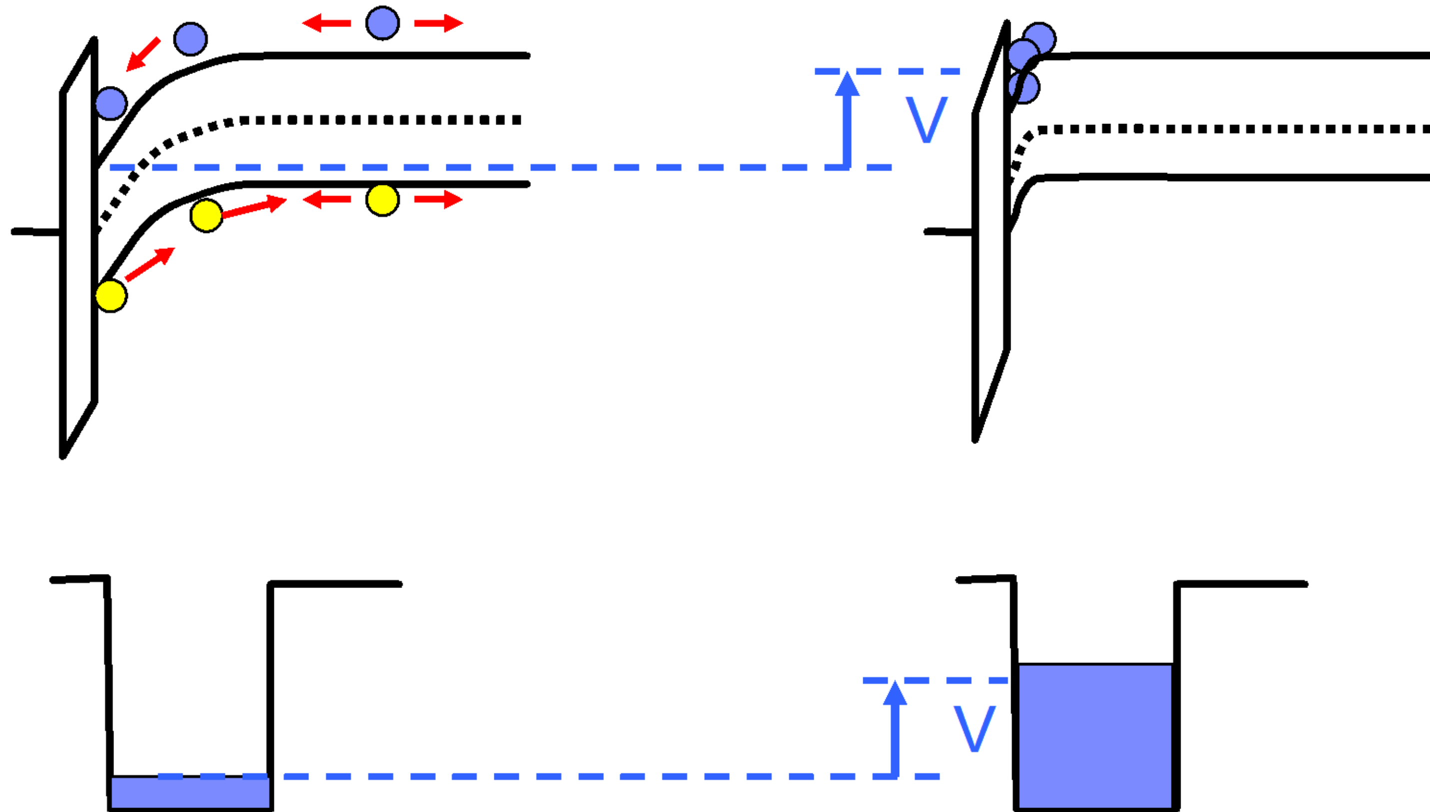
- Given the sensor quantum efficiency, conversion gain, and area its *sensitivity* measured in V/Lux·s can be determined

- Readout speed determines the video *frame rate* that an image sensor can operate at – 30 to 60 frames/s are typical, but lower frame rates are sometimes dictated by the available bandwidth (e.g., wireless camera), and higher frame rates are required for many industrial and military applications

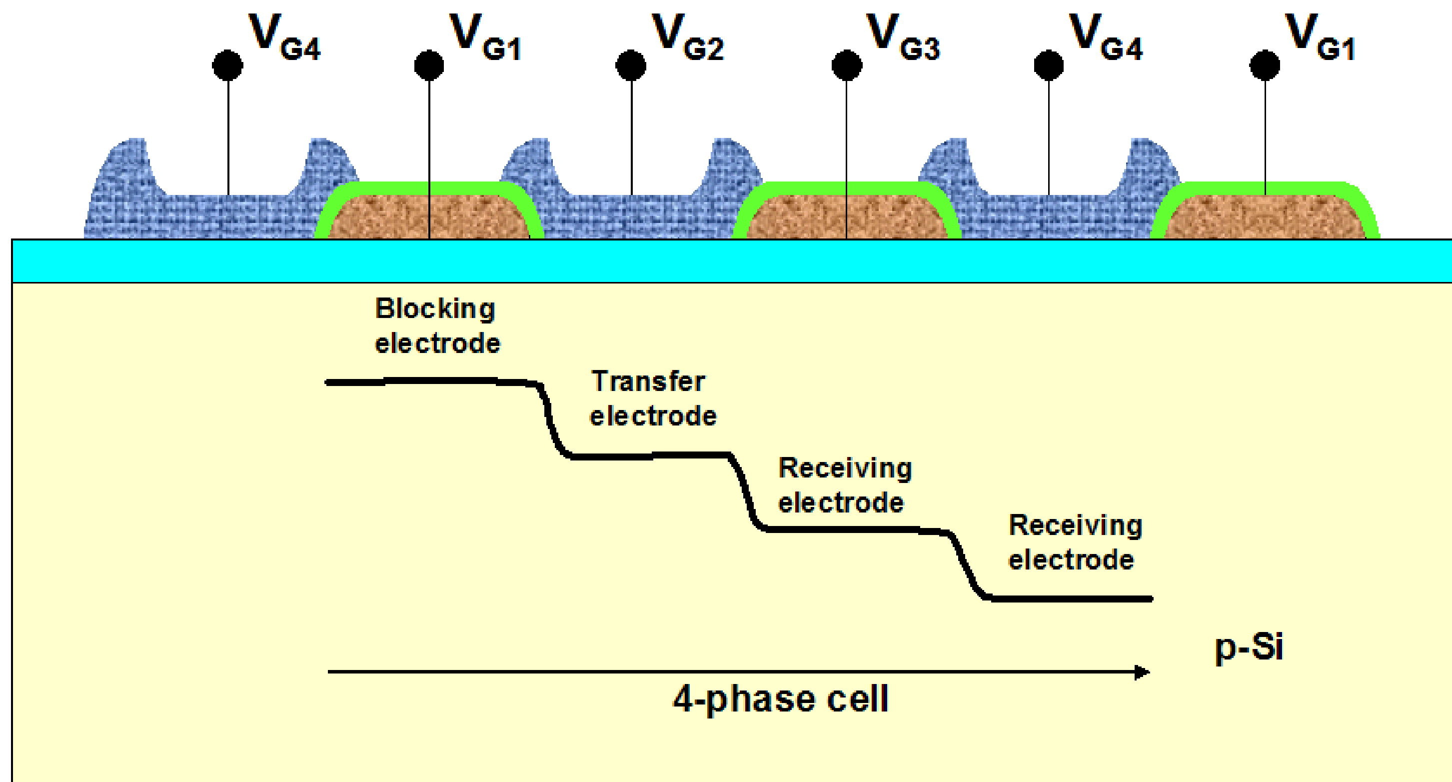
Charge-Coupled Devices

- CCD is a *dynamic* analog (charge) shift register
- It consists of a series of MOS capacitors coupled with one another
- CCD is clocked, and all operations are in transient mode
- Charge is *coupled* from one gate to the next gate by fringing electric field, potential and carrier density gradient
- We first discuss CCD operation using different clocking methods, then discuss their use in image sensors

Potential Well Analogy – MOS Capacitor

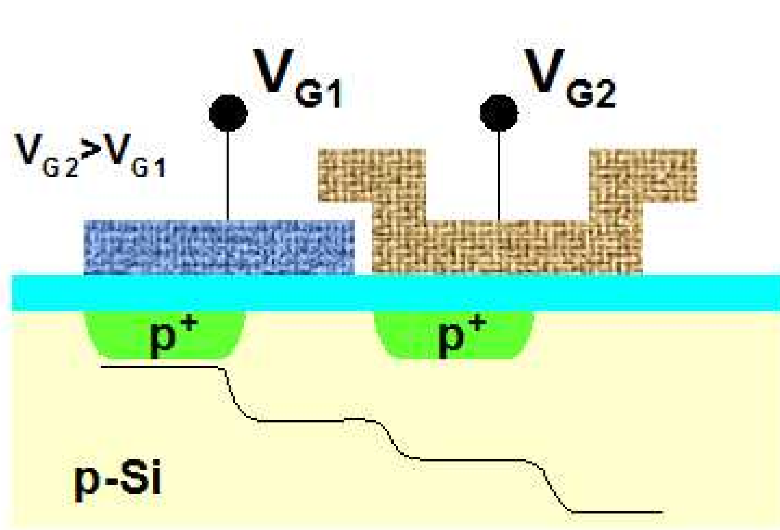


Basic 4-Phase CCD

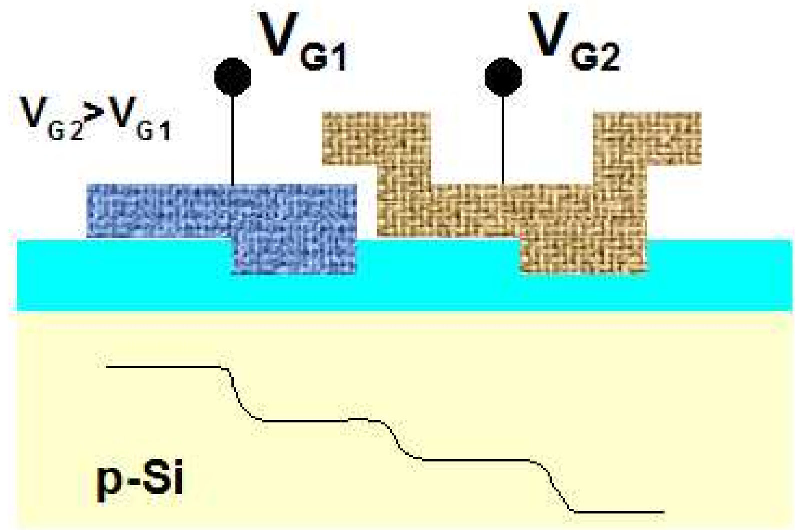


- A uni-directional potential gradient must be provided for charge transfer
- Gap between electrodes must be small (compared to the oxide thickness) to enable fringing electric field from neighboring electrodes to couple the charge across

Surface Potential Control



Doping

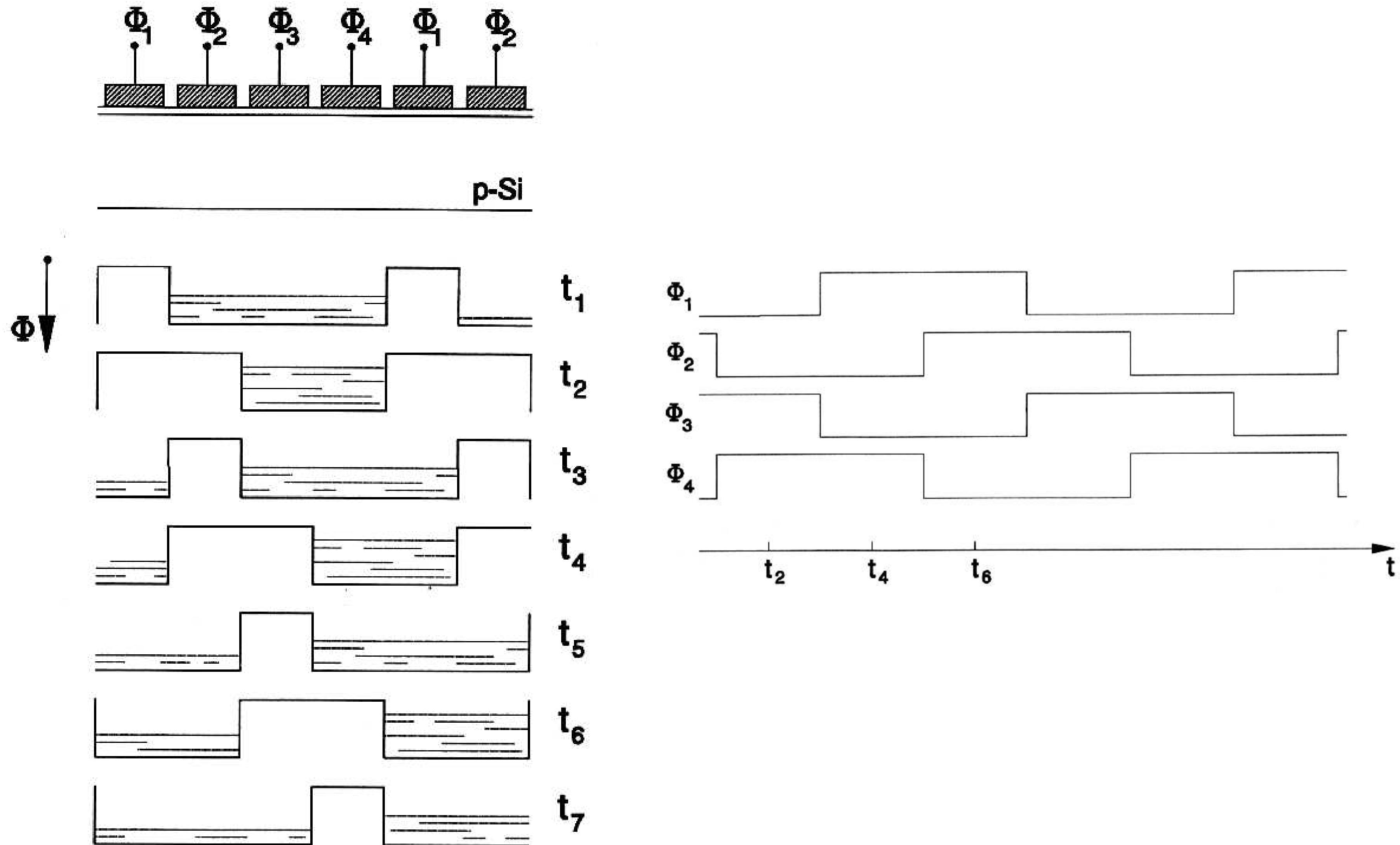


Oxide step

CCD Electrodes

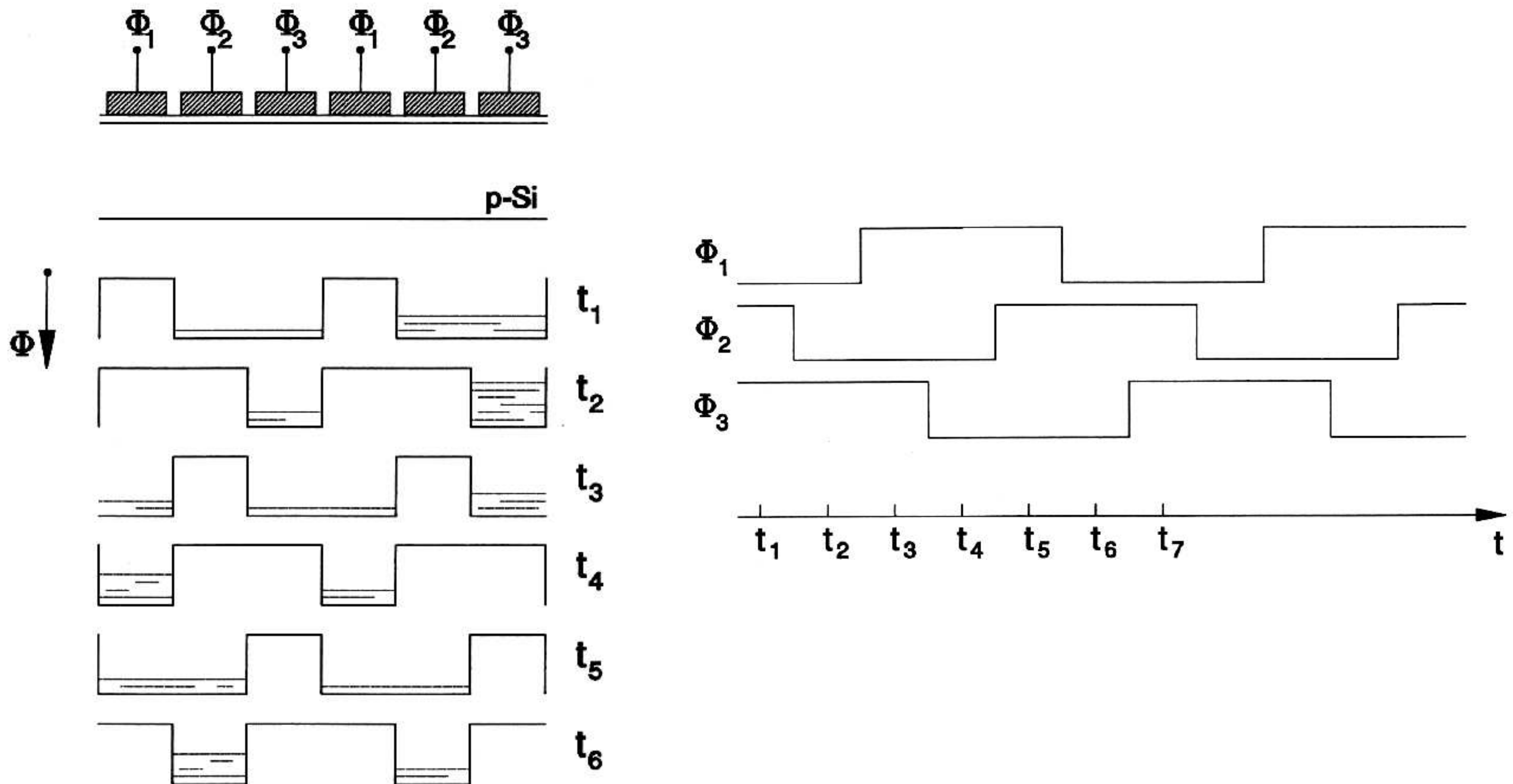
- Overlapping polysilicon electrodes
  - Oxidized polySi sidewall provides the electrode isolation
  - 2 levels polySi for 4-phase and 2-phase CCD
  - 3 levels polySi for 3-phase CCD
- Single polySi electrode also possible provided the electrode gap is small
- Most common: 4-phase, 3-phase, 2-phase
  - Other uncommon ones: ripple clock, accordion clock

Charge Transfer in a 4-Phase CCD



A. Theuwissen, "Solid State Imaging with Charge-Coupled Devices," Kluwer (1995)

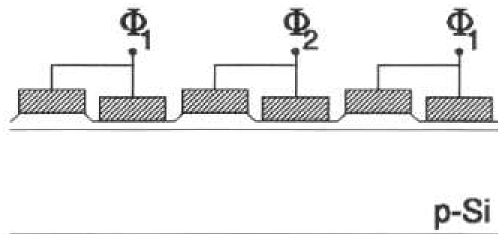
Charge Transfer in a 3-Phase CCD

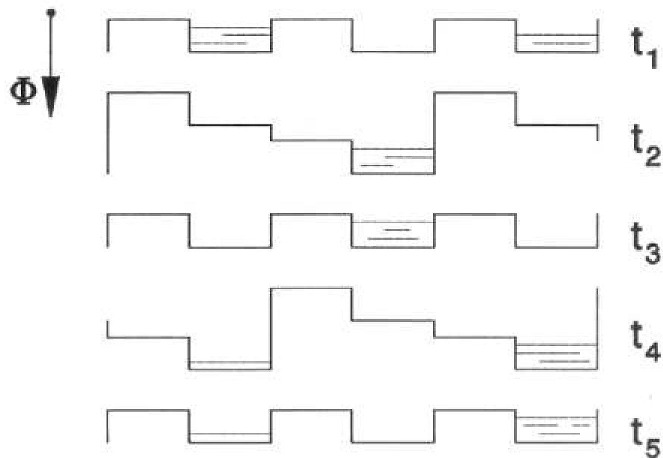


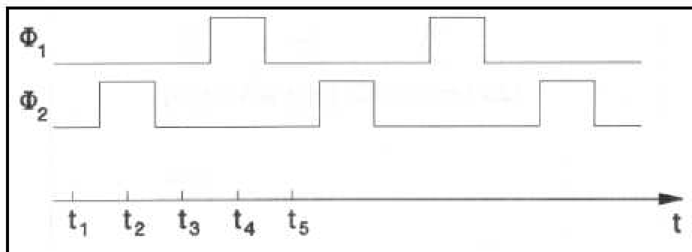
A. Theuwissen, "Solid State Imaging with Charge-Coupled Devices," Kluwer (1995)

Charge Transfer in a 2-Phase CCD

Two-clock mode



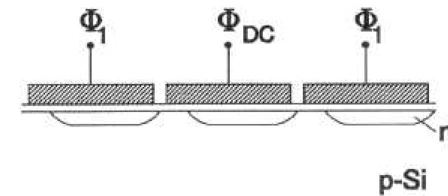


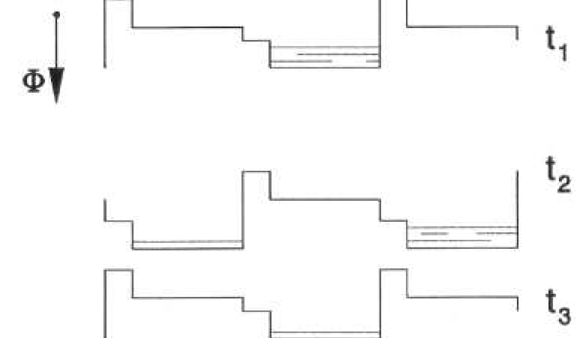


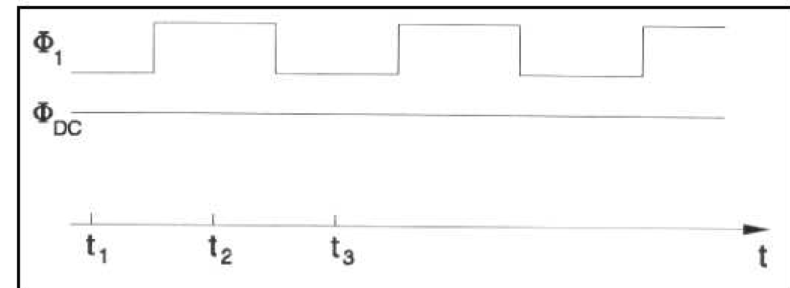
Potential step can be due to oxide, doping or other means

One-clock mode (1 ½ phase)

(phase one is DC biased)

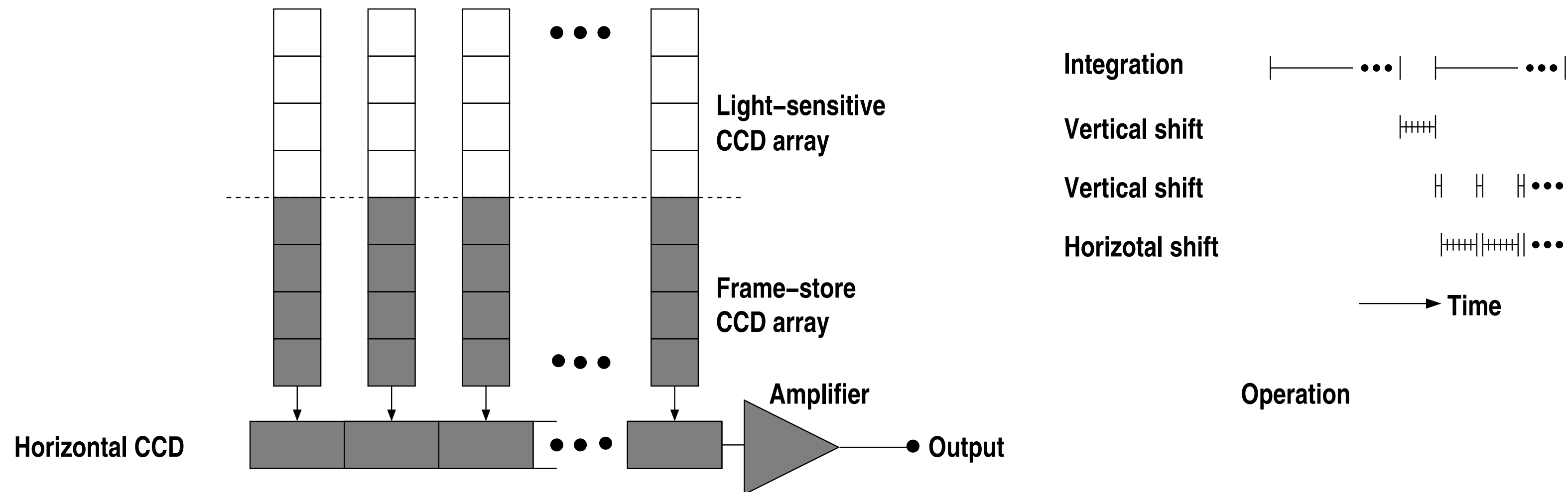






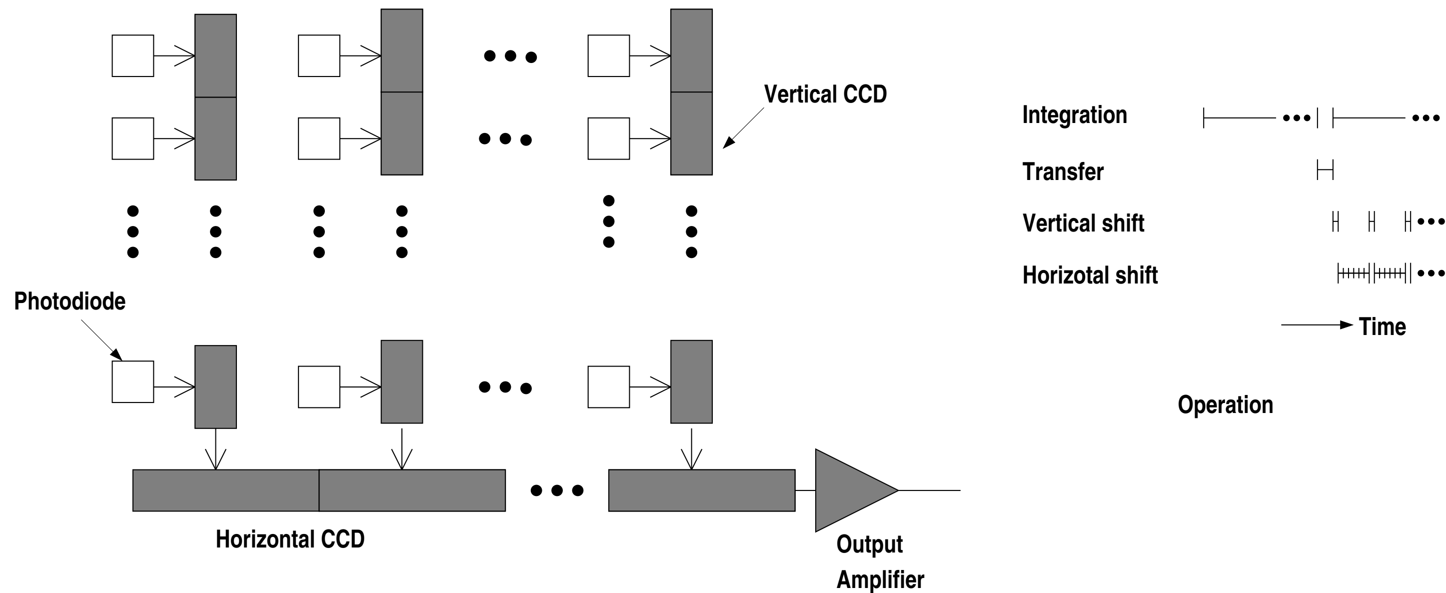
A. Theuwissen, "Solid State Imaging with Charge-Coupled Devices," Kluwer (1995)

Frame Transfer CCD Image Sensor



- Top CCD array used for photodetection (photogate) and vertical shifting
- Bottom CCD array optically shielded – used as frame store
- Operation is pipelined: data is shifted out via the bottom CCDs and the horizontal CCD during integration time of next frame
- Transfer from top to bottom CCD arrays must be done very quickly to minimize corruption by light, or in the dark (using a mechanical shutter)
- Output amplifier converts charge into voltage, determines sensor conversion gain

Interline Transfer CCD Image Sensor



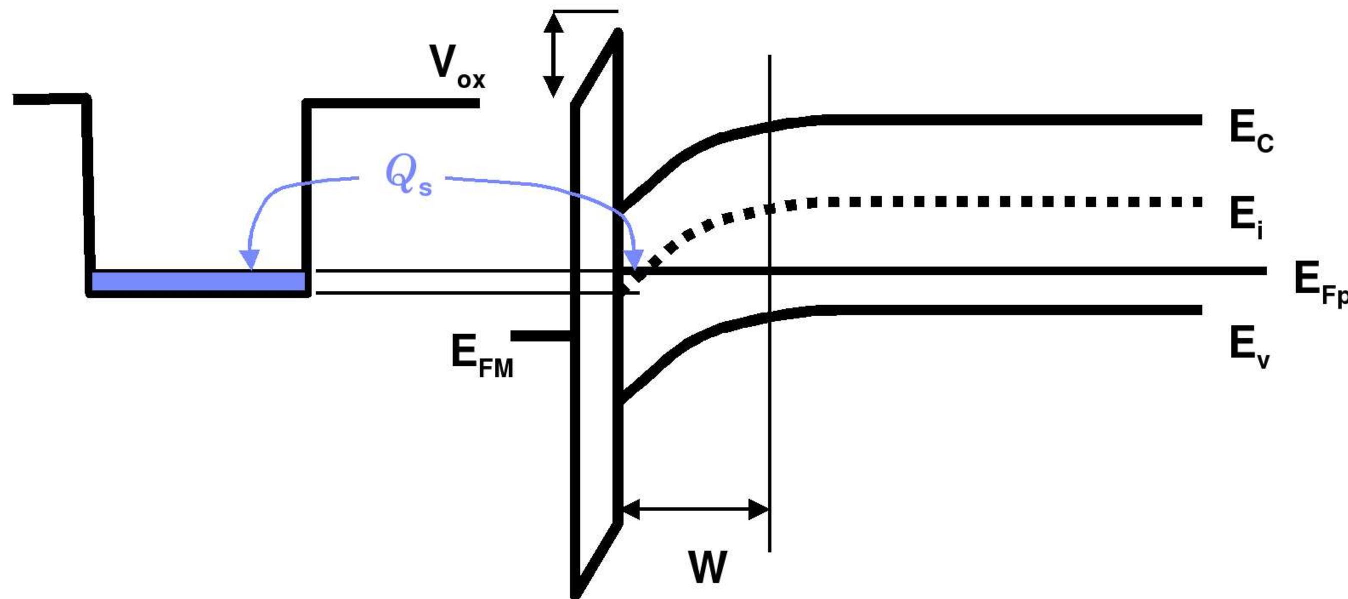
- Photodiodes or pinned diodes are used
- All CCDs are optically shielded, used only for readout
- Collected charge is *simultaneously* transferred to the vertical CCDs at the end of integration time (a new integration period can begin right after the transfer) and then shifted out
- Charge transfer to vertical CCDs simultaneously *resets* the photodiodes, (shuttering done electronically for "snap shot" operation)

Frame Transfer Versus Interline Transfer

- Frame transfer uses simpler technology (no photodiodes), and achieves higher *fill factor*, which is the fraction of pixel area occupied by the photodetector, than interline transfer
- Interline transfer uses optimized photodiodes with better quantum efficiency than the photogates used in frame transfer
- In interline transfer the image is captured at the same time ("snap shot" operation) and the charge transfer is not subject to corruption by photodetection (can be avoided in frame transfer using a mechanical shutter)
- Frame transfer has shorter integration time for the same frame rate than interline due to its nonoverlapping integration and readout times
- Frame transfer chip area (for the same number of pixels) can be larger than interline transfer
- Most of today's CCD image sensors use interline transfer

Surface Channel CCD Static Analysis

- Let's examine the amount of charge a surface channel CCD can store
- We need to relate the CCD gate voltage to the surface potential when there is depletion charge and mobile charge (Q_s in electrons/cm^2) under the gate (MOS capacitor)
- Surface potential under an MOS capacitor:



- We can relate the surface potential ψ_s to the applied bias voltage v_G and the charge stored Q_{sig} in electrons/cm^2 as follows

  The gate voltage is given by

$$v_G = \psi_s - v_{FB} + \frac{qQ_s}{C_{ox}},$$

  where

$$Q_s = N_a x_d + Q_{sig}$$

  is the total charge

  The depletion width is given by (see Appendix III of LN 1)

$$x_d = \sqrt{\frac{2\epsilon_s \psi_s}{qN_a}},$$

  where

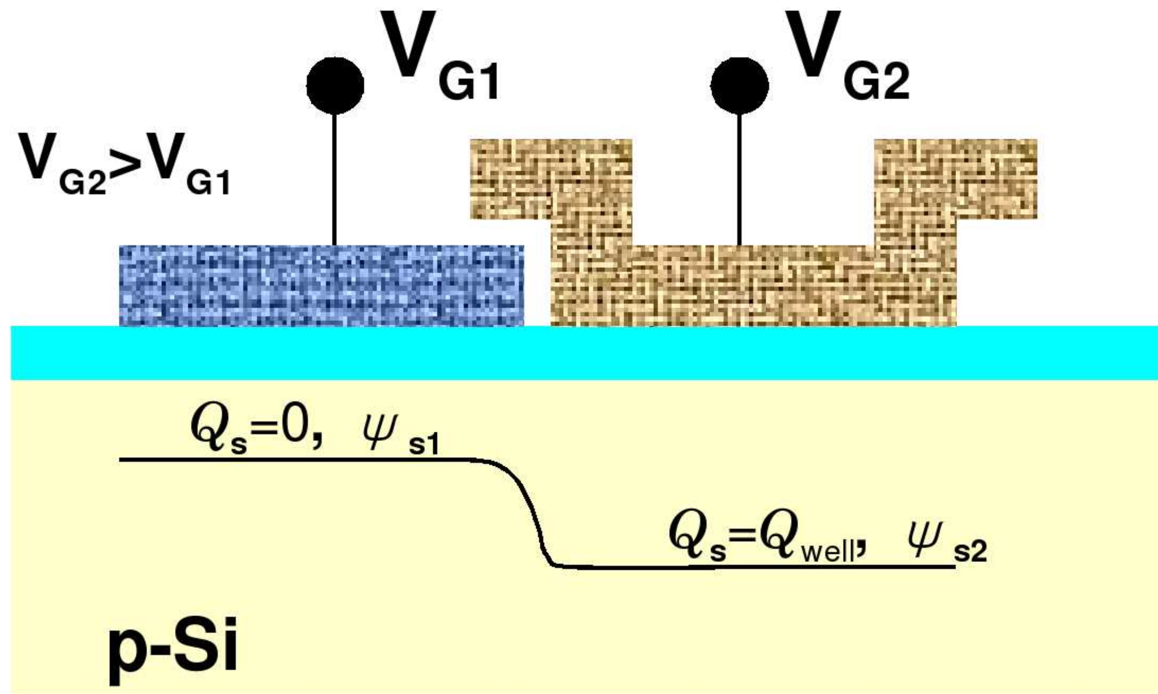
$$\psi_s = v_1 + v_2 - \sqrt{v_2^2 + 2v_1 v_2}$$

  Here

$$\begin{aligned} v_1 &= v_G + v_{FB} + \frac{qQ_{sig}}{C_{ox}} \\ v_2 &= \epsilon_s q N_a / C_{ox}^2 \end{aligned}$$

Well Charge Capacity for Surface Channel CCD

- Empty well – semiconductor is depleted
- Non-empty well – semiconductor is less depleted or has mobile charge



- We can derive the well charge capacity Q_{well} in electrons/cm^2 using the equations above as follows.
First at the top of the potential wells, $\psi_{s1} = \psi_{s2}$, thus

$$\begin{aligned} v_{G1} + v_{FB1} &= \psi_{s1} + \frac{\epsilon_s q N_a}{C_{ox}} \\ v_{G2} + v_{FB2} &= \psi_{s1} + \frac{\epsilon_s q N_a}{C_{ox}} + \frac{q Q_{\text{well}}}{C_{ox}}, \end{aligned}$$

Now, assuming $v_{FB1} = v_{FB2}$ and subtracting, we obtain

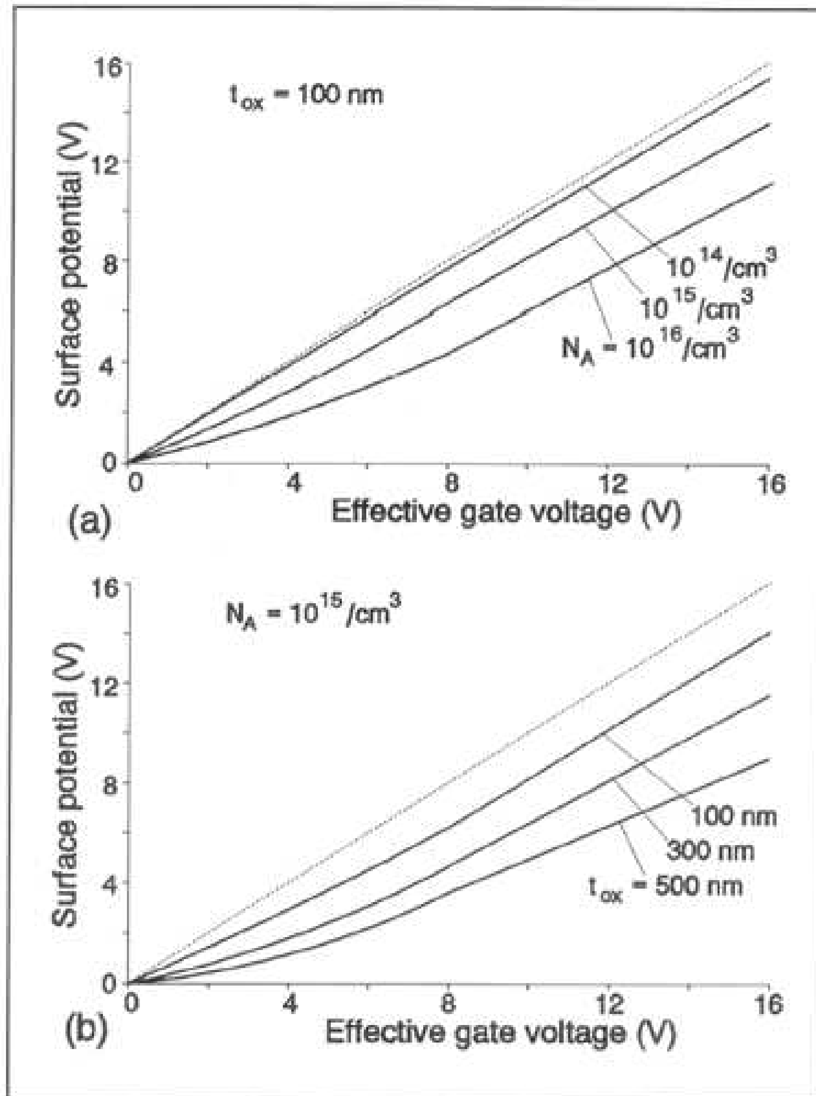
$$v_{G2} - v_{G1} = \frac{q Q_{\text{well}}}{C_{ox}}$$

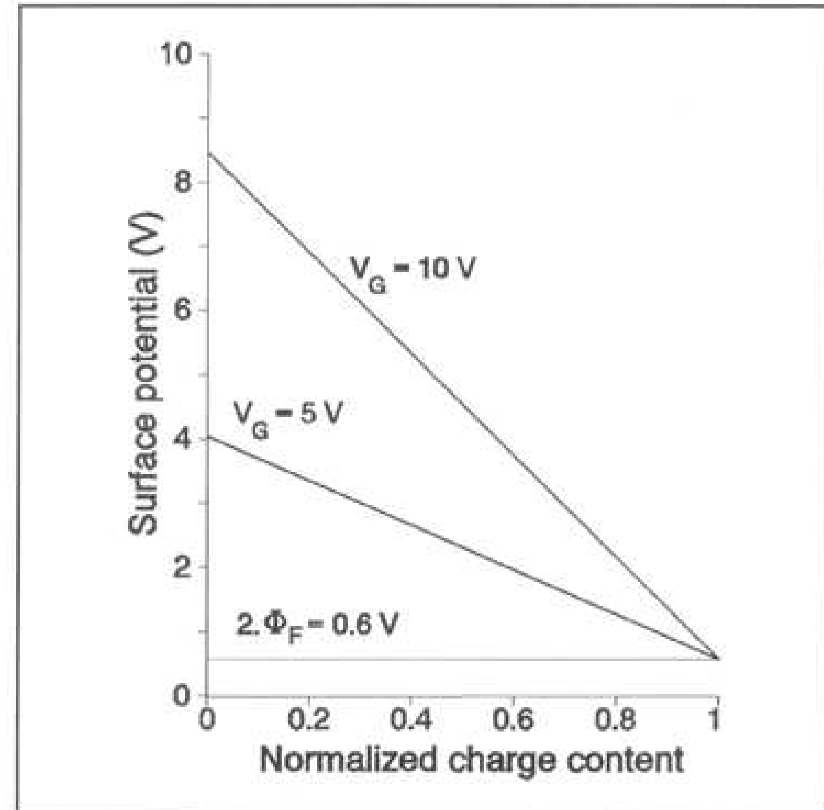
Thus

$$Q_{\text{well}} = \frac{(v_{G2} - v_{G1}) C_{ox}}{q}$$

The excess gate voltage is balanced by the charge in the well

Surface Channel CCD Static Design Curves



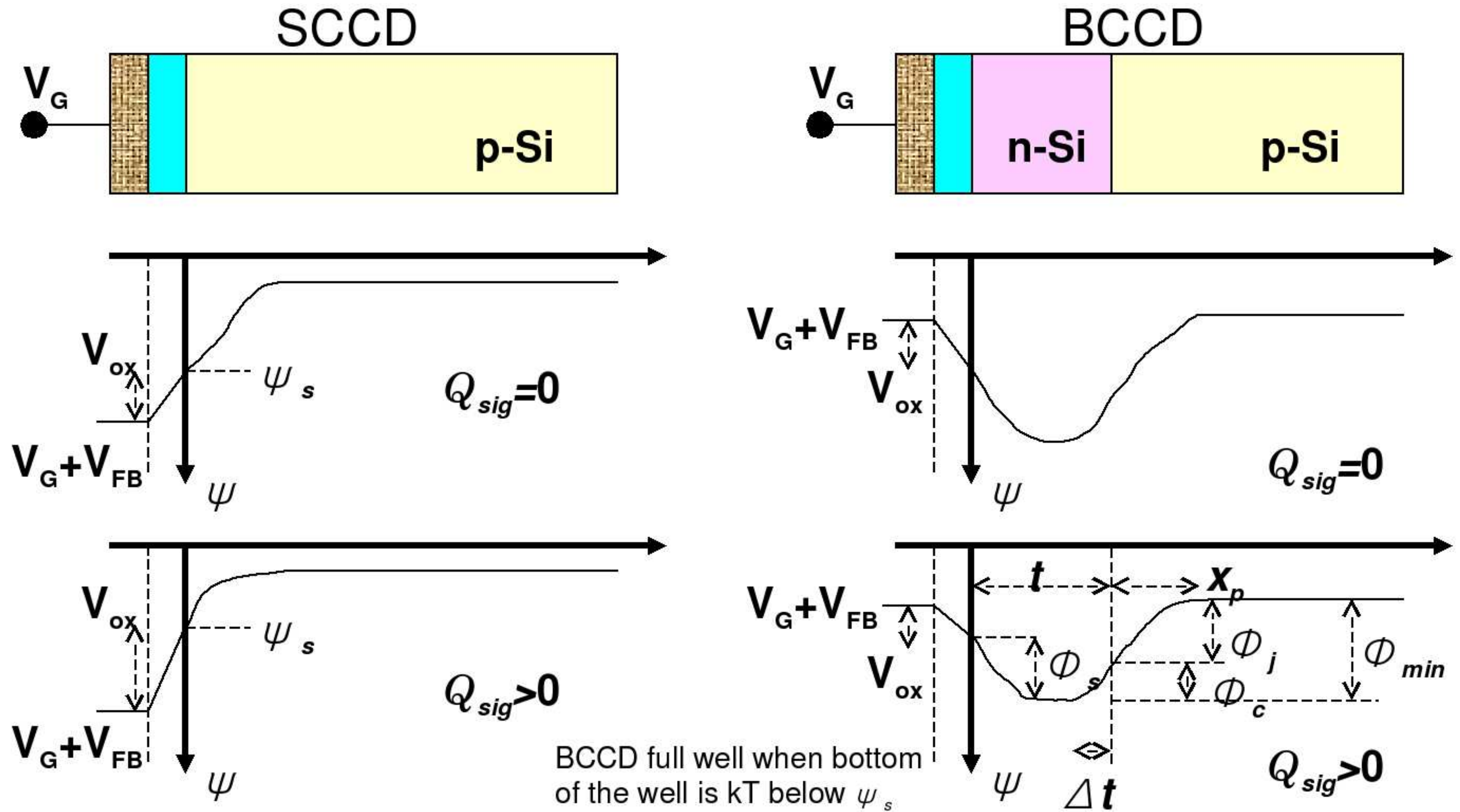


A. Theuwissen, "Solid State Imaging with Charge-Coupled Devices," Kluwer (1995).

Buried Channel CCD

- Having the mobile charge at the surface as in the surface channel CCD (SCCD) has several disadvantages
  - Si/SiO_2 interface states will capture the mobile carriers and release them at a later time, causing transfer inefficiency (to be discussed later)
  - Si/SiO_2 interface states introduce dark current due to surface generation (as discussed in Lecture Notes 1)
- It is therefore desirable to store the carriers some distance below the Si/SiO_2 interface – this is called buried channel CCD (BCCD)
- In a BCCD, the surface is doped with the opposite polarity (e.g., n-Si if the substrate is p-Si), forming a junction beneath the surface
- The surface doping region (n-Si) is completely depleted (empty well)
- As signal charge is stored in the BCCD, the surface doping region becomes less depleted

Channel Potential of SCCD and BCCD



Buried Channel CCD Static Characteristics

- In order to determine the charge well capacity of a BCCD, we need to know the minimum of the energy well (or maximum of potential well) $\phi_{\min}$, where $\phi_{\min}$ is referenced to the substrate potential
- To avoid surface channel operation, the energy minimum should be a few kT below the potential at the surface
- We calculate the relationship between the applied voltage v_G, the signal charge Q_{sig}, and the potential $\phi_{\min}$ in a way analogous to the surface channel case
- By KVL,

$$v_G + v_{FB} + v_{ox} + \phi_s = \phi_{\min} \text{ and } \phi_{\min} = \phi_j + \phi_c$$

By Gauss's law

$$v_{ox} = \frac{q(N_d(t - \Delta t) - Q_{sig})}{C_{ox}}$$

Using standard pn junction theory, we can relate the potential across the depletion region to its thickness as follows

$$\phi_s = \frac{qN_d}{2\epsilon_s}\left(t - \Delta t - \frac{Q_{sig}}{N_d}\right)^2,$$

$$\phi_j = \frac{qN_a x_p^2}{2\epsilon_s}, \quad \phi_c = \frac{qN_d(\Delta t)^2}{2\epsilon_s}, \text{ and}$$

$$x_p = \frac{N_d \Delta t}{N_a}$$

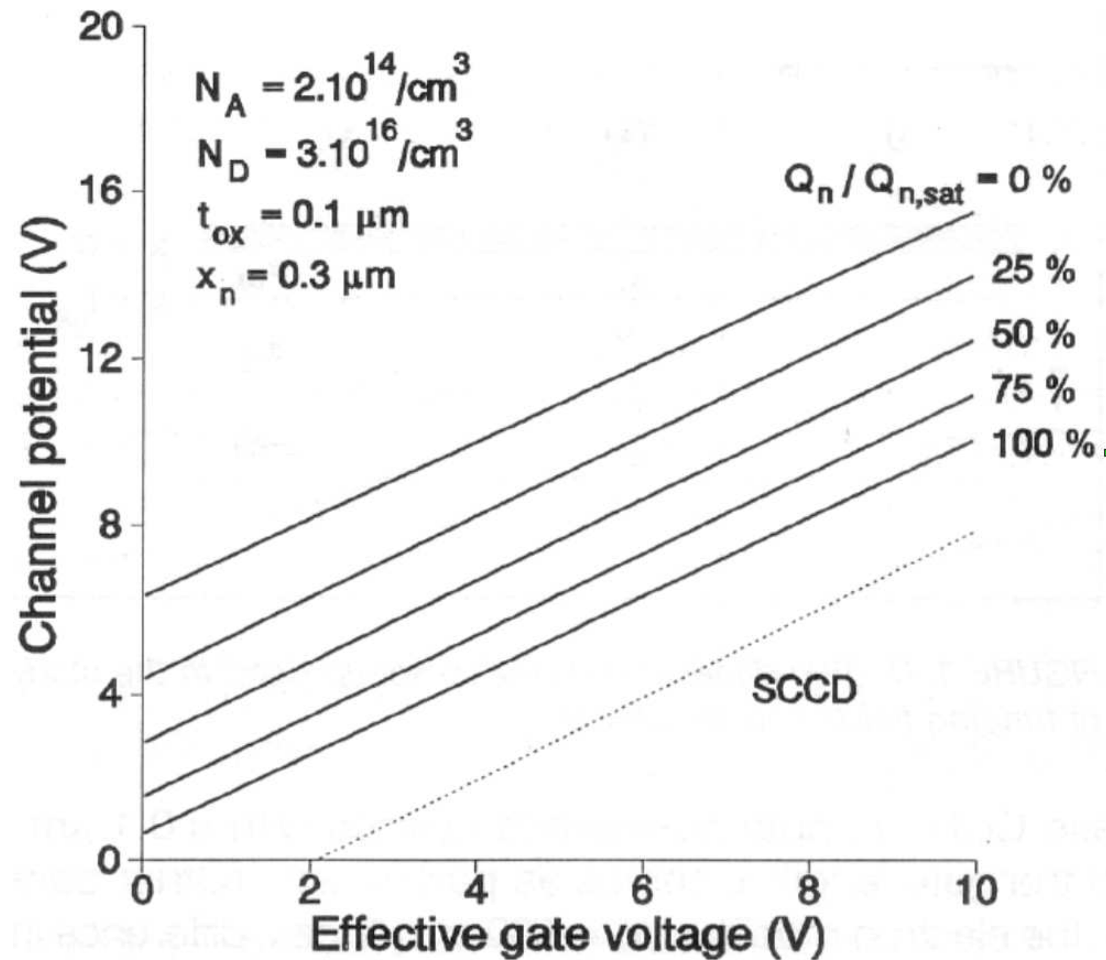
Note that ϕ_s is the same as ψ_s. Combining the above equations, we obtain the following quadratic equation in $\phi_{\min}^{1/2}$

$$\frac{N_d}{N_d + N_a}\phi_{\min} + \left(\frac{1}{C_{ox}} + \frac{t}{\epsilon_s} - \frac{Q_{sig}}{N_d \epsilon_s}\right)\left(\frac{2q\epsilon_s N_a N_d}{N_d + N_a}\right)^{\frac{1}{2}} \phi_{\min}^{\frac{1}{2}} = v_G + v_{FB}$$
$$+qN_d t\left(\frac{1}{C_{ox}} + \frac{t}{2\epsilon_s}\right) - qQ_{sig}\left(\frac{1}{C_{ox}} + \frac{t}{\epsilon_s} - \frac{Q_{sig}}{2N_d\epsilon_s}\right)$$

After finding $\phi_{\min}$, all other unknowns ($\phi_s, \phi_j, \phi_c, \Delta t$, v_{ox}, and x_p) can be found

Reference: D. F. Barbe, "Imaging Devices Using the Charge-Coupled Concept," *Proceedings of IEEE*, vol 63, pp 28-67, 1975

Buried Channel CCD Static Design Curves



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Charge Transfer in CCD

- Four mechanisms are involved in the dynamic charge transfer process
  - Self-induced drift
  - Electrostatic repulsion
  - Thermal diffusion
  - Fringing field
- The first charge carriers are transferred by self induced drift and the charge is re-distributed within the well by electrostatic repulsion Both processes are fairly quick.
- Thermal diffusion is a slower process.
- Finally, the last remaining charge is transferred by fringing field
- The *charge transfer efficiency* η is the fraction of charge transferred ($1 - \eta$ is the *inefficiency*)
- Self-induced drift and electrostatic repulsion give $1 - \eta \approx 10^{-2}$

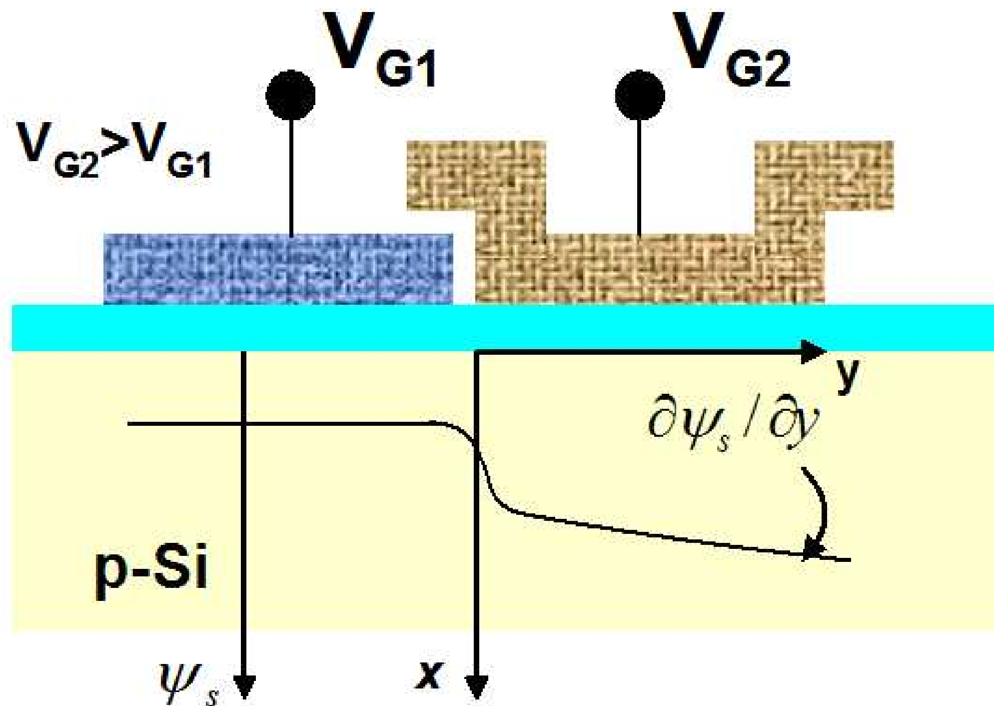
- Adding thermal diffusion gives $1 - \eta \approx 10^{-3}$
- Further adding fringing field gives $1 - \eta \approx 10^{-4}$
- In order to achieve high transfer efficiency and high transfer speed, CCD should be designed to have large fringing field

Charge Transfer in CCD

- The four driving forces involved in the charge transfer process can be quantified by an equivalent electric field. Define the signal charge areal density as $\rho_s(y, t)$ in electrons/cm^2
  - Self-induced drift:
$$E_d = \frac{q}{C_{ox}} \cdot \frac{\partial \rho_s}{\partial y}$$
  - Electrostatic repulsion:
$$E_r = -\frac{2qt_{ox}}{\epsilon_{ox} + \epsilon_s} \cdot \frac{\partial \rho_s}{\partial y},$$
  - Thermal diffusion:
$$E_{th} = \frac{kT}{q\rho_s} \cdot \frac{\partial \rho_s}{\partial y}$$
  - Fringe field: E_{FR}
- We provide a qualitative explanation of these four quantities

Self-Induced Drift

- A gradient in charge distribution (during the transfer process) results in a gradient in surface potential along the transfer direction (y)

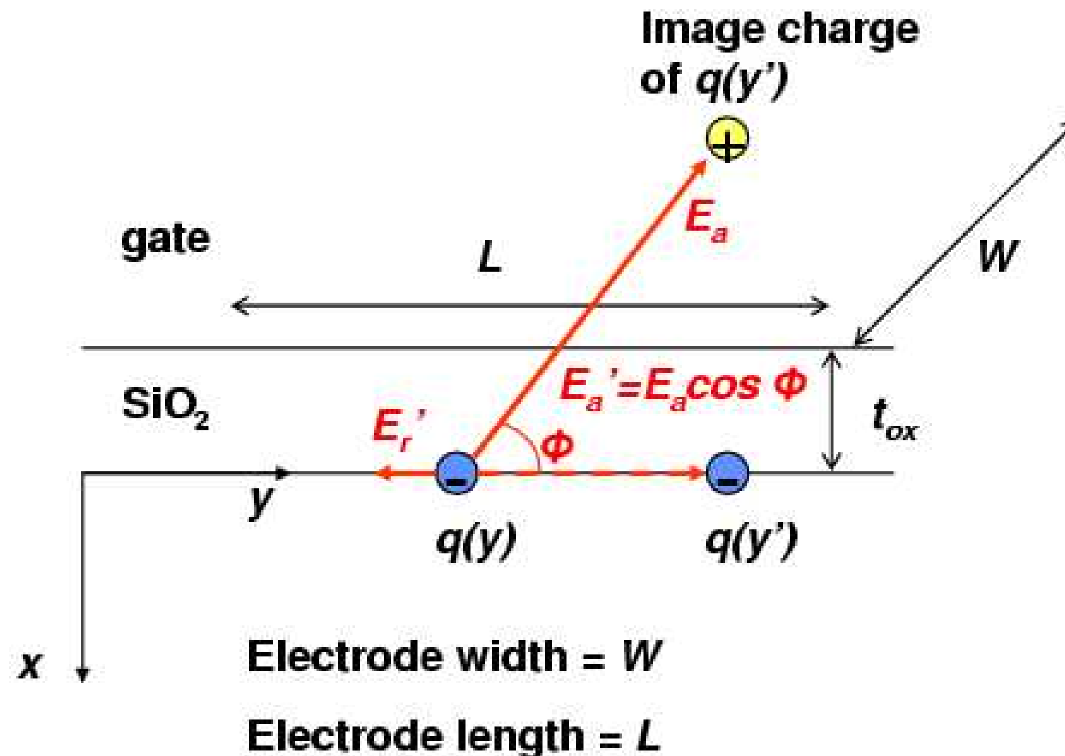


- Assuming $t_{ox} << x_d$, we obtain

$$E_d \approx \frac{q}{C_{ox}} \cdot \frac{\partial \rho_s}{\partial y}$$

Electrostatic Repulsion

- Electrostatic repulsion arises from the electrostatic forces acting on $q(y)$ by $q(y')$ (repulsion) and its image charge (attraction)



- The resulting field is given by

$$E_r = -\frac{2qt_{ox}}{\epsilon_{ox} + \epsilon_s} \cdot \frac{\partial \rho_s}{\partial y} \approx -\frac{q}{2C_{ox}} \cdot \frac{\partial \rho_s}{\partial y},$$

where we made the approximation $\epsilon_s \approx 3\epsilon_{ox}$

Thermal Diffusion

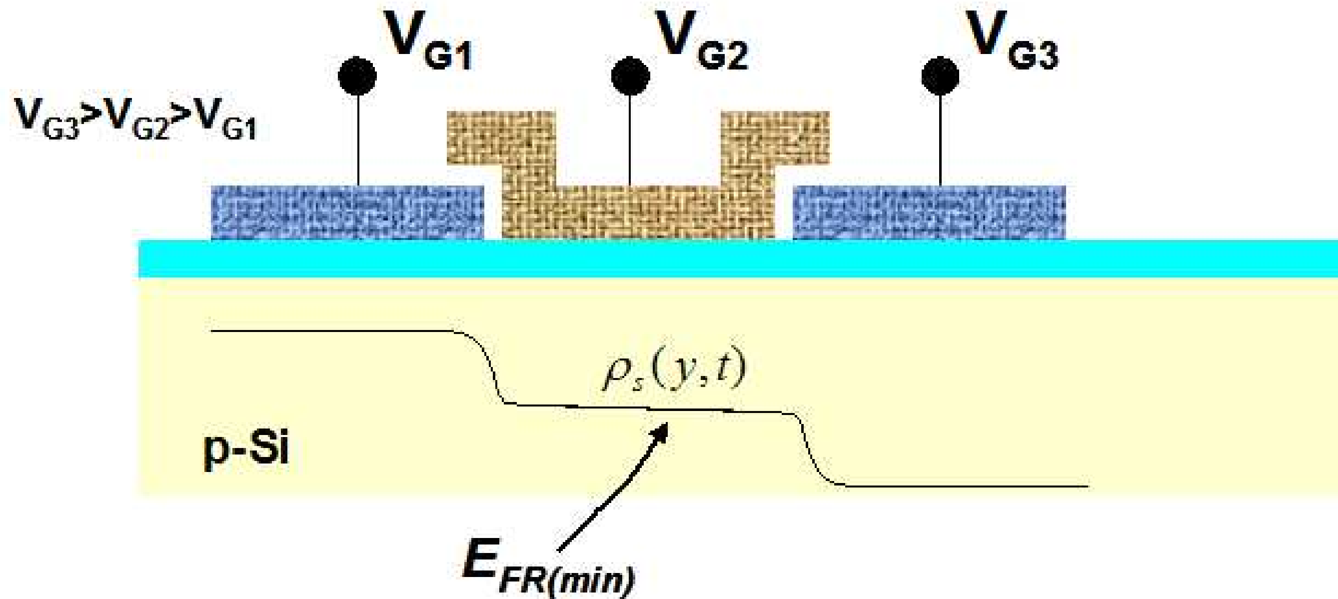
- A gradient of charge density along the transfer direction (y) establishes a diffusion current
- The diffusion can be modeled as an effective electric field acting on the carriers, which is given by

$$E_{th} = \frac{kT}{q\rho_s} \cdot \frac{\partial \rho_s}{\partial y}$$

- This effective field depends on carrier density in the CCD well

Fringe Electric Field

- Fringe electric field arises from the 2-dimensional nature of the potential in the device – coupling from neighboring electrodes
- The fringe electric field is smallest at the middle of the electrode



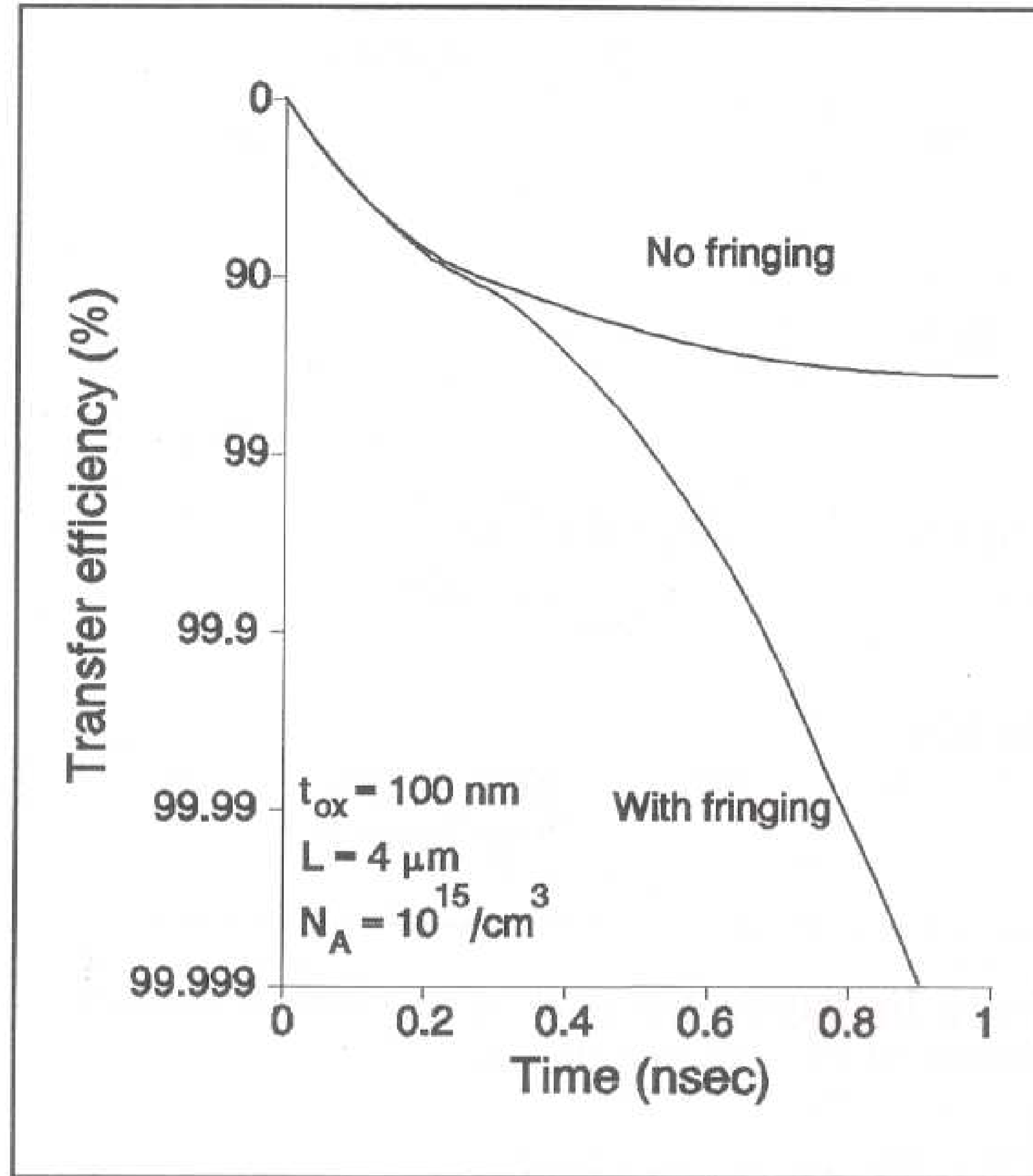
- The following approximate analytical expression for $E_{FR(min)}$ can be found by solving the 2D Poisson equation

$$E_{FR(\min)} \approx \frac{2\pi}{3}\frac{\epsilon_s \Delta v}{L^2 C_{ox}}\left(\frac{5x_d L}{1+5x_d L}\right)^4$$

where

$$\Delta v = v_{G2} - v_{G1}$$

J. E. Carnes, W. F. Kosonocky, and E. G. Ramberg, "Drift-aiding fringing fields in charge-coupled devices," IEEE Journal of Solid-State Circuits, vol. 6, pp. 322 - 326, October 1971.



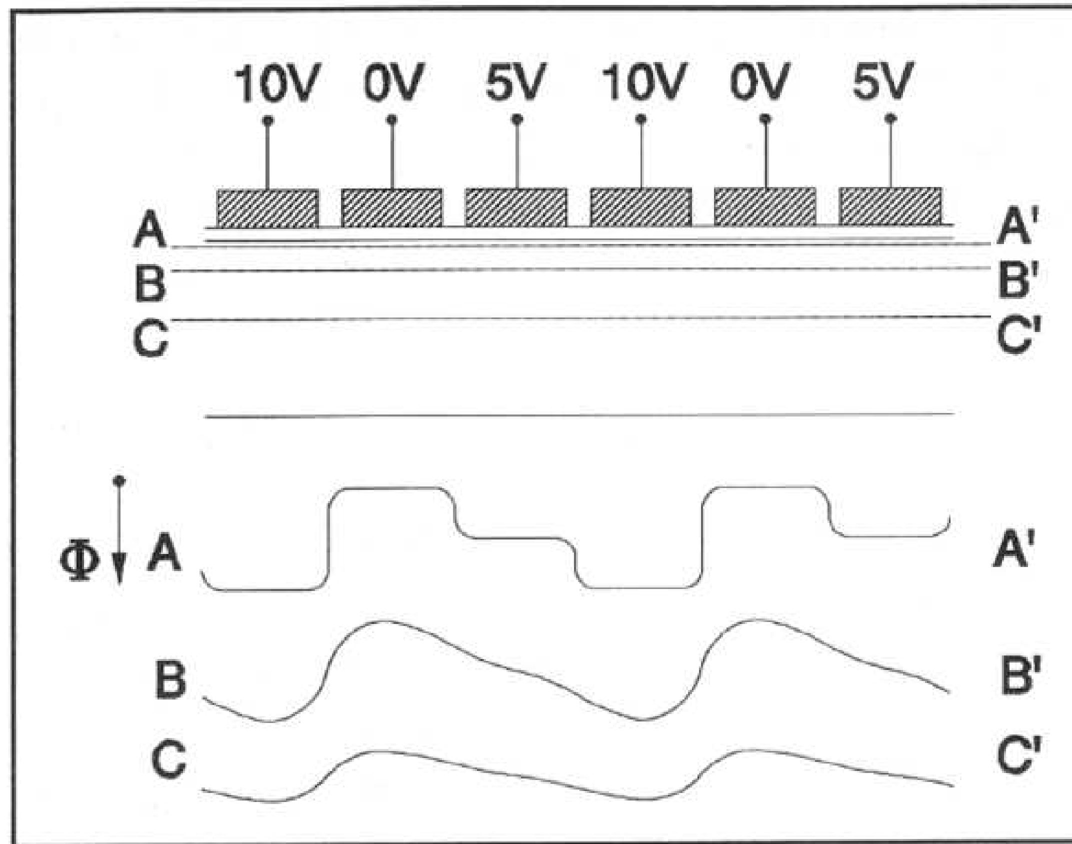
A. Theuwissen, “Solid State Imaging with Charge-Coupled Devices,” Kluwer (1995).

Methods to Increase Fringing Field

- Increase gate oxide thickness
- Decrease substrate doping
- Reduce CCD gate length (E_{FR} varies as $1/L^2$)
- Increase the gate voltage difference

Charge Transfer Advantage of BCCD

- A major advantage of buried channel CCD is the large fringing field, which results in fast charge transfer



Charge Transfer Efficiency

- The CCD charge *transfer efficiency*, $\eta \le 1$, is the fraction of signal charge transferred from one CCD stage to the next, i.e.,

$$\eta = 1 - \frac{Q(t)}{Q(0)},$$

  where

$$Q(t) = W \int_0^L \rho_s(y,t)\, dy$$

  Here L and W are the gate length and width of the CCD, respectively

- η must be made very close to 1, because in a CCD image sensor charge is transferred up to $n+m$ CCD stages ($3 \times (n+m)$ times for 3-phase CCD)

- Example: consider a 1024×1024 CCD image sensor
  The table lists the charge transfer efficiency η and the corresponding worst case fraction of charge transferred to the output

η	fraction at output
0.999	0.1289
0.9999	0.8148
0.99999	0.9797

Transfer Efficiency Analysis

- The "equivalent" electric field that acts on the charge carriers in a CCD well can be used to derive the charge transfer efficiency
- The derivations are too detailed to go through in this course, so we just state the results
- The total equivalent electric field is given by

$$\begin{aligned} E_{tot}(y,t) &= E_d + E_r + E_{th} + E_{FR} \\ &\approx \frac{q}{C_{ox}} \cdot \frac{\partial \rho_s}{\partial y} - \frac{q}{2C_{ox}} \cdot \frac{\partial \rho_s}{\partial y} + \frac{kT}{q\rho_s} \cdot \frac{\partial \rho_s}{\partial y} + E_{FR} \\ &\approx \frac{q}{2C_{ox}} \cdot \frac{\partial \rho_s}{\partial y} + \frac{kT}{q\rho_s} \cdot \frac{\partial \rho_s}{\partial y} + E_{FR} \end{aligned}$$

- Recall that the current density can be expressed as

$$j = q\mu_n nE + qD\frac{\partial n}{\partial y}$$

We can then transform the equivalent electric field into an equivalent diffusion constant as if the current is all due to diffusion

$$D_{eff} = \mu_n \left(\frac{\rho_s}{2C_{ox}} + \frac{kT}{q} + \frac{E_{FR}(y)}{\left(\frac{1}{\rho_s} \cdot \frac{\partial \rho_s}{\partial y}\right)} \right)$$

Now, we weight average over the length of the CCD gate to obtain

$$\overline{D}_{eff} = \mu_n \left(\frac{\overline{\rho}_s}{2C_{ox}} + \frac{kT}{q} + \frac{2LE_{FR(\min)}}{\pi} \right)$$

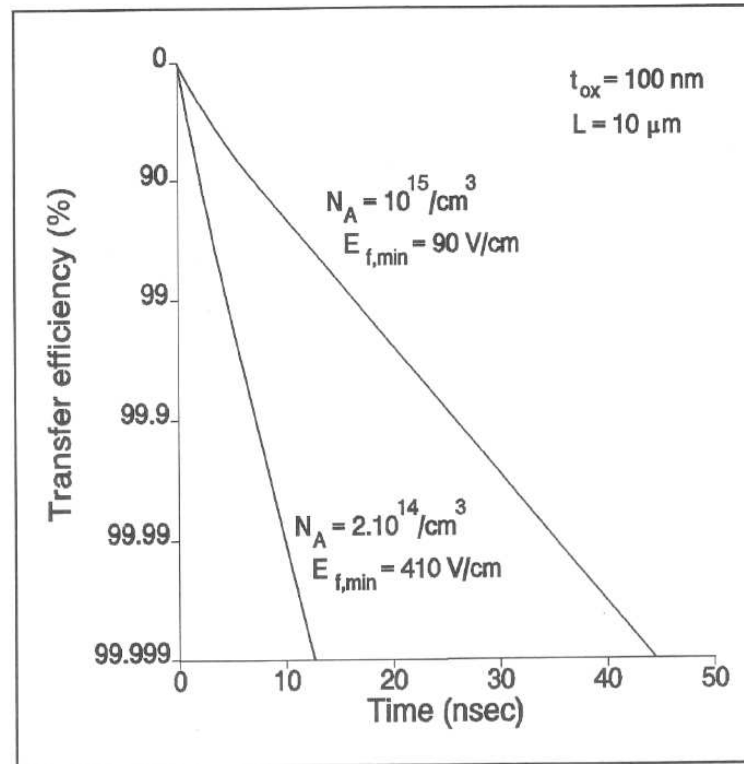
- The transfer inefficiency is thus $\propto e^{-t/\tau}$, where

$$\frac{1}{\tau} = \overline{D}_{eff} \times \left(\frac{\pi}{2L}\right)^2$$

- High transfer efficiency is achieved if
  - the time available to complete the transfer is long enough (a function of CCD clocking speed)
  - surface state density is low
- Since $\tau \propto L^2$, shorter CCD gates will have faster transfer

A Simple Illustration

- 99% of charge transferred immediately and remaining 1% transferred slowly by thermal diffusion and fringing field
- Last 1% accounts for most of the transfer time



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CCD Readout Speed

- CCD imager readout speed is limited mainly by the array size and the charge transfer efficiency requirement
- Example: consider a 1024×1024 3-phase interline transfer CCD image sensor with $\eta = 0.99997$, $L = 4\mu$m, and $D_n = 35$cm$^2/s$, find the maximum video frame rate

  transfer time for the horizontal CCD limits the readout speed
  to find the minimum required transfer time per CCD stage, t_{min}, we use the equation

$$\eta = 0.99997 = (1 - 0.01e^{-\frac{t_{min}}{3\tau}})^3,$$

  which gives $t_{min} = 37.8$ns, thus the time required to shift one row out is 37.8ns$\times 1024 = 38.7\mu$s
  ignoring the row transfer time (from vertical CCDs), we get minimum frame transfer time of 39.6ms, or maximum video frame rate of 25frame/s
  Note: CMOS image sensors can be much faster than CCDs