Lecture Notes for EE 101

Winter Quarter 2002–2003

Department of Electrical Engineering
Stanford University

Introduction to Circuits

Professor Abbas El Gamal

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Lecture Notes 1
Introduction

- About EE101
  - in EE curriculum
  - circuit analysis
  - device models
- Course goals
- Course topics
- Lecture notes

EE101

- **EE at Stanford:** 5 labs in two general areas:

  Systems – emphasis on applications of mathematics to EE

  - Computer Systems Lab (CSL)
  - Information Systems Lab (ISL)
  - Space, Telecommunications, and Radioscience (STAR)

  Devices – emphasis on applications of physics to EE

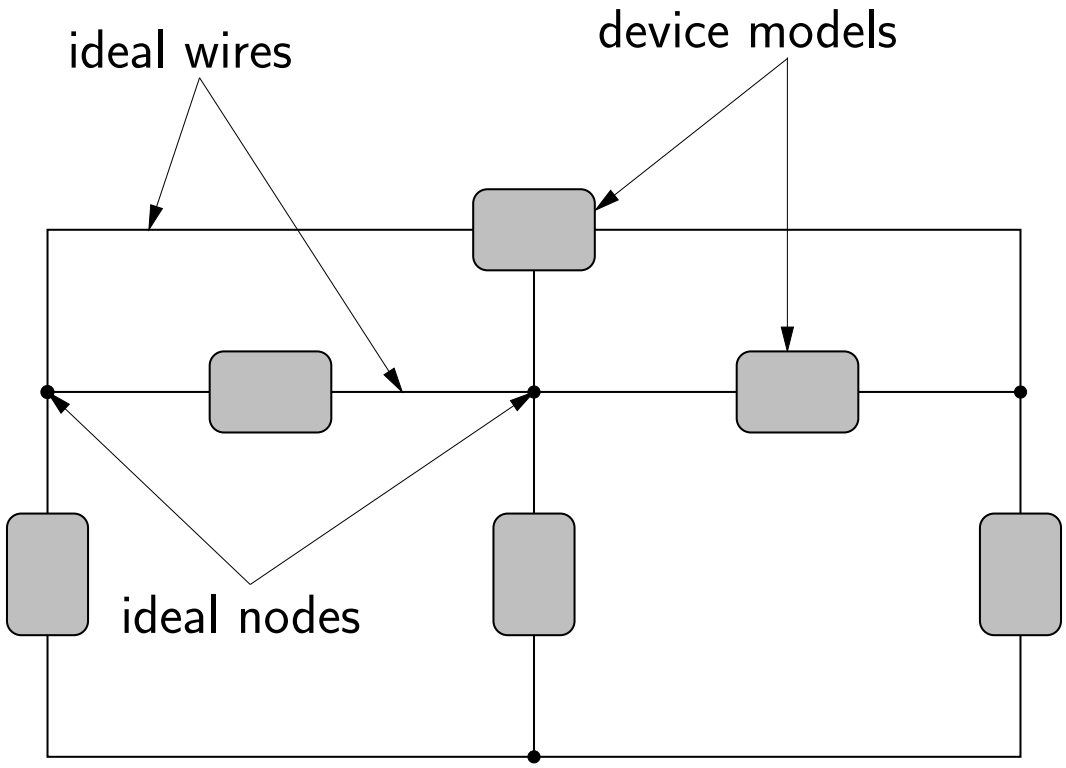
  - Solid State and Photonics Lab (SSPL)
  - Integrated Circuits Lab (ICL)

- EE 101 is the first course in EE major sequences
  - 101, 102, 103 are first "systems" courses
  - 111, 112 are first "devices" courses
  - 113 is a blend of the two

- EE101 deals with basic circuit *analysis* techniques
  - it deals with circuit *models* not physical circuits and it is not a lab course
  - EE 121 and 122 deal with circuit *design* and are lab courses

Circuit Analysis

a circuit model is an interconnection of *device models* or *circuit elements* using ideal wires and ideal connections (or nodes), $i.e.$, ideal short circuits

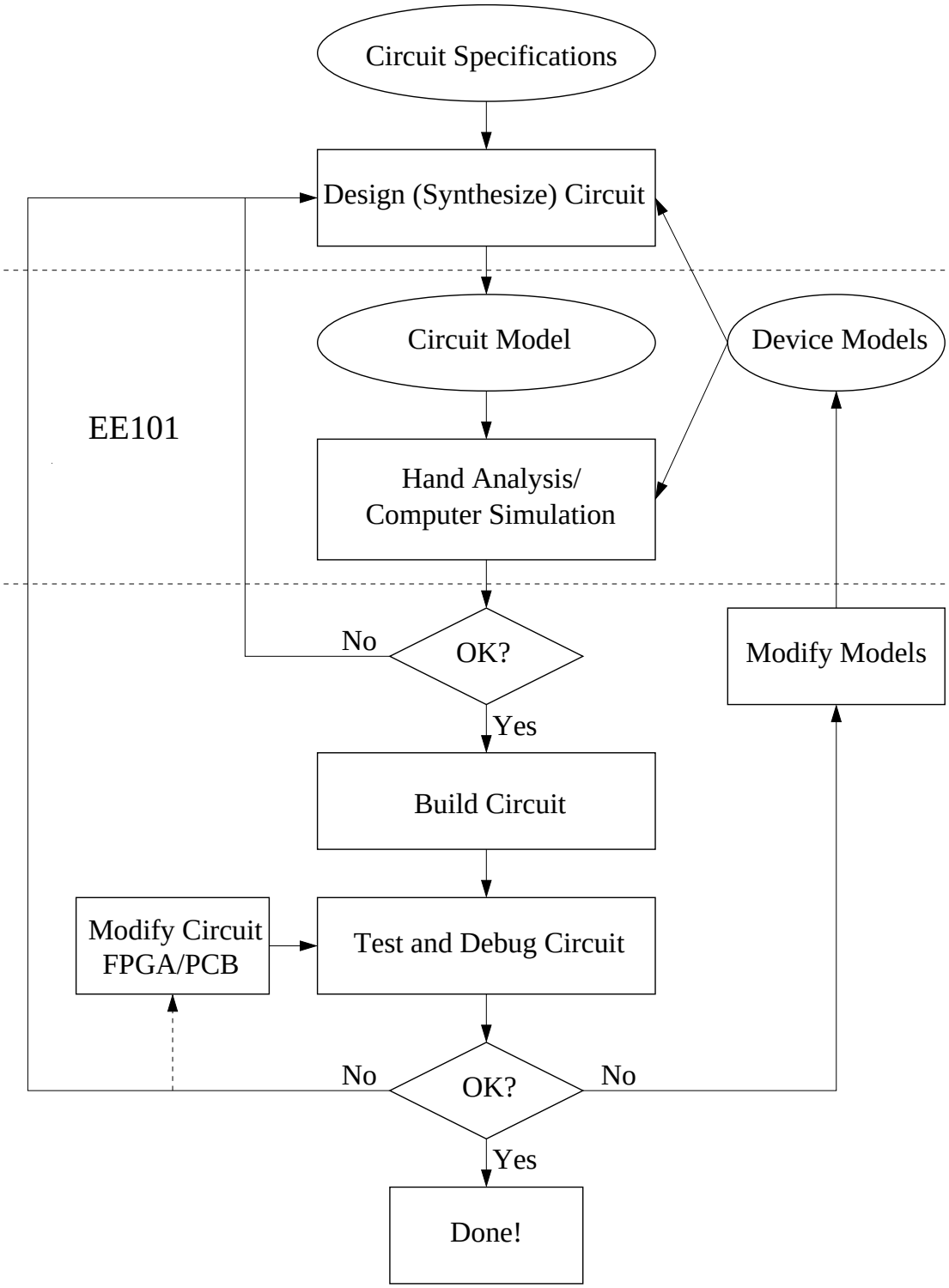


the purpose of circuit analysis is to determine the currents and voltages in the circuit

analysis done using *only*:

- device models, which specify relations between each device terminals' voltages and currents, and
- Khirkoff's current and voltage laws (KCL, KVL)

Circuit Design Process



Device Models

- characterize the device terminal electrical behavior, $i.e.$, relations between terminal voltages and currents
  - over certain ranges of voltages and currents
  - under certain operating conditions, $e.g.$, frequency, temperature
  - to some accuracy

- models are typically mathematical, but can also be specified using tables or graphs

  Example: 100Ω ($1/2\mathrm{W}$, 5%) carbon resistor
  common model ('Ohm's law'): $v(t) = i(t)R$, where
  - $R \approx 100\Omega$ (presumably within 5%)
  - $v(t)$ is the voltage across the resistor at time t
  - $i(t)$ is the current through the resistor at time t

  this is a good model
  - for $|v(t)| < 7\mathrm{V}$ or so
  - for $v(t)$ not changing too much in 100nsec or so
  - over some temperature range, $e.g.$, $25°$C $\pm 5°$C

Device Models – contd.

- same device can have many different models
  - for different modes of operation, *e.g.*, analog vs. digital, static (dc) vs. dynamic (ac)
  - very simple models for hand analysis (EE101)
  - more complex and accurate models for computer simulation

Analog versus digital models

analog models assume that voltages and currents change over a range of real numbers, $e.g.$, voltage vary from -12 to $12\mathrm{V}$

- necessary for interfacing to real world signals, $e.g.$, audio, video, sensors, ...
- models are in the form of continuous functions relating terminal voltages and currents, $e.g.$, $v = iR$ for a resistor

digital models assume voltages can only take one of two values called logic levels, $e.g.$, $0\mathrm{V}$ corresponds to logic level 0 and $3.3\mathrm{V}$ corresponds to logic level 1

- hide details of actual voltage waveforms to simplify circuit design and functional verification of digital systems (need analog models to verify timing and power consumption)
- models are in the form of truth tables or boolean expressions

EE101 deals with analog circuits, digital circuits are discussed in other classes including EE121

we will discuss several analog models of digital circuits

Static versus dynamic models

static models assume that voltages and currents are constant, or change slowly, with time

- terminal voltages and currents are real constants (v, i, ...)
- device models are typically *algebraic* equations relating v, i

Example: simple resistor, with $v = iR$

dynamic models account for time-varying terminal voltages and currents

- terminal voltages and currents are functions of time ($v(t)$, $i(t)$, ...)
- device models are typically *differential* or *integral* equations relating $v(t)$, $i(t)$

Example: simple capacitor, with

$$i(t) = C\frac{dv(t)}{dt}$$

for the next few weeks we will concentrate on static models

Where do models come from?

circuit and device models come from

- physics (*e.g.*, E&M, semiconductor physics, . . .)
- empirical measurements of devices
- combination of both

in EE101 we manipulate and study circuit models that you will learn about **elsewhere** (*e.g.*, EE111, 112 . . .)

- it is not necessary to understand in detail the origin of a model
- it is necessary to understand the limits of applicability of a model

Course Goals

- understand basic circuit analysis techniques
  - how to use them
  - where they apply
  - where they come from
- develop ability to analyze simple circuits 'by hand' using these techniques
- understand basic circuit theory and why it is useful
- learn a few things about 'real world' circuits through examples and homework problems

Course Topics

- Static (DC) circuits: **(T&R Ch. 1-4)**
  - **Static circuit models: resistors, diodes, voltage and current sources, opamp, bipolar and MOS transistors**
  - **Techniques for 'hand' analysis of circuits: series and parallel resistors, source transformation, equivalent resistance, diode circuits, simple transistor circuits**
  - **Introduction to circuit theory: general formulation of KCL and KVL, power conservation, branch relations**
  - **Circuits with linear elements and ideal sources: node voltage analysis, superposition, Thevenin and Norton equivalents, maximum power transfer, load line analysis**
  - **Small signal models and circuit analysis**
- Dynamic (AC) circuits: **(T&R Ch. 5.1-4, Ch. 6.1,2,4,8, Ch. 7.1-4, Ch. 8, Ch. 14.1-3, Ch. 12.1,2,4,5)**
  - **Dynamic circuit models: time varying sources, capacitor, inductor, opamp, MOS transistor**
  - **Natural and step response for RC and RL circuits: delay and power analysis in digital CMOS circuits, 'hand' analysis of natural and step response of linear circuits with a single capacitor or inductor, charge sharing**
  - **Sinusoidal steady-state analysis: impedance, 'hand' analysis of SSS circuits using node voltage analysis, superposition, and Thevenin and Norton equivalents. Energy and power analysis, , maximum power transfer**
  - **Introduction to frequency response: transfer function, Bode plots, frequency response of RC, RL and RLC circuits**

Lecture notes

- help organize and reduce note taking in lectures
- you will need to take some notes, *e.g.*, clarifications, solutions to most examples, and extra examples
- slide title indicates a topic that often continues over several consecutive slides (indicated by ... contd. in the slide titles)
- one column format should give you enough room for taking notes
- lecture notes + your notes should be sufficient, you may need to refer to books for more explanations or different approaches

Lecture Notes 2
Review

- Review of electrical quantities: charge, current, energy, voltage, power
- Associated reference directions, power flow
- Review of KCL, KVL
- Power conservation

Electrical Quantities

the most fundamental physical quantities in circuits are **charge** measured in Coulombs (Coul) and **energy** measured in Joules (J)

in the analysis of circuits we typically deal with **current** in Amperes (A), **voltage** in Volts (V) and **power** in Watts (W)

charge (Q) comes in discrete quantities (multiples of electron charge 1.6×10^{-19}Coul) and can be both $(+)$ and $(-)$

we encounter charge over a very wide range from femto Coulombs (fCoul), $i.e.$, 10^{-15}Coul, to several Coulombs

examples:

charge in a modern DRAM cell (when 1 is stored)	30 fCoul
charge on power supply capacitor	5 mCoul
charge of lightning bolt	3000 Coul

Current (i)

charge flow or the change in charge per unit time, $i.e.$, $i = \frac{dQ}{dt}$ measured in Amperes (A) = Coul/sec

we encounter currents ranging from fAs to hundreds of Amps

examples:

transistor leakage currents in an IC	fA
transistor signal currents in an IC	$\mu\mathrm{A}$ – mA
power supply currents in ICs	$100\mathrm{mA}$ – $10\mathrm{A}$
LED indicator lamp	$10\mathrm{mA}$ – $100\mathrm{mA}$
small appliances, lamps	$1\mathrm{A}$ – $10\mathrm{A}$
residential receptacle limit	$20\mathrm{A}$
residential service	$100\mathrm{A}$
commercial/ light industrial service ($i.e.$, big 0000 wires or bus bars)	$1000\mathrm{A}$

Voltage (v)

electric potential in Volts (V) or the change in energy E per unit charge Q, *i.e.*,

$$v = \frac{dE}{dQ}\ \mathrm{J/Coul\ or\ V}$$

we encounter voltages ranging from microvolts ($\mu\mathrm{V} = 10^{-6}\mathrm{V}$) to kilovolts ($\mathrm{kV} = 10^{3}\mathrm{V}$)

examples:

antenna signal	$1\mu\mathrm{V}$
microphone signal (quiet source)	$1\mu\mathrm{V}$
"line" level audio signal (CD player)	$100\mathrm{mV}$
supply voltage for an IC	$1.8\mathrm{V}$ to $12\mathrm{V}$
car battery	$10\mathrm{V}$
residential power	$100\mathrm{V}$
local power transmission, color monitor	
accelerator voltage	$10\mathrm{kV}$
serious power transmission	$> 100\mathrm{kV}$

- breakdown voltage in air is about $700\mathrm{V/mm}$ (depends on humidity, etc.)
- $< 50\mathrm{V}$: usually safe
- $> 200\mathrm{V}$: treat with *extreme* respect

Power (p)

energy flow in Watts (W), $i.e.$,

$$p = \frac{dE}{dt}\ \mathrm{J/sec\ or\ W}$$

in terms of voltage v and current i,

$$p = \frac{dE}{dQ}\frac{dQ}{dt} = vi\ \mathrm{W}$$

we encounter powers ranging from picowatts ($1\mathrm{pW} = 10^{-12}\mathrm{W}$) to gigawatts ($1\mathrm{GW} = 10^{9}\mathrm{W}$)

examples:

power output of microphone (quiet source)	pW
ICs	$\mu\mathrm{W}$ to several Ws
residential lamp	$100\mathrm{W}$
theatrical lamp or space heater	$1\mathrm{kW}$
residential service maximum	$25\mathrm{kW}$
coliseum rock-and-roll sound system total output	$50\mathrm{kW}$
large radio transmitter	$100\mathrm{kW}$
coliseum rock-and-roll lighting system	$250\mathrm{kW}$
large power plant output	$1\mathrm{GW}$

Reference directions and polarities

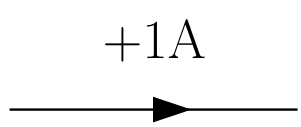
statements such as

- '$2\mathrm{A}$ flows through resistor R_{13}'
- '$-8\mathrm{V}$ is across resistor R_{27}'

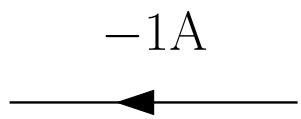
are *ambiguous* until we specify

- the direction of current flow that we consider positive
- which terminal has a higher potential when we say the voltage is positive

we use a small arrow marker to specify the *reference direction* for current:



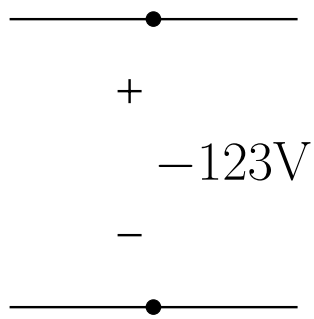
which is the same as



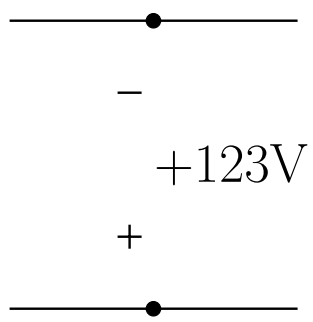
note that the arrow marker *does not* indicate the direction of current flow; it indicates the direction of current flow when the current is positive

Reference directions – contd.

we use $+$ and $-$ marks to identify the polarity of a voltage between two nodes:



which is the same as

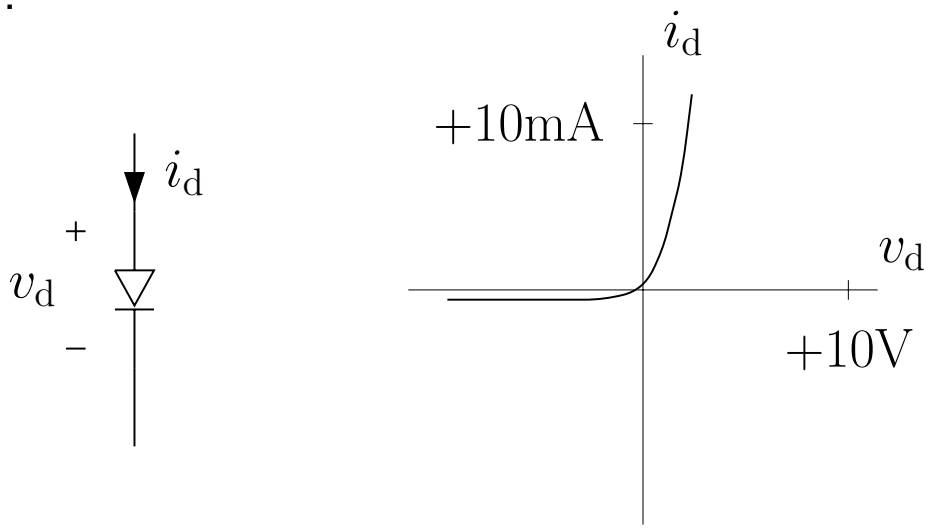


voltmeters have $+/-$ (or red/black) marks on their terminals, to show polarity

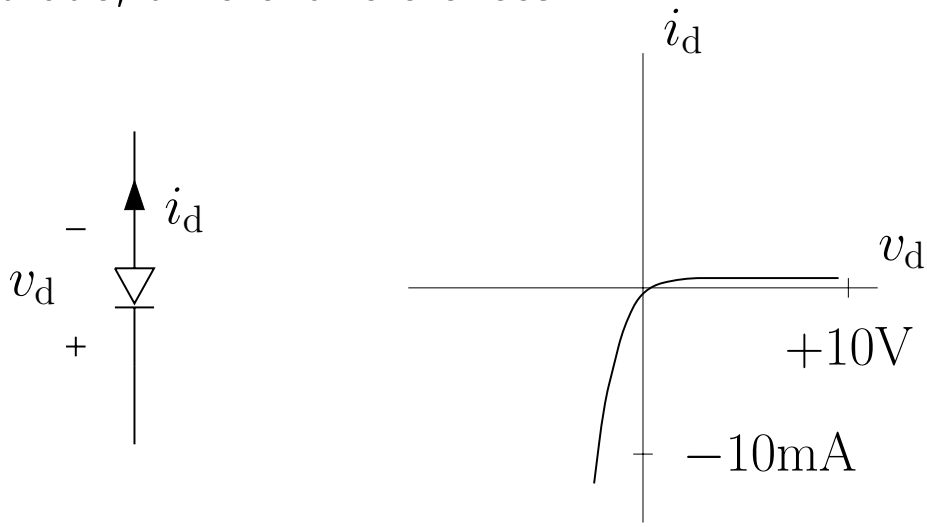
note that the $+$ mark *does not* indicate the node with higher potential (unless the voltage is positive)

Reference directions – contd.

we must show reference marks when we describe a device model!



same diode, different references:

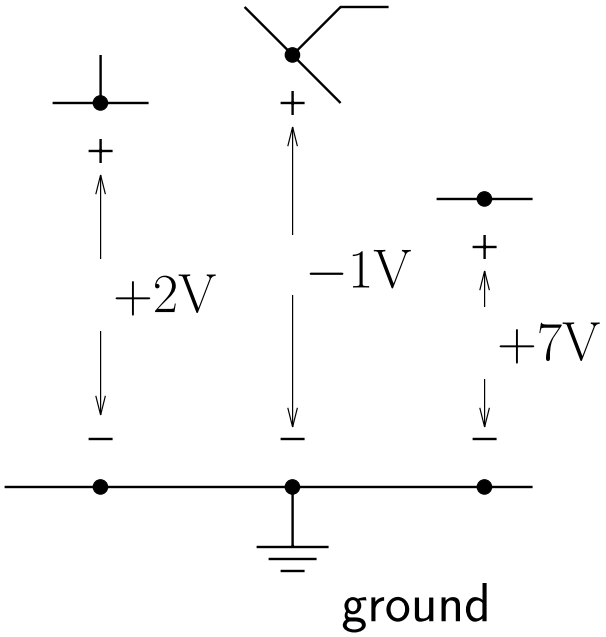


note that

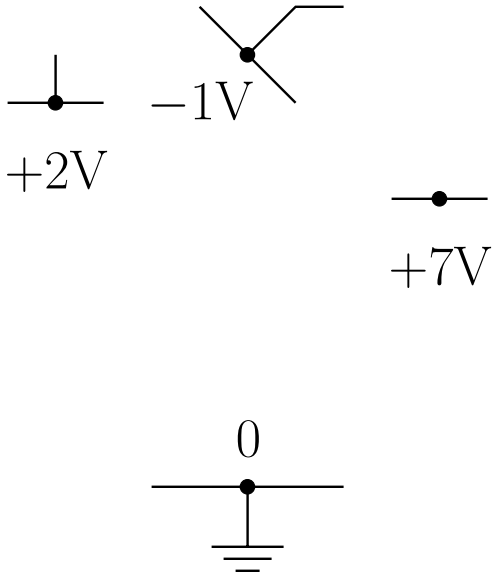
- solid arrow shows reference direction
- arrow in schematic symbol shows physical orientation of device

Common (ground) node

often we have a common − reference for voltages in a circuit, called the *common* node, or *ground* node:

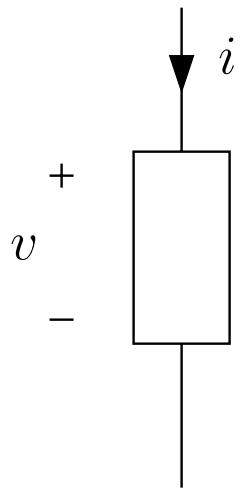


in this case we just show the voltage difference to ground, or *node potentials:*



Associated (passive) reference directions

a common and useful convention for a two-terminal device or *circuit branch:*
current reference direction points *into* + voltage reference terminal:



in this case we say the current and voltage reference directions are *associated* or *passive*
with associated reference directions, $p = vi$ is the electrical power flowing *into* device
(from the rest of the circuit)

- $p > 0$ means electrical power is dissipated or absorbed in the device, turned into some other form (heat, light, motion, etc.)
- $p < 0$ means electrical power is generated by or supplied by the device
  (presumably from some other form!)

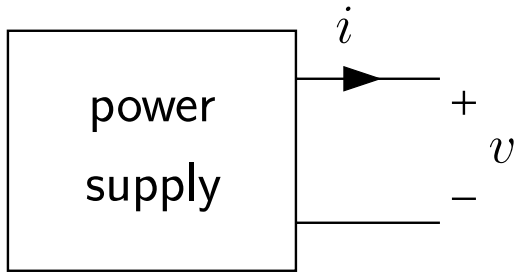
Associated reference directions – contd.

Common *exceptions* to associated reference convention:

- batteries
- power supplies
- generators

(which, in normal operation, supply or generate power)

in these cases, the common convention is to reverse associated directions:

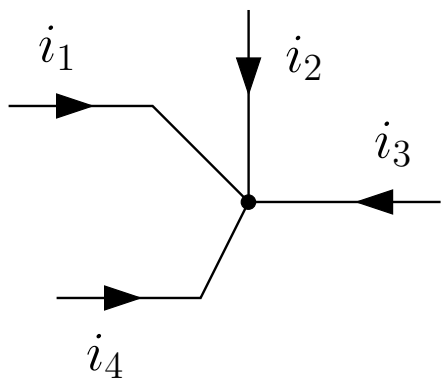


here, $p = vi$ is the power flowing *from* the device (power supply, battery, $etc.$) into the rest of the circuit
(and is positive in normal operation)

Review of KCL

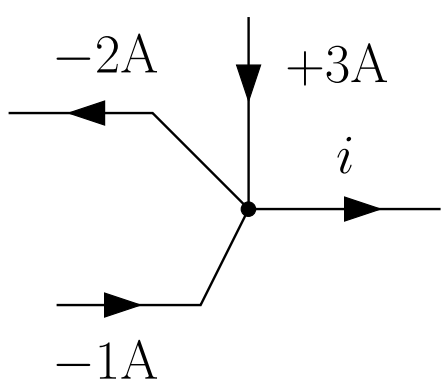
Khirkoff's current law (KCL): sum of all currents flowing into a node is zero
KCL is a direct consequence of *charge conservation* (an ideal node cannot store charge)

'flowing into' means reference current directions point into node



$$i_1 + i_2 + i_3 + i_4 = 0$$

Example:



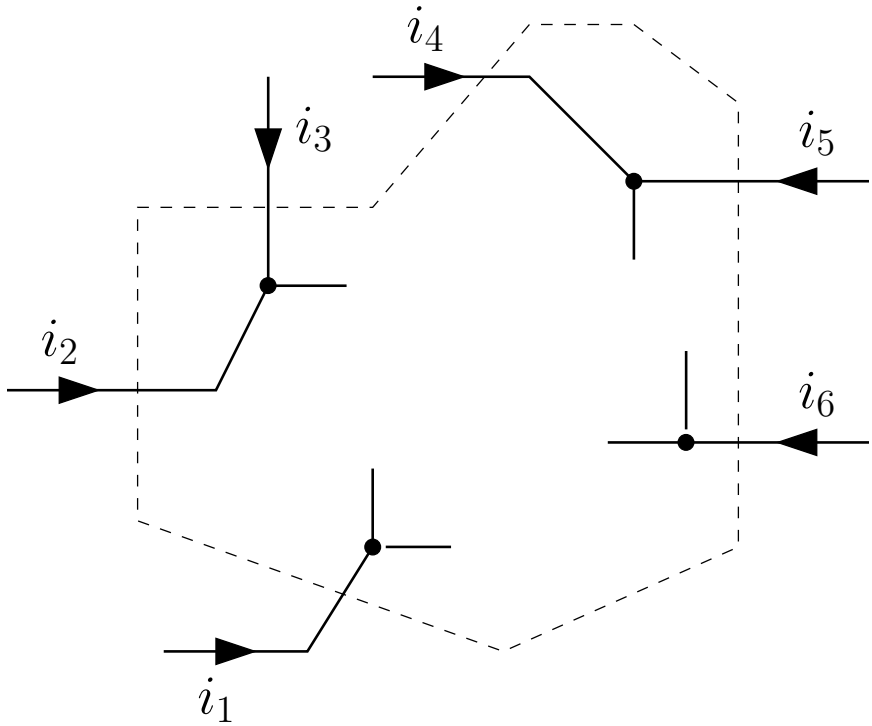
what is i?

KCL: $-(-2\mathrm{A}) + (-1\mathrm{A}) + (3\mathrm{A}) - i = 0$, so $i = 4\mathrm{A}$.

Review of KCL – contd.

an extension of KCL (that follows from KCL):

total current entering a region or part of a circuit (containing multiple nodes) is zero



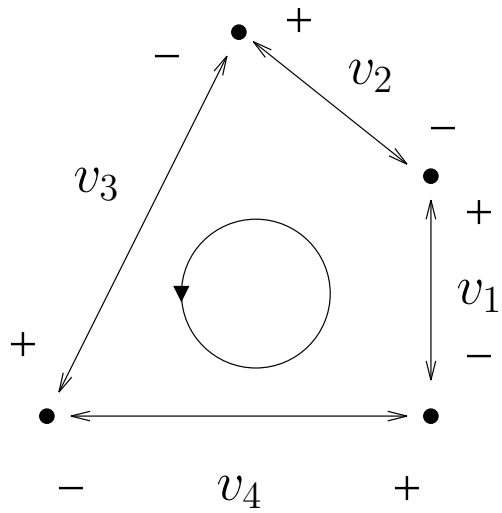
$$i_1 + i_2 + i_3 + i_4 + i_5 + i_6 = 0$$

to derive this extension:
add up KCL equations for all nodes inside region

Review of KVL

Khirkoff's voltage law (KVL): sum of voltage around a loop is zero
('around a loop' means the voltage reference directions all agree, $i.e.$, clockwise or counterclockwise)

KVL is a direct consequence of *energy conservation* (the work needed to move charge around a loop is zero)



$$v_1 + v_2 + v_3 + v_4 = 0$$

Review of KVL – contd.

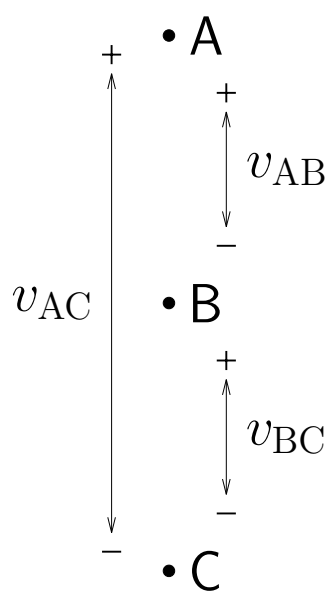
a second form of KVL is in terms of *voltage drops*

if A, B, and C are three nodes in a circuit

v_{AB} is the voltage drop from node A to node B
v_{BC} is the voltage drop from node B to node C
v_{AC} is the voltage drop from node A to node C

then

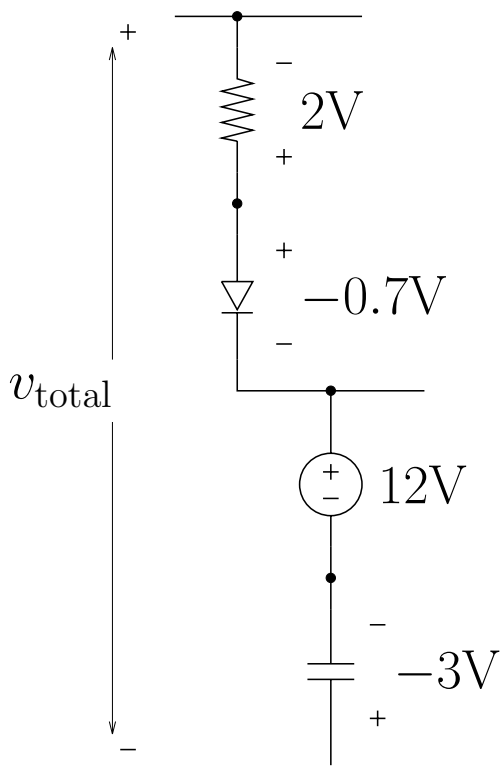
$v_{\mathrm{AC}} = v_{\mathrm{AB}} + v_{\mathrm{BC}}$



a third form of KVL says that the voltage across a device is the difference of its terminal node potentials (voltages to ground), *i.e.*, $v_{\mathrm{AB}} = e_{\mathrm{A}} - e_{\mathrm{B}}$

Review of KVL – contd.

Example:



$$v_{\text{total}} = -(2\text{V}) + (-0.7\text{V}) + (12\text{V}) - (-3\text{V}) = +12.3\text{V}$$

these three forms of KVL

- sum of voltages around loop is zero
- $v_{\text{AC}} = v_{\text{AB}} + v_{\text{BC}}$
- node potentials: $v_{\text{AB}} = e_{\text{A}} - e_{\text{B}}$

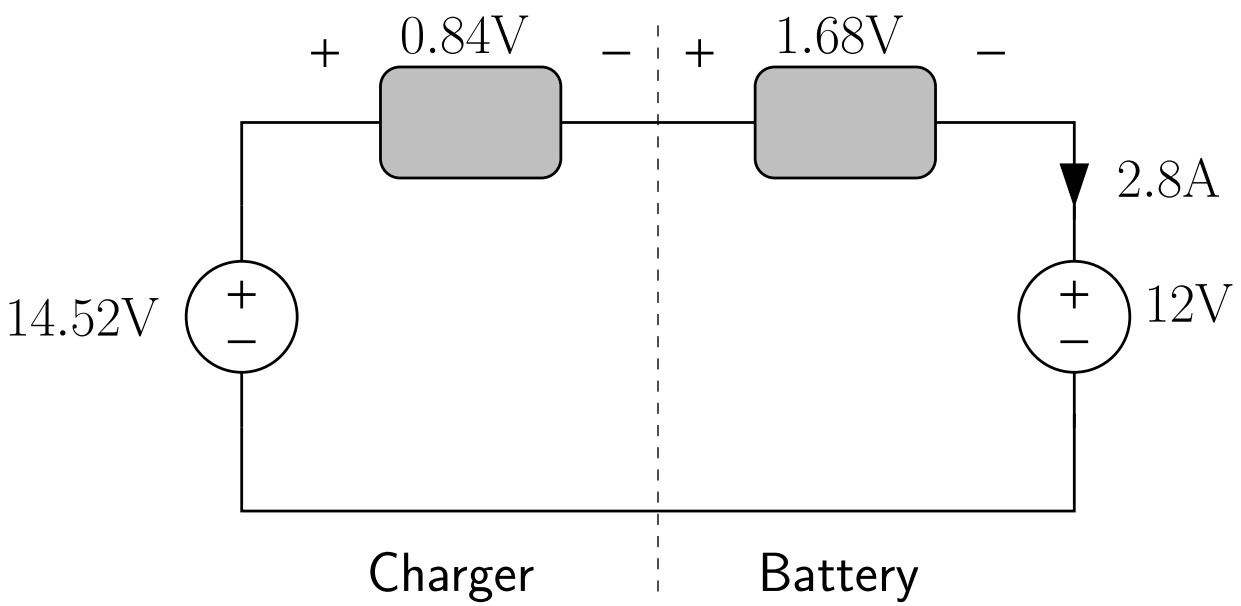
are *equivalent* – from each one we can derive the other two

Power Conservation

a consequence of KCL and KVL (as we shall mathematically prove later) is that:

in any circuit, the total power dissipated (or absorbed) equals the total power supplied (or generated)

Example: *Battery Charger*

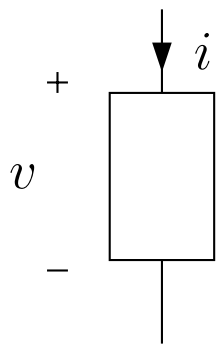


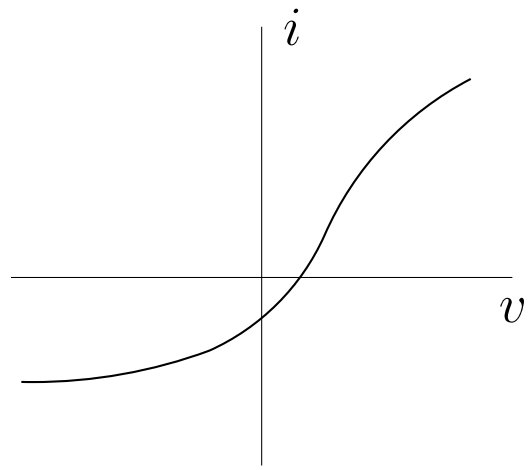
- find the power delivered to the battery
- verify power conservation

Lecture Notes 3
Basic Analysis of Static Circuits

- two-terminal static circuit elements
  - linear and nonlinear resistors
  - voltage and current sources
  - diodes: ideal, exponential
  - linearity and passivity
- basic (hand) analysis techniques
  - resistors in series and parallel
  - source transformation
  - diode circuit analysis

Two-terminal static element

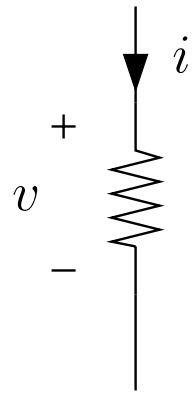


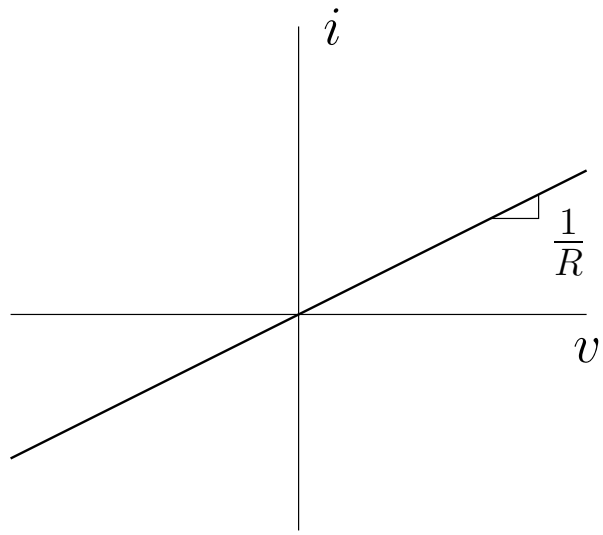


the element is specified via a relationship between v and i expressed as a graph, table, or function $i = f(v)$ with respect to some v and i reference directions

model must also specify the range of v or i (and other variables, $e.g.$, temprature) where it is applicable

Linear resistor





- Ohm's law: $v = iR$

  units of *resistance* are $\mathrm{V/A} = \Omega$ (ohm)

- material resistivity (resistance of a 1cm cube of the material) varies over a very wide range

superconductors	0Ω
conductors, $e.g.$, copper, alluminum	10^{-6} to $10^{-3}\Omega$
semiconductors, $e.g.$, silicon	$10^{5}\Omega$
insulator	$10^{18}\Omega$

- alternate description: $i = Gv$

  units of *conductance* are $\mathrm{A/V}$ (mho).

- electrical power $p = iv = i^2R = v^2/R$ is always dissipated in resistor

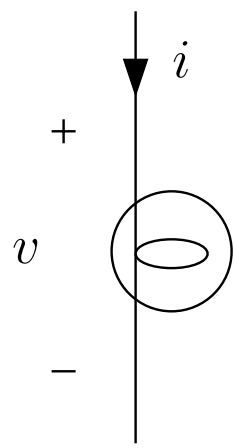
Linear resistor – contd.

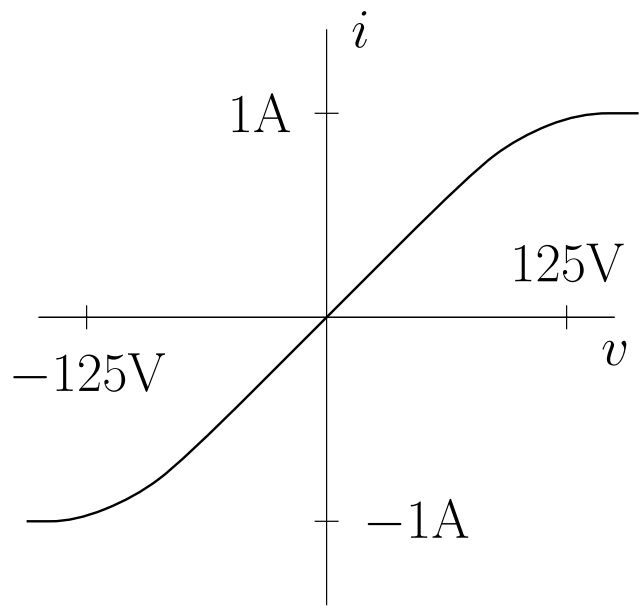
- two important special cases
  - *short circuit*, $R = 0$
  - *open circuit*, $R = \infty$

- linear resistor is good model of real resistors, $e.g.$, carbon resistors, as long as the voltage and frequency of operation are low enough

Nonlinear resistor

some resistors, $e.g.$, filament lamp (light bulb) are operated such that the relationship between v and i is nonlinear

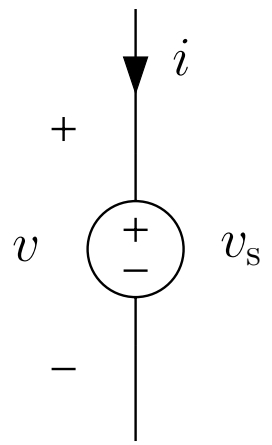


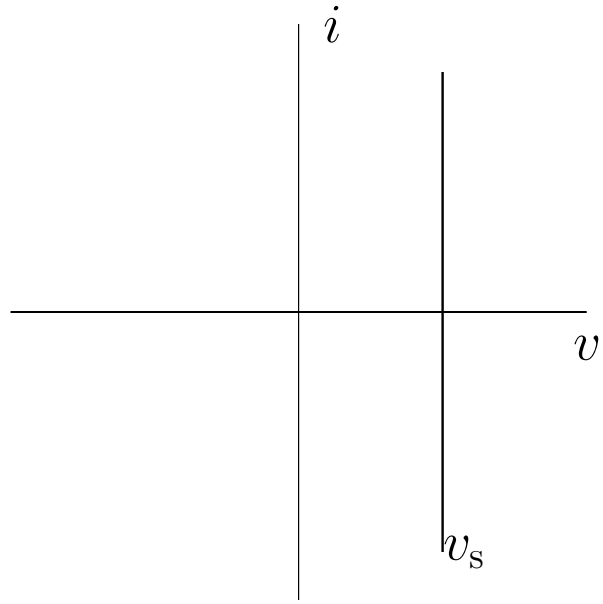


- reason for nonlinearity: filament resistance increases as it heats up
- *Stanford historical note:* Hewlett and Packard's original innovation was using a filament lamp in an oscillator to regulate amplitude

(Ideal) voltage source

model: $v = v_{\mathrm{s}}$ (which is the *source voltage*)

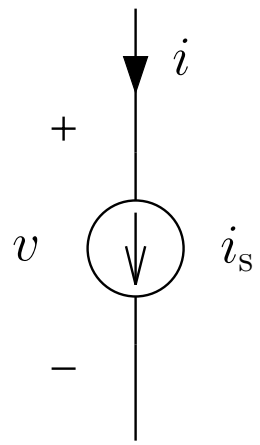


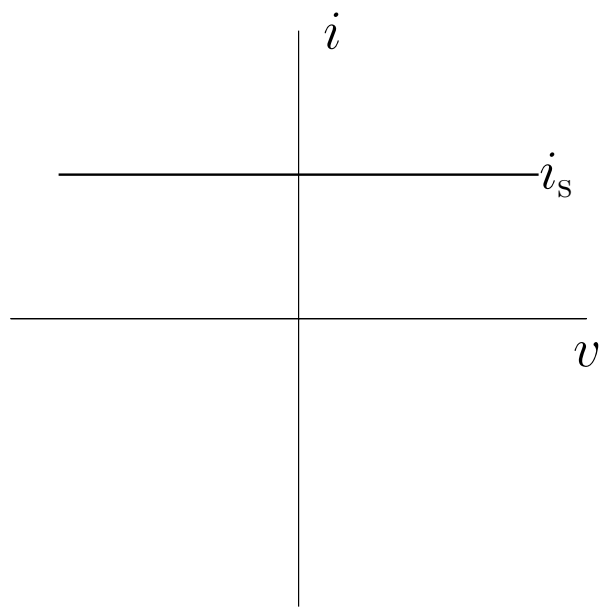


- voltage source maintains v_{s} across its terminals (supplying whatever current is necessary to do this!)
- the current and voltage references shown are the associated directions, which is not the convention for votage source
- when $v_{\mathrm{s}} = 0$, voltage source is a *short circuit* or (ideal) *wire*: no voltage drop across it, and arbitrary current flow
- since current i can have either sign, ideal voltage source can either dissipate power or supply it
- good model for a battery for very low current

(Ideal) current source

model: $i = i_{\mathrm{s}}$ (which is *source current*)

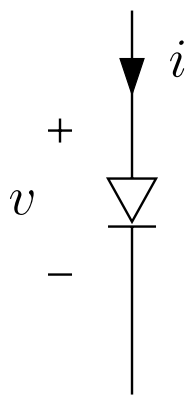


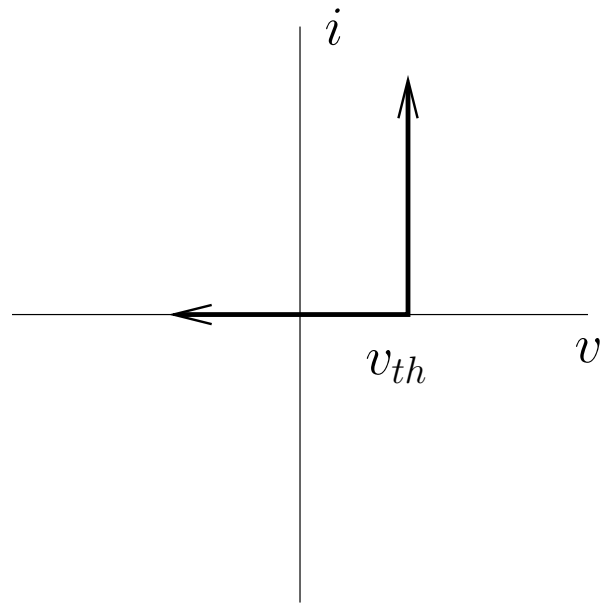


- current source maintains a current of i_{s} (using whatever voltage is necessary)
- when $i_{\mathrm{s}} = 0$, current source is an *open circuit*: no current flows through it, and it can support an arbitrary potential difference
- current source can either supply or dissipate power
- current sources are used in models of active devices, *e.g.*, transistors

Diode

basic idea: diode restricts current flow to one direction
simplest model is the **ideal diode** model:





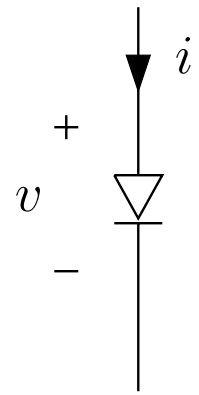
characterized by:

either $i \geq 0$ and $v = v_{th}$ or $v < v_{th}$ and $i = 0$

- when $i > 0$ we say diode is 'on', 'conducting', or 'forward biased'
- when $i = 0$ we say diode is 'off' or 'reverse biased'
- v_{th} is typically in the range from 0.4 to $0.7\mathrm{V}$
- ideal diode model is only an approximation of real diode behavior – useful for rough, hand calculations

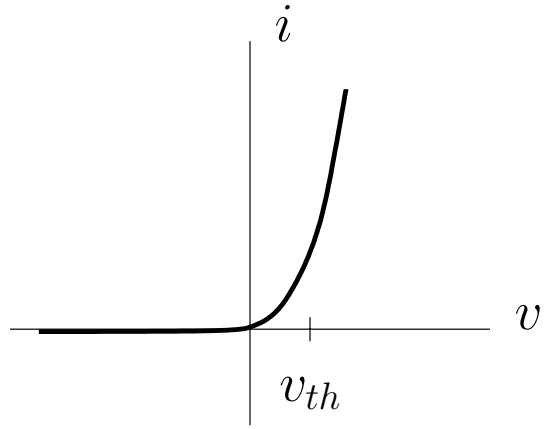
Exponential diode model

a more accurate model of a real (junction) diode:



$$i = i_0(e^{v/v_{\mathrm{T}}} - 1)$$

i_0 depends on the physical characteristics of the diode (reasonable range: $10^{-15}\mathrm{A}$ to $10^{-11}\mathrm{A}$) and $v_{\mathrm{T}} \approx 26\mathrm{mV}$



- should not confuse v_{th}, which is the voltage when the diode is "on" in the ideal model, with v_T
- model comes from device physics
- exponential model fails to capture some important properties of real diodes ($e.g.$, avalanche breakdown)
- the diode always dissipates power, since $p = vi \geq 0$

Linearity

a two-terminal device model is *linear* if v is a linear function of i, $i.e.$, $i = \alpha v$ for some constant α (including $i = 0$ and $v = 0$)

an equivalent definition is that the device v–i relation satisfy:

superposition: whenever (v,i) and $(\tilde{v}, \tilde{i})$ are possible terminal voltage/current pairs, $(v + \tilde{v}, i + \tilde{i})$ is also a possible terminal voltage/current pair, and

scaling: whenever (v,i) is a possible terminal voltage/current pair, and α is any real number, $(\alpha v, \alpha i)$ is also a possible terminal voltage/current pair

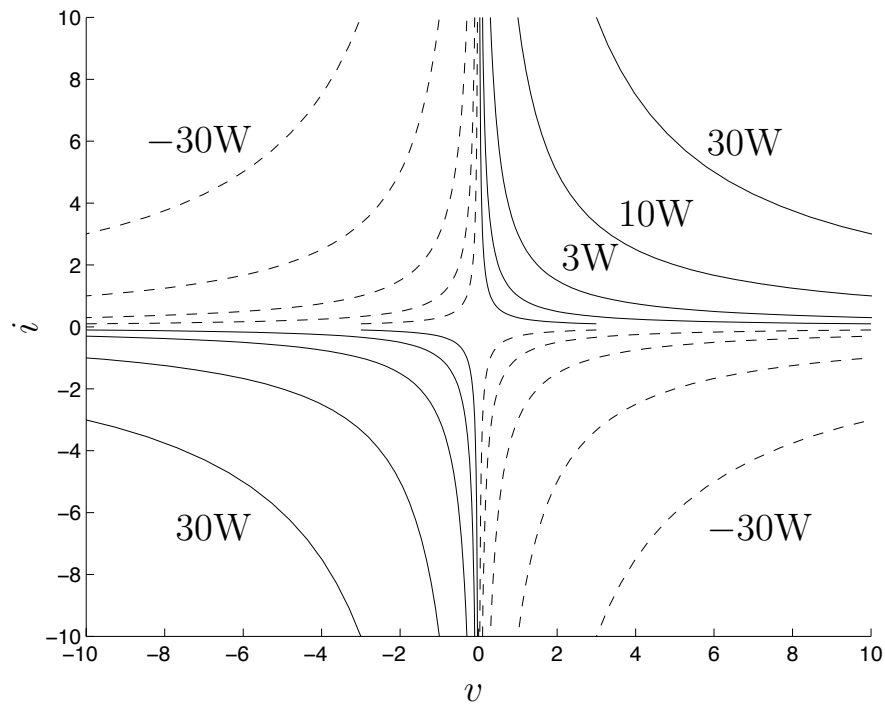
also equivalent to:

- $v - i$ relation of element is straight line through origin
- element is a resistor (with $+$ or - resistance, also open- and short-circuit)

Power dissipation

power dissipated in device is $p = vi$

on v – i plot, constant power curves are hyperbolas:



(contours for $\pm 1, \pm 3, \pm 10, \pm 30\mathrm{W}$ shown)

can find device operating voltage/current pairs by superimposing its v – i relation (see HW problem)

Passivity

an element is *passive* if $p = vi \geq 0$ for all possible v, i

- passive means electrical power always flows *into* device
- element is passive iff its $v - i$ curve lies in first and third quadrants only
- all elements we've seen (except sources) are passive (for resistor, assuming $R \geq 0$)
- voltage and current sources are *not* passive, since they can supply power

Basic static circuit analysis techniques

many practical circuits (with simple element models) can be analyzed by clever use of:

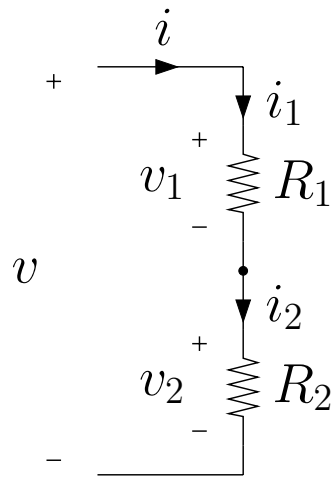
- KVL and KCL
- branch relations ($e.g.$, Ohm's law)
- tricks such as series/parallel resistor equivalent, voltage/current dividers, Δ - Y transformation, source transformation, $etc.$

while these tricks are good for small circuits, they are not good for hand analysis of large circuits (by hand or using computers)

later we'll present circuit formulations and analysis techniques that are better suited for computers and for hand analysis of large circuits

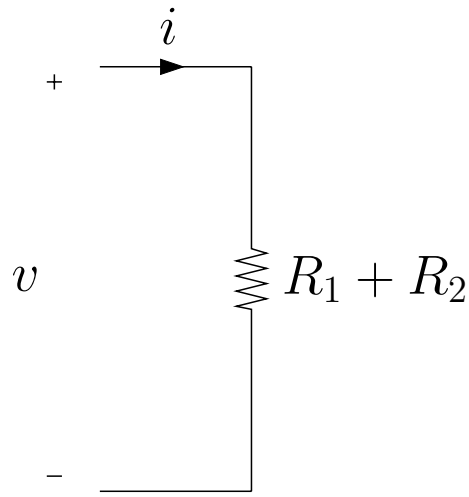
Resistors in series

resistors in series connection:



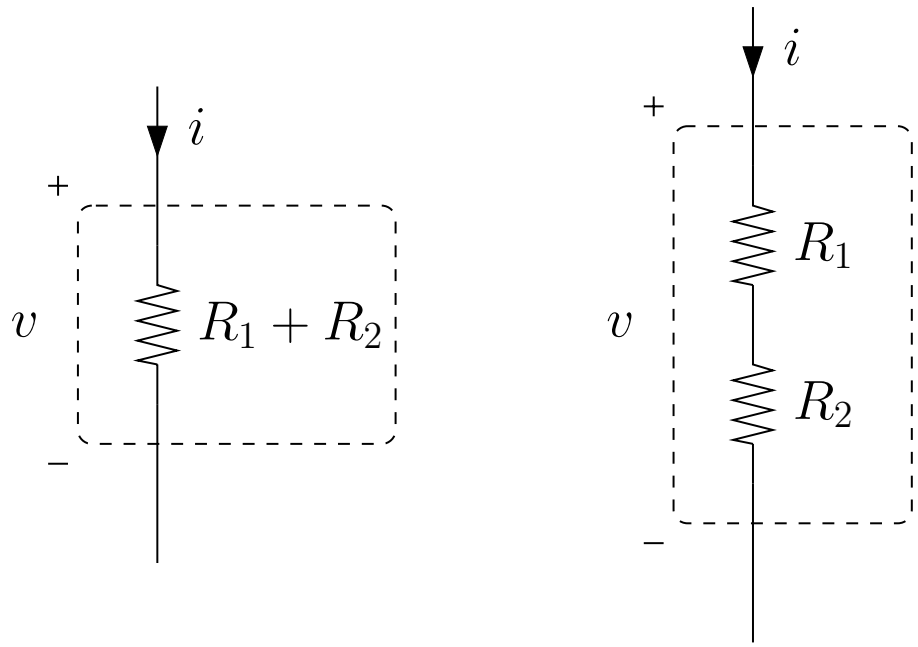
- by Ohm's law (resistor model), $v_1 = i_1 R_1$, $v_2 = i_2 R_2$
- by KCL at middle node, $i_1 - i_2 = 0$, *i.e.*, $i = i_1 = i_2$
- by KVL, $v = v_1 + v_2$

eliminating i_1, i_2, v_1, v_2, we get $v = i(R_1 + R_2)$, *i.e.*, the v – i relation of a resistor with resistance $R_1 + R_2$:



Resistors in series – contd.

series connection of resistances R_1 and R_2 is *(electrically) equivalent* to a single resistance $R_1 + R_2$

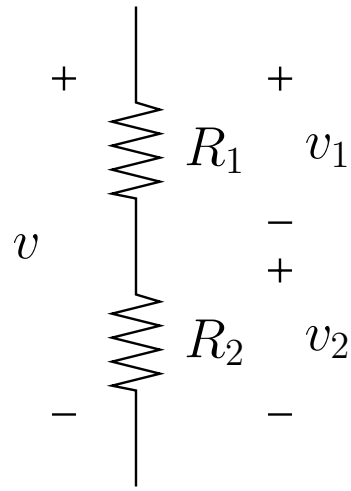


What does this mean?

- they have the same $v - i$ relation
- no electrical measurement *outside* the boxes could distinguish the two
- one box can be substituted for the other, in any circuit, without affecting the circuit

Voltage divider principle

for two resistors in series,

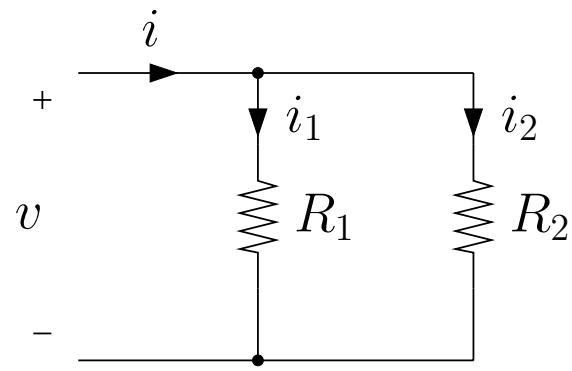


$$v_1 = \frac{R_1}{R_1 + R_2} v, \quad v_2 = \frac{R_2}{R_1 + R_2} v$$

voltage across resistors in series divides as element resistance / total resistance

Resistors in parallel

parallel connection:



- Ohm's law: $v = i_1 R_1 = i_2 R_2$
- KCL: $i = i_1 + i_2$

so

$$i = \frac{v}{R_1} + \frac{v}{R_2} = v(\frac{1}{R_1} + \frac{1}{R_2}),\ i.e.,$$
$$v = i\frac{1}{1/R_1 + 1/R_2} = i\frac{R_1 R_2}{R_1 + R_2}$$

resistances R_1, R_2 in parallel are equivalent to resistance

$$R_1 \| R_2 \triangleq \frac{R_1 R_2}{R_1 + R_2}$$

(read 'R_1 parallel R_2')

Resistors in parallel – contd.

in terms of conductances, we have

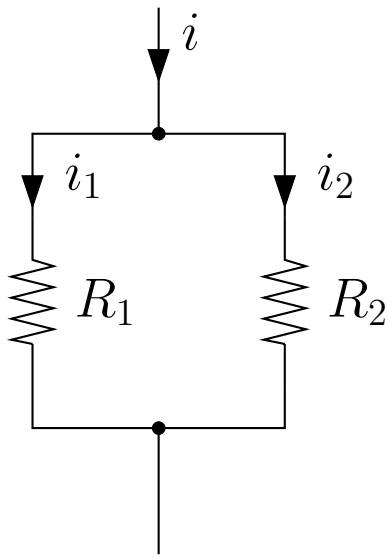
$$1/(R_1 \| R_2) = 1/R_1 + 1/R_2$$

$i.e.$, in parallel, *conductances add*

- (provided $R_1 > 0$, $R_2 > 0$) $R_1 \| R_2$ is smaller than both R_1 and R_2
- $R \| R = \frac{1}{2} R$
- $R_1 \| R_2 \approx \min\{R_1, R_2\}$ if one resistance is much larger than the other ($e.g.$, $1\mathrm{k}\Omega \| 1\mathrm{M}\Omega \approx 1\mathrm{k}\Omega$)

Current divider principle

current i flowing through parallel resistors:



current divides as element conductance / total conductance:

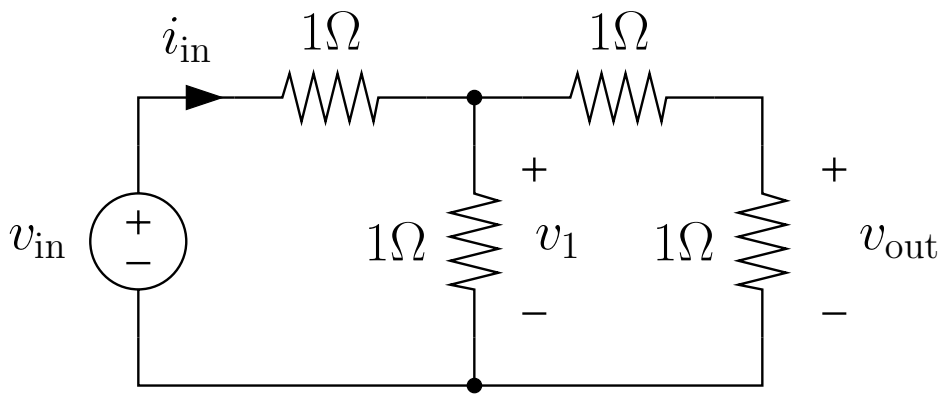
$$i_1 = \frac{G_1}{G_1 + G_2} i, \quad i_2 = \frac{G_2}{G_1 + G_2} i$$

where $G_1 = 1/R_1$, $G_2 = 1/R_2$

can also be expressed as

$$i_1 = \frac{R_2}{R_1 + R_2} i, \quad i_2 = \frac{R_1}{R_1 + R_2} i$$

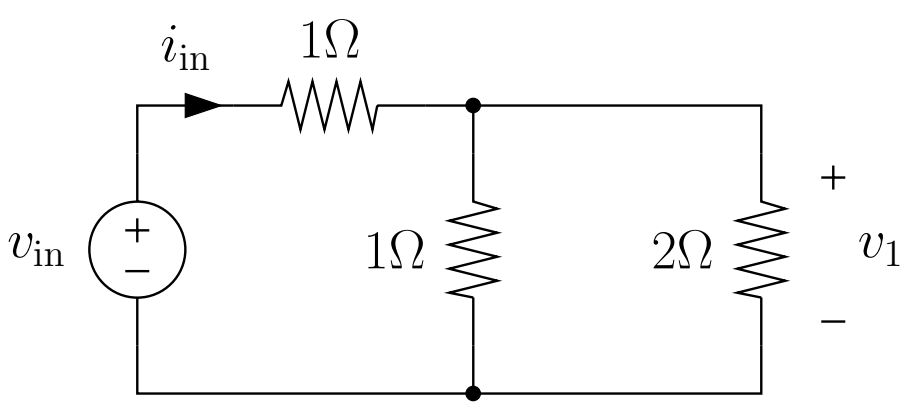
Example of 'hand' circuit analysis



find i_{in} and v_{out} in terms of v_{in}

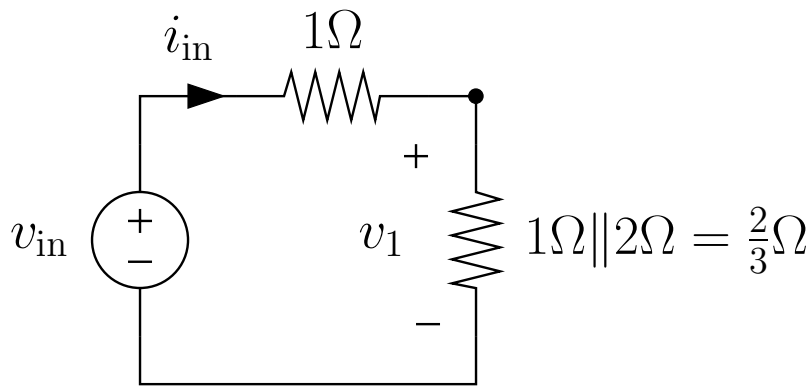
One way (there are many!):

1. by voltage divider, we have $v_{\text{out}} = v_1/2$
2. combine resistors in series at right to get



Example – contd.

3. now combine parallel connection to get

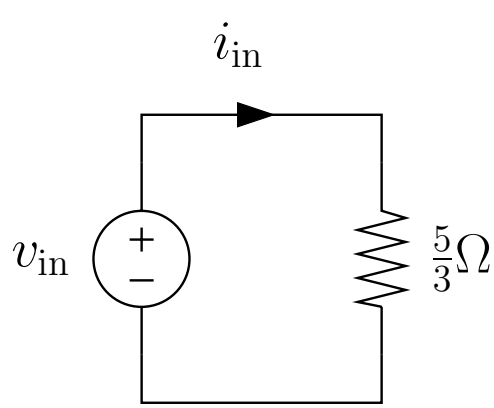


4. by voltage divider, we have

$$v_1 = \frac{2/3}{1 + (2/3)} v_{\text{in}} = (2/5) v_{\text{in}}$$

so with (1) we conclude $v_{\text{out}} = (1/5) v_{\text{in}}$

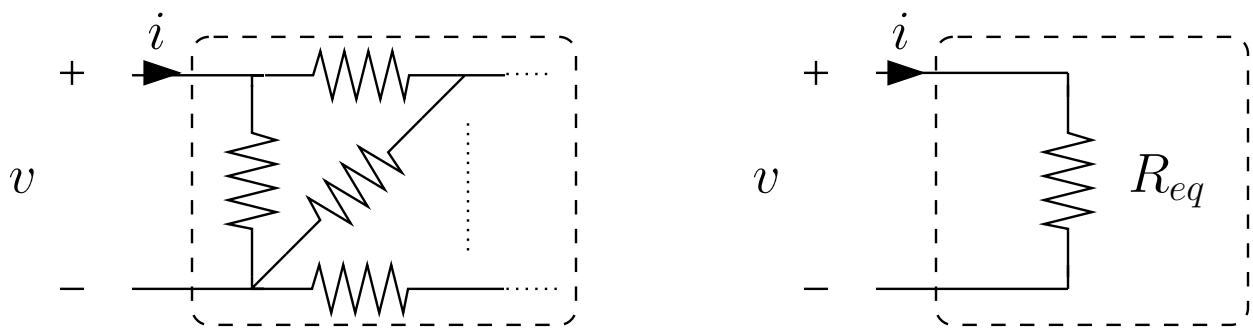
5. combine series connection to get



6. by Ohm's law we have $i_{\text{in}} = v_{\text{in}} / \frac{5}{3}\Omega$

Equivalent resistance

any two-terminal circuit consisting only of resistors is (electrically) equivalent to a single resistor

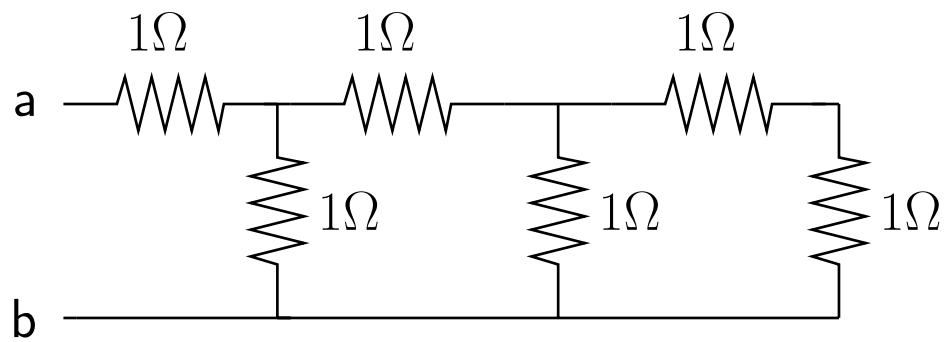


this is a consequence of the linearity of the resistor relation (Ohm's law), KCL, and KVL (more on this later)

Finding R_{eq}

first method: use series/parallel resistance equivalences

Example:

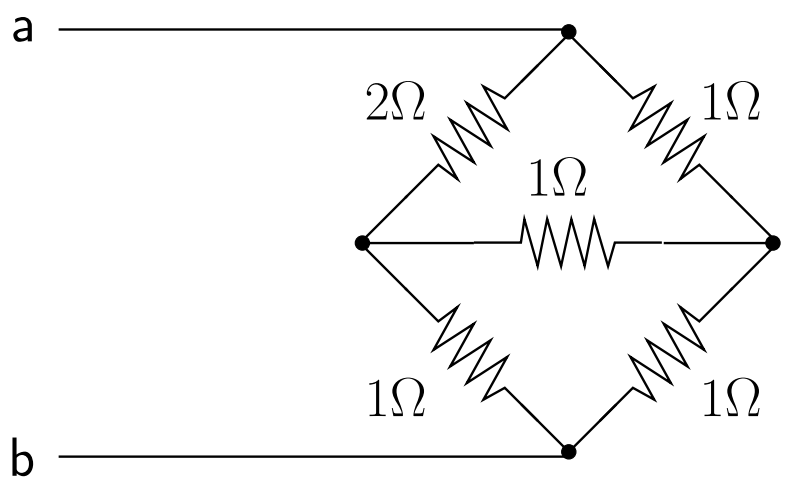


find R_{eq}

Finding R_{eq} – contd.

for some resistor circuits series/parallel reductions may not be possible

Example:



find R_{eq}

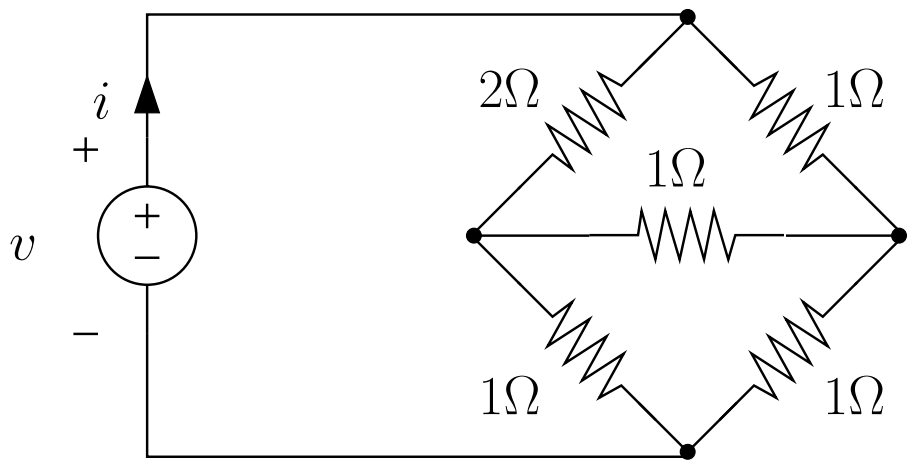
how can we find R_{eq} in this case ?

second method: we apply voltage (or current) source v to the input and find the resulting current i (or voltage)

$$R_{eq} = \frac{v}{i}$$

Finding R_{eq} – contd.

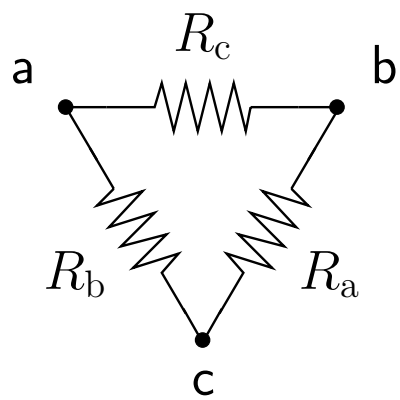
for our example

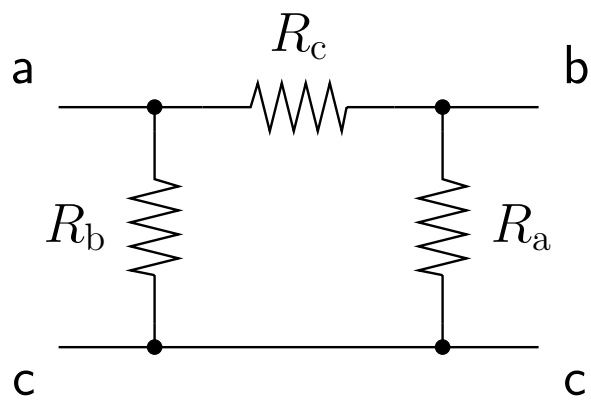


$\triangle$ – Y transformation

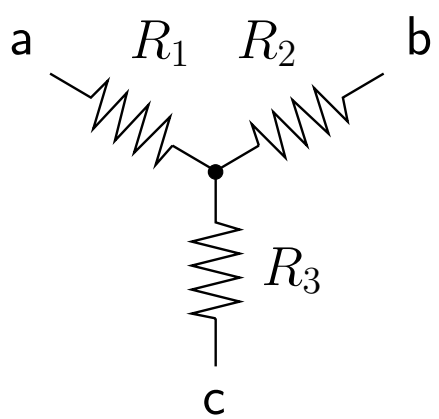
another useful trick

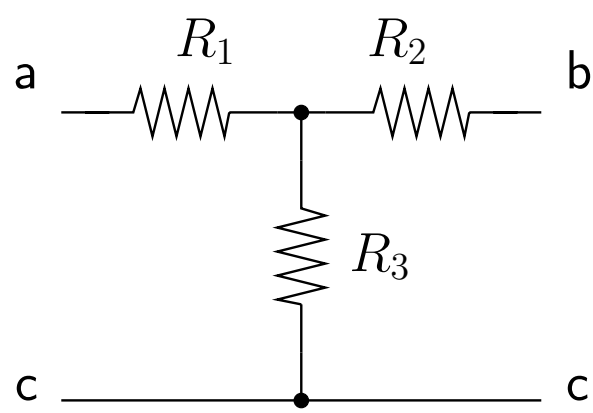
$\triangle$ or Π connection of resistors:





Y or T connection of resistors:





$\triangle$ – Y transformation – contd.

are equivalent provided:

$$
\begin{aligned}
R_1 &= \frac{R_\mathrm{b} R_\mathrm{c}}{R_\mathrm{a} + R_\mathrm{b} + R_\mathrm{c}} \\
R_2 &= \frac{R_\mathrm{a} R_\mathrm{c}}{R_\mathrm{a} + R_\mathrm{b} + R_\mathrm{c}} \\
R_3 &= \frac{R_\mathrm{a} R_\mathrm{b}}{R_\mathrm{a} + R_\mathrm{b} + R_\mathrm{c}}
\end{aligned}
$$

(this is called the $\triangle \rightarrow$Y transformation)

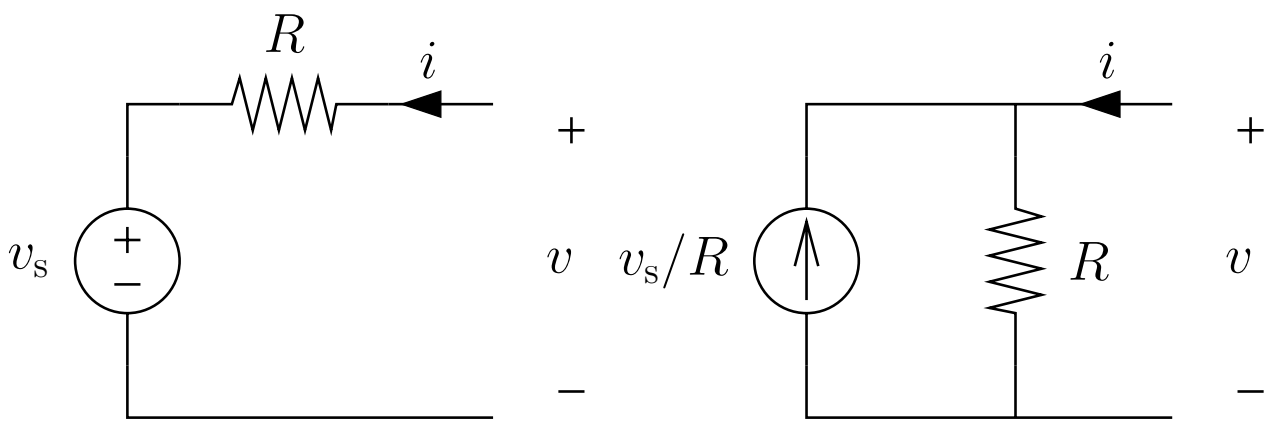
or, the other way around:

$$
\begin{aligned}
R_\mathrm{a} &= \frac{R_1 R_2 + R_2 R_3 + R_1 R_3}{R_1} \\
R_\mathrm{b} &= \frac{R_1 R_2 + R_2 R_3 + R_1 R_3}{R_2} \\
R_\mathrm{c} &= \frac{R_1 R_2 + R_2 R_3 + R_1 R_3}{R_3}
\end{aligned}
$$

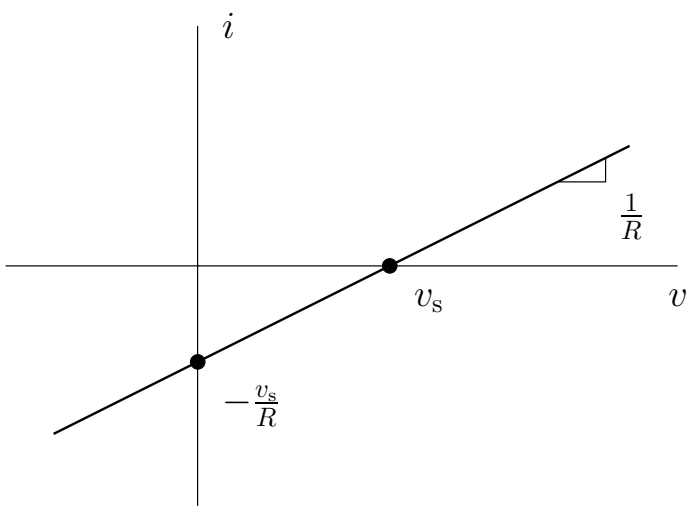
(this is called the Y$\rightarrow \triangle$ transformation)

Source transformation

series combination of voltage source v_s and resistor R is equivalent to parallel combination of current source v_s/R and resistor R



both circuits have the v – i relation: $v = v_\mathrm{s} + iR$:

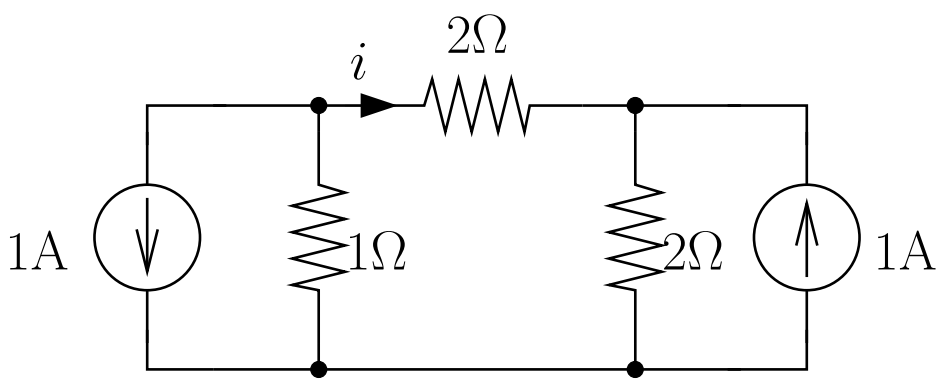


Source transformation – contd.

two pathologies:

- when the circuit is a voltage source, there is no current source circuit equivalent
- when the circuit is a current source, there is no voltage source equivalent

Example:



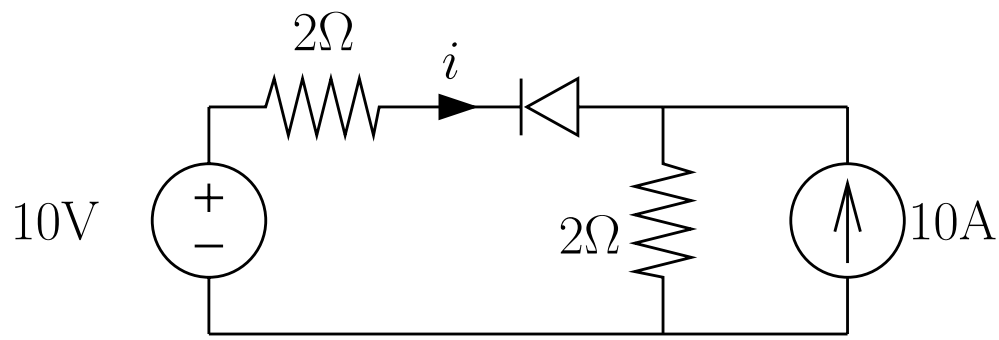
find i

Hand analysis of diode circuits

for hand analysis we typically assume the ideal diode model

- we assume that the diode is on (or off) and replace it by voltage source v_{th} (or by an open circuit)
- we analyze the circuit to see if our assumption is correct
- if we get an inconsistency, we know that the diode must be in the opposite state – we set the diode to the opposite state and reanalyze the circuit

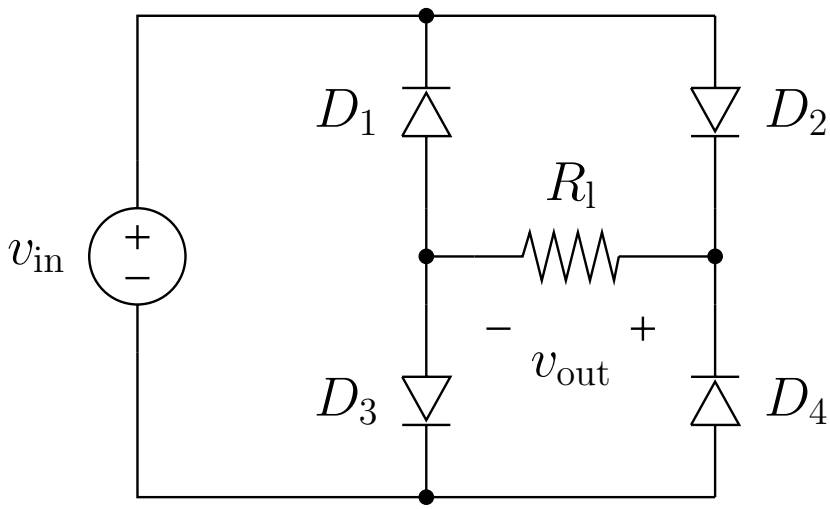
Example:



find i assuming the ideal diode model with $v_{th} = 1\text{V}$

Application: diode bridge

also called full wave rectifier – used in AC to DC converters



let's find v_out assuming ideal diode model with $v_{th} = 0$

Application: diode bridge – contd.

careful (& boring) analysis

there are sixteen possibilities: each diode 'on' ($v = 0$, $i \geq 0$) or 'off' ($v < 0$, $i = 0$)

Case I: all diodes off
all diode currents zero $\Rightarrow$ load current zero $\Rightarrow v_{\mathrm{out}} = 0$
but $v_{\mathrm{out}} = -v_{\mathrm{D}_2} - v_{\mathrm{D}_1} > 0$, so Case I cannot occur

Case II: D_1 on; D_2, D_3, D_4 off.
$i_{\mathrm{R_L}} = i_{\mathrm{D}_2} + i_{\mathrm{D}_4} = 0$ so $v_{\mathrm{out}} = 0$
but $v_{\mathrm{out}} = -v_{\mathrm{D}_3} - v_{\mathrm{D}_4} > 0$, a contradiction, this case also cannot occur

. . . skipping some cases . . .

Case X: D_1 on, D_2 off, D_3 off, D_4 on.
(This one turns out to be possible!)
Since $v_{\mathrm{D}_1} = v_{\mathrm{D}_4} = 0$ we have

$$v_{\mathrm{out}} = -v_{\mathrm{in}}, \quad v_{\mathrm{D}_2} = v_{\mathrm{in}}, \quad v_{\mathrm{D}_3} = v_{\mathrm{in}}$$

so we get $v_{\mathrm{out}} = -v_{\mathrm{in}}$, $v_{\mathrm{in}} < 0$.

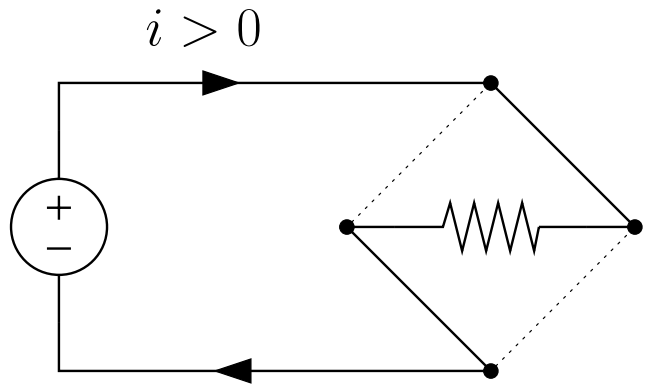
. . . skipping more cases . . .

Case XVI: all diodes on.
this yields $v_{\mathrm{in}} = v_{\mathrm{out}} = 0$

Application: diode bridge – contd.

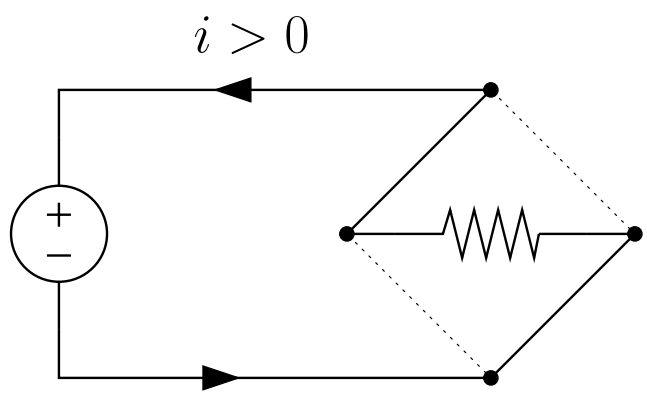
Intuitive analysis

for $v_{\text{in}} > 0$:



thus $v_{\text{out}} = v_{\text{in}}$

for $v_{\text{in}} < 0$:



thus $v_{\text{out}} = -v_{\text{in}}$

current always flows same way through resistor!

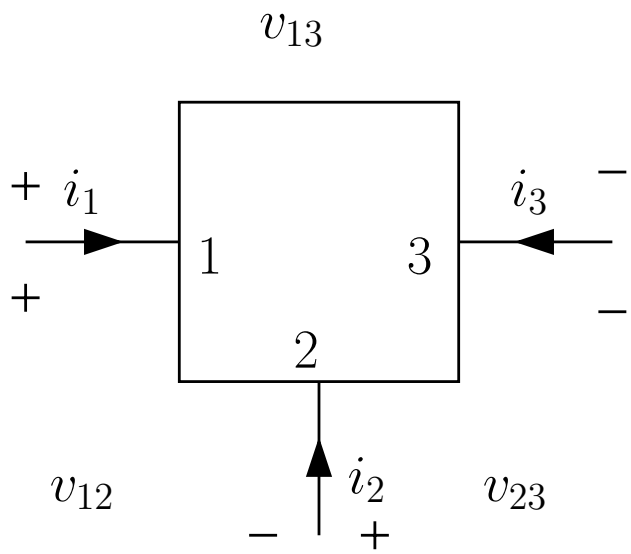
$v_{\text{out}} = |v_{\text{in}}|$

Lecture Notes 4
Multi-terminal static circuit elements

- dependent sources
- operational amplifiers (op-amps)
- transistors
- the CMOS inverter

Multi-terminal circuit element

some of the most important devices have three or more terminals, *e.g.*, transistors, op-amps



to specify a multi-terminal circuit element

- specify reference directions for terminal currents
- specify reference polarities for terminal voltages
- specify how the terminal voltages and currents are related
- the model must satisfy KCL and KVL, *e.g.*, for the three-terminal device in the figure

$$\begin{aligned} i_1 + i_2 + i_3 &= 0, \text{ and} \\ v_{12} + v_{23} - v_{13} &= 0 \end{aligned}$$

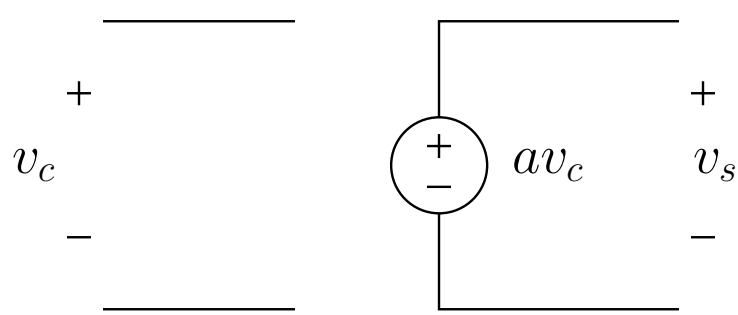
Dependent sources

a dependent source is an ideal voltage or current source whose value depends on (controlled by) the voltage or current at a different branch of the circuit

- dependent sources are used in modelling active devices, $e.g.$, transistors and amplifiers
- a dependent source is *linear* if its value is linear in the control branch's voltage or current

four flavors of linear dependent sources:

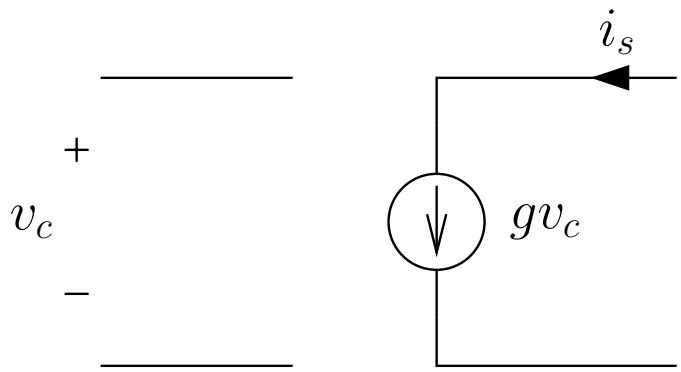
voltage controlled voltage source (VCVS or voltage amplifier)



a is called *voltage gain* (unitless)

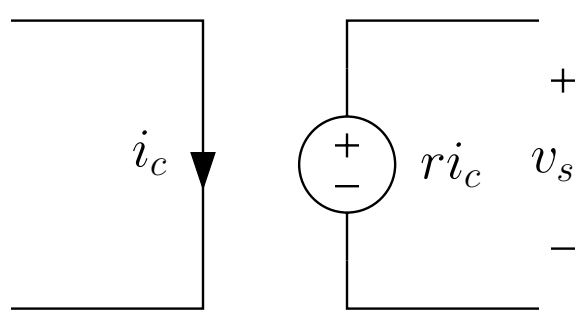
Dependent sources – contd.

voltage controlled current source (VCCS or transconductance amplifier)



g is called *transconductance*, and has units $\mathrm{A/V}$ or mho

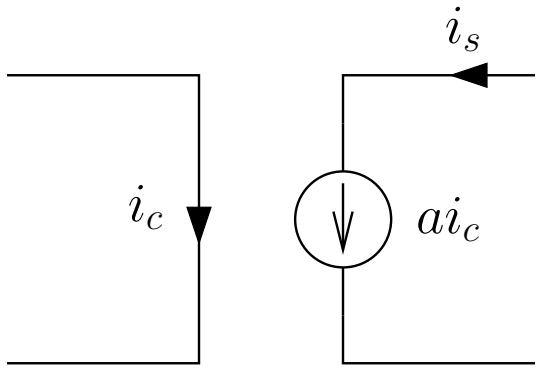
current controlled voltage source (CCVS or transresistance amplifier)



r is called *transresistance*, and has units $\mathrm{V/A} = \Omega$

Dependent sources – contd.

current controlled current source (CCCS or current amplifier)

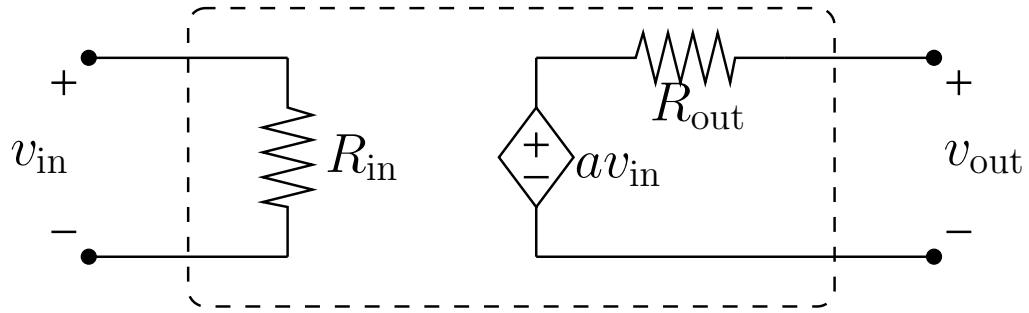


a is called *current gain* (unitless)

to distiguish dependent from (independent) sources we will always draw them as diamond

Linear voltage amplifier

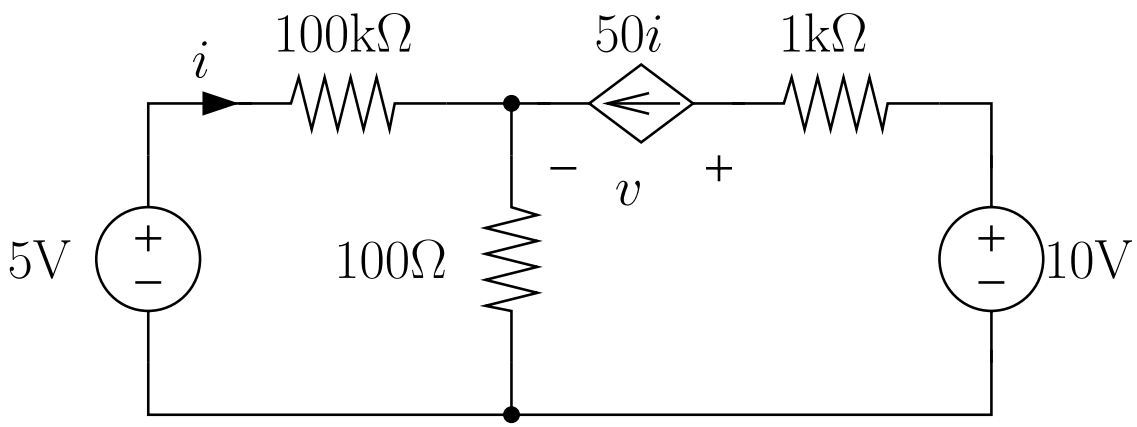
static model



examples:

- power audio amplifier (to speaker): $R_{\text{in}} \approx 10\text{k}\Omega$, $R_{\text{out}} \approx 0.1\Omega$, $a \approx 50$
- line-level audio amplifier (from CD): $R_{\text{in}} \approx 10\text{k}\Omega$, $R_{out} \approx 100\Omega$, $a \approx 5$
- line-level video amplifier (from VCR): $R_{\text{in}} \approx 75\Omega$, $R_{\text{out}} \approx 75\Omega$, $a \approx 10$
- op-amp: $R_{\text{in}} \approx 1\text{M}\Omega$, $R_{\text{out}} \approx 500\Omega$, $a \approx 10^6$

Example: linear bipolar transistor circuit

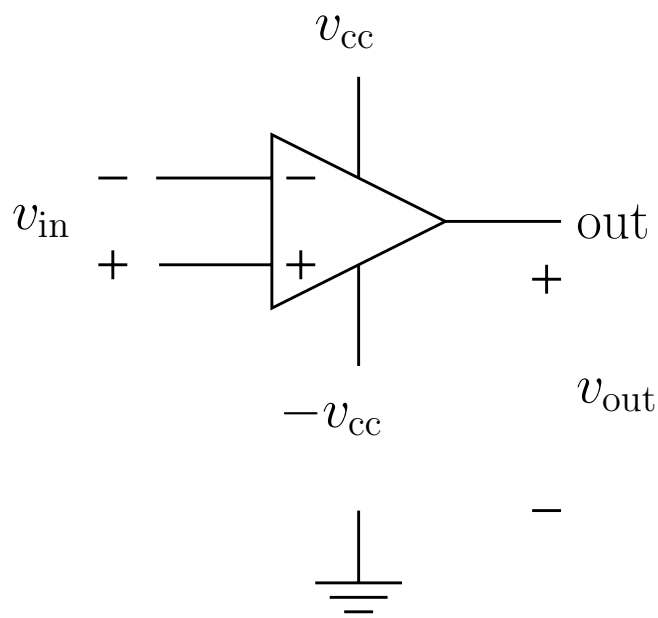


find v

The Operational Amplifier (op-amp)

the op-amp is the most important building block in analog circuits (used in the design of amplifiers, analog-to-digital converters, filters, ...)

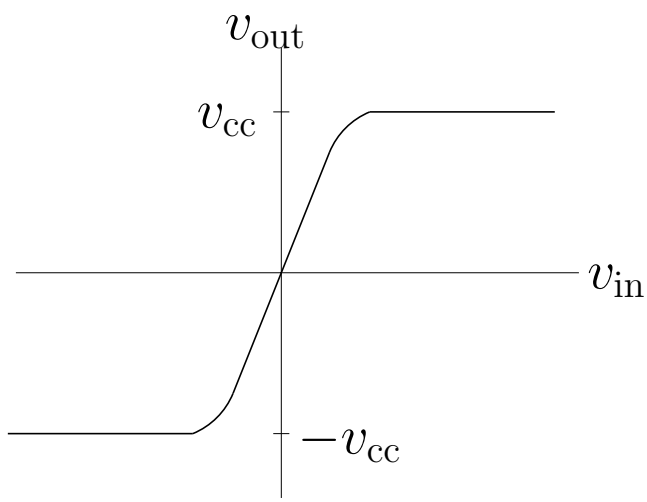
- the op-amp is physically a five-terminal device (not counting ground)



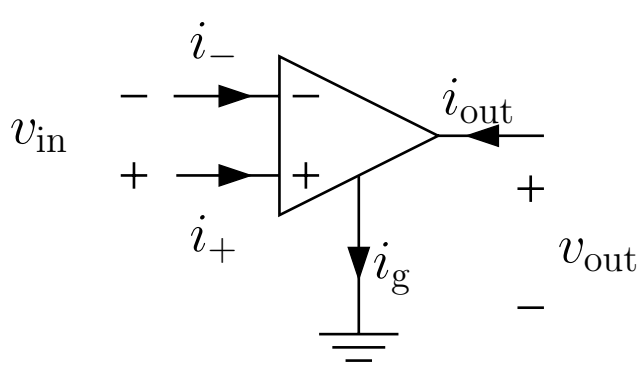
terminals v_{cc} and $-v_{\mathrm{cc}}$ are connected to power supplies ($e.g.$, $+12$ and -12)

The Operational Amplifier – contd.

- the op-amp v_{in} – v_{out} relation is nonlinear



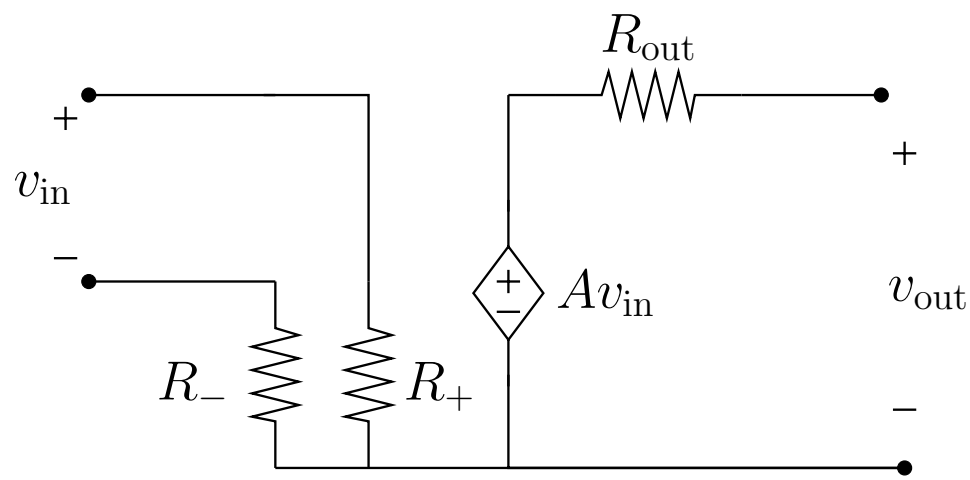
- in 101 we only consider the op-amp operation in the linear region and supress the $\pm v_{\text{cc}}$ terminals (connect them to the ground terminal)



The Operational Amplifier – contd.

- in the linear region, the op-amp can be modelled as a

linear voltage amplifier:



R_+ and R_- are typically very large (MΩs) and R_{out} is very small (100s of Ωs), so we can simplify the op-amp model by setting $R_+ = R_- = \infty$ and $R_{\text{out}} = 0$ to get the

VCVS model:

$$\begin{aligned} i_+ &= 0 \\ i_- &= 0 \\ v_{\text{out}} &= Av_{\text{in}} \end{aligned}$$

The Operational Amplifier – contd.

- we can simplify the model further by using the fact that the op-amp gain is typically very high ($> 10^6$), and so to operate in the linear region v_{in} must be very small and we get the

  ideal op-amp model:

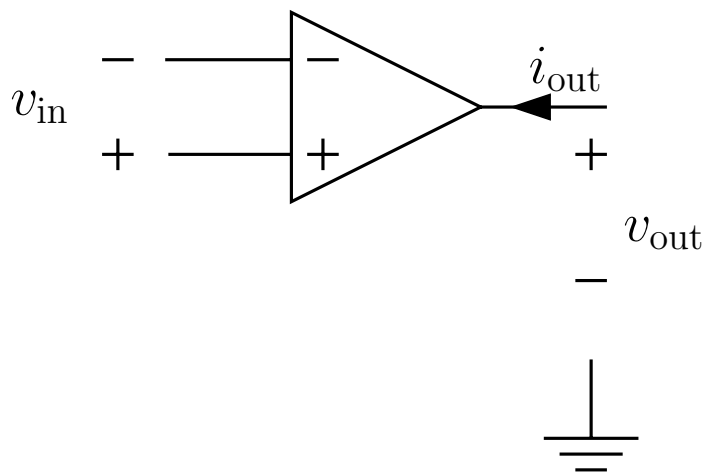
$$
\begin{aligned}
i_+ &= 0 \\
i_- &= 0 \\
v_+ &= v_-
\end{aligned}
$$

  here v_{out} and i_{out} are unconstrained (which seems very strange) and are determined by the rest of the circuit

- in 101 we will often assume the ideal op-amp model

Basic op-amp circuits

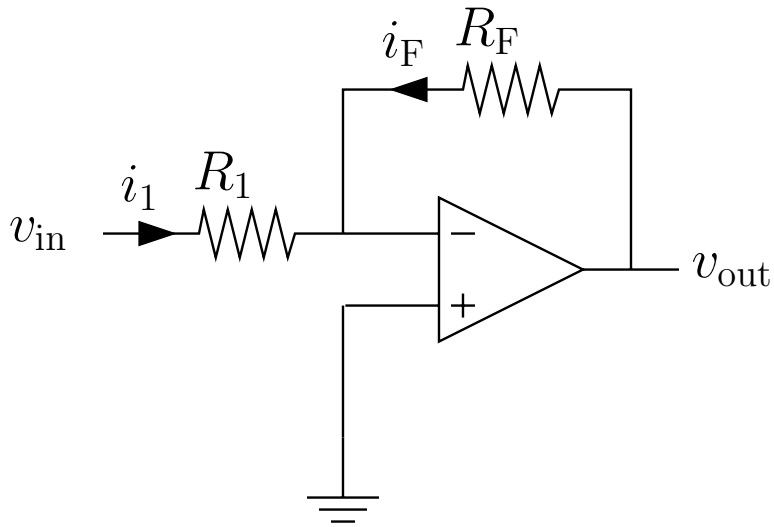
assuming that the op-amp operates in the linear region, we draw its symbol as a three terminal device



we should remember that i_{out} flows through the suppressed fourth terminal to ground (or more accurately to the power supply terminals) and **not** to the input terminals

basic op-amp circuits implement analog signal processing functions, $e.g.$, scaling, addition, weighted sum (of voltages or currents)

Inverting Amplifier



assuming the ideal op-amp model,

- $v_- = v_+ = 0$, and thus $i_1 = v_{in}/R_1$, and $i_F = v_{out}/R_F$
- since $i_- = 0$, we have (by KCL) $i_1 + i_F = 0$, thus

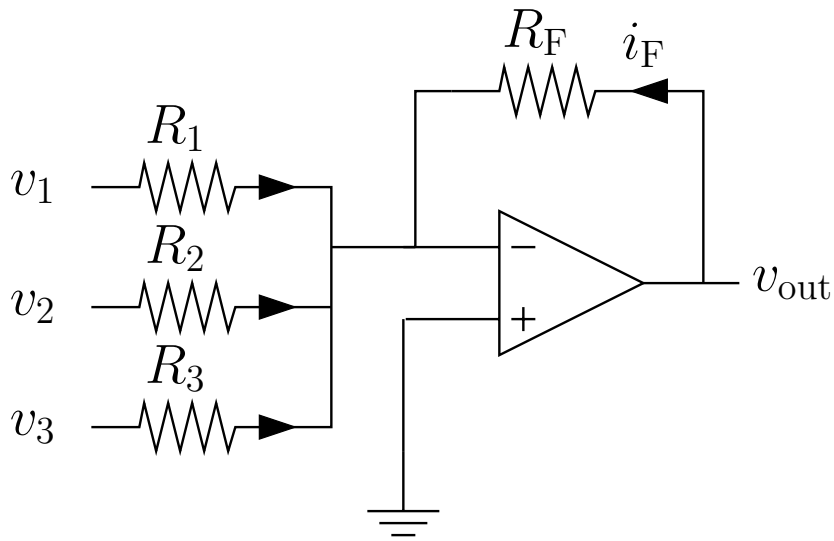
$$\frac{v_{in}}{R_1} + \frac{v_{out}}{R_F} = 0, \text{ or}$$

$$v_{out} = (-\frac{R_F}{R_1})v_{in}$$

and the circuit is a linear voltage amplifier with *gain* $-R_F/R_1$

check this assuming the VCVS model

Summing Amplifier



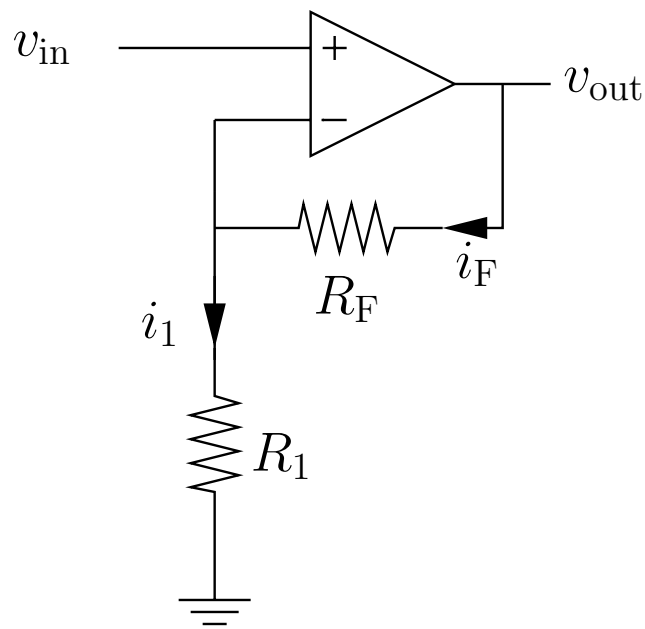
analysis:

- $v_- = 0$ (since voltage at the $+$ terminal is zero)
- $i_F = -(v_3/R_3 + v_2/R_2 + v_1/R_1)$ (since no current flows into $-$ terminal)
- $v_{out} = i_F R_F$ so we have:

$$v_{out} = -\frac{R_F}{R_1}v_1 - \frac{R_F}{R_2}v_2 - \frac{R_F}{R_3}v_3$$

- v_{out} is a weighted sum of the input voltages

Non-inverting Amplifier



analysis:

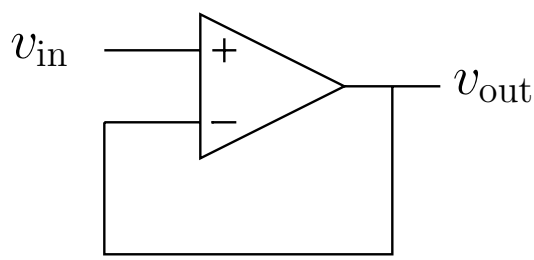
- $i_1 = i_{\rm F}$ and $v_- = v_+ = v_{\rm in}$
- also $i_1 = v_-/R_1$ and $i_{\rm F} = v_{\rm out}/(R_1 + R_{\rm F})$
- therefore,

$$\begin{aligned} \frac{v_-}{R_1} &= \frac{v_{\rm out}}{R_1 + R_{\rm F}} \\ v_{\rm out} &= \frac{R_1 + R_{\rm F}}{R_1} v_{\rm in} \\ v_{\rm out} &= (1 + \frac{R_{\rm F}}{R_1}) v_{\rm in} \end{aligned}$$

and the circuit is an amplifier with gain $(1 + R_{\rm F}/R_1)$, a positive number

Unity gain amplifier

an interesting special case (for $R_{\mathrm{F}} = 0$ and $R_1 = \infty$) is the unity gain amplifier circuit (also called voltage follower amplifier or analog buffer)



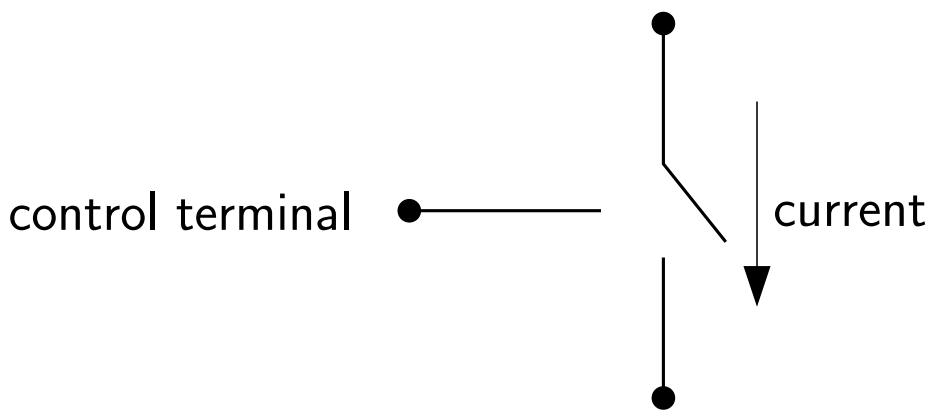
here $v_{\mathrm{out}} = v_{\mathrm{in}}$!

what is this circuit good for?

circuit used to supply a large current at constant voltage (to a load) from a voltage source that cannot supply enough current directly (or at constant voltage)

Transistors

the transistor is a three terminal device that operates as a *switch* between two terminals (more accurately as a dependent current source) controlled by the third (control) terminal's voltage or current



used in *all* analog and digital circuits

two main types:

- **bipolar junction transistor (BJT):** invented in 1948 at Bell Labs by Bardeen, Brattain, and Shockley (who later became a professor at Stanford) – they later received the Nobel prize in physics for their invention

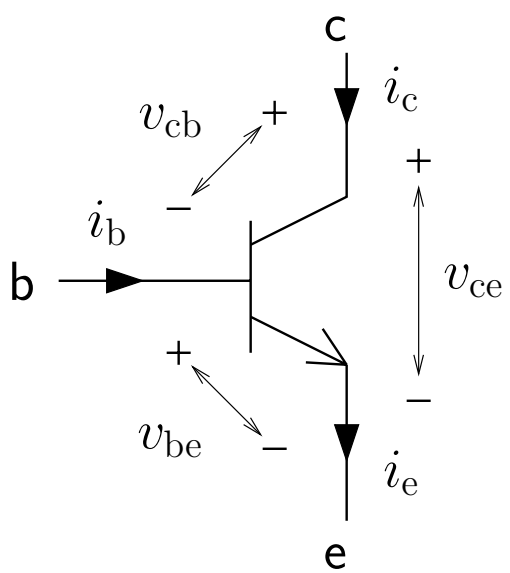
  today, BJTs are only used in very high power (or speed) analog integrated circuits ($e.g.$, power amplifiers for radio transmitters), and are rarely used in digital circuits

Transistors – contd.

- **metal-oxide-semiconductor (MOS) transistor:** invented earlier than the BJT but the technology needed to build it was developed much later (in early 1970s)
  - almost all digital circuits ($e.g.$, microprocessors, DRAMs, DSPs) and most analog circuits today use MOS transistors
  - in current MOS technology (with minimum feature size of 0.18μm) over 50 million transistors can be integrated on a 1cm^2 integrated circuit (IC, chip)
  - The number of transistors per chip has been doubling every 2 years and will reach 1 billion by the year 2010!! (this is known as Moore's law after Gordon Moore, one of Intel's founders)

Bipolar junction transistor (BJT)

terminals: collector, base, emitter (npn is shown)

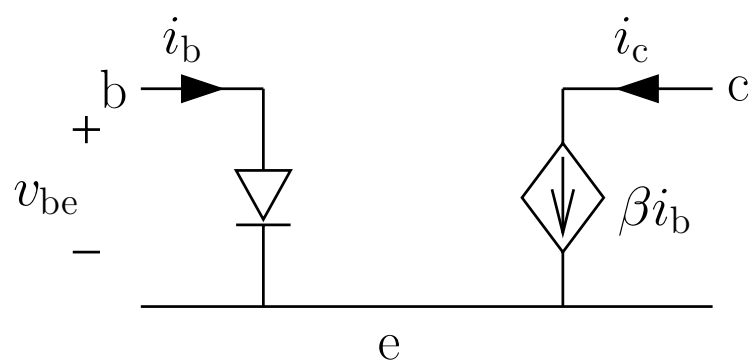


KVL says: $v_{ce} = v_{be} + v_{cb}$
(so only two independent voltages)

KCL says: $i_b + i_c - i_e = 0$
(so only two independent currents)

BJT model

- the base to collector circuit is a diode
- the base to emitter circuit is also a diode
- in normal operation (the only case we consider here) the base to collector diode is off (more specifically $v_{\mathrm{bc}} \leq 0$), and the BJT behaves as a CCCS



- assuming ideal diode model we get two regions of operation:
  - $v_{\mathrm{be}} < v_{\mathrm{th}}$: $i_{\mathrm{b}} = i_{\mathrm{c}} = 0$ and the transistor is off
  - $v_{\mathrm{be}} = v_{\mathrm{th}}$: $i_{\mathrm{c}} = \beta i_{\mathrm{b}}$ and the transistor is on (a CCCS), where β depends on the physical characteristics of the device (typical value of $\beta \approx 100$ or so)

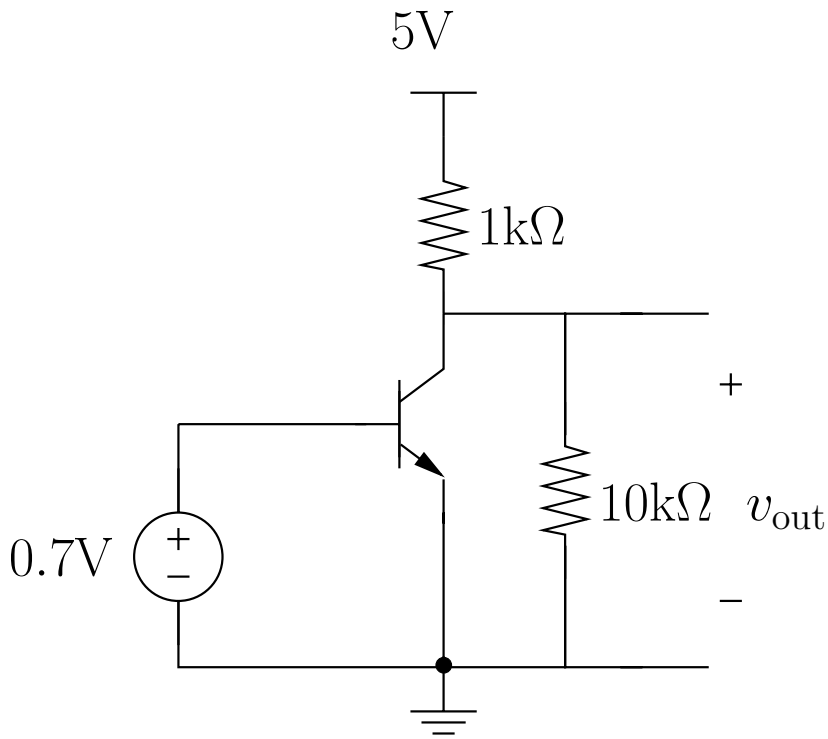
BJT model – contd.

- if we assume the exponential diode model we get the two equations:

$$\begin{aligned} i_{\mathrm{b}} &= i_0(e^{\frac{v_{\mathrm{be}}}{v_{\mathrm{T}}}} - 1), \text{ and} \\ i_{\mathrm{c}} &= \beta i_{\mathrm{b}} \end{aligned}$$

- the model provides 2 equations in the 4 unknown voltages and currents (the rest are provided by the circuit)
- model derived from device physics (as in EE 111/112)

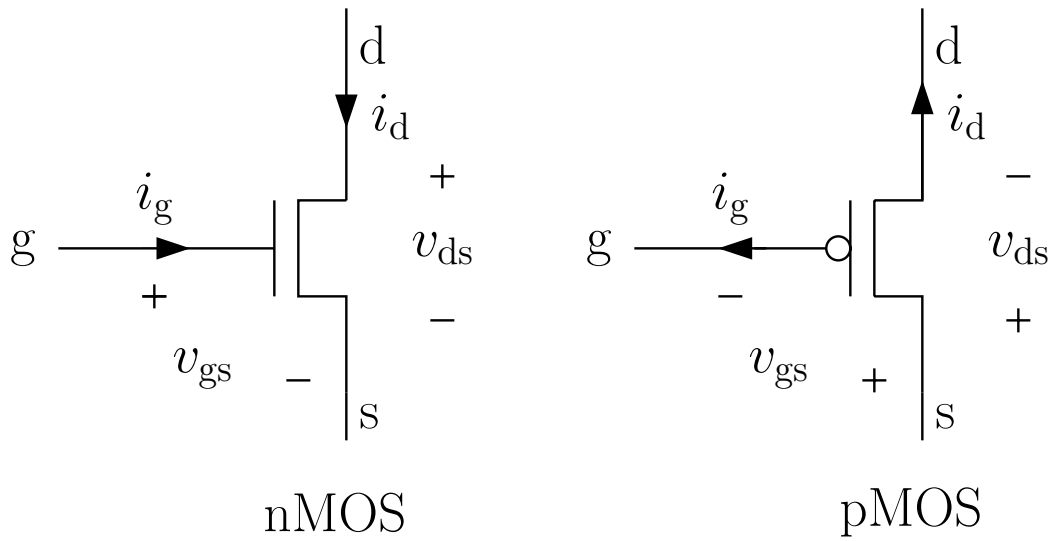
BJT circuit example



find v_{out}, assuming the exponential diode model with $i_0 = 10^{-14}$A, $\beta = 100$

MOS transistor

two (complementary) types

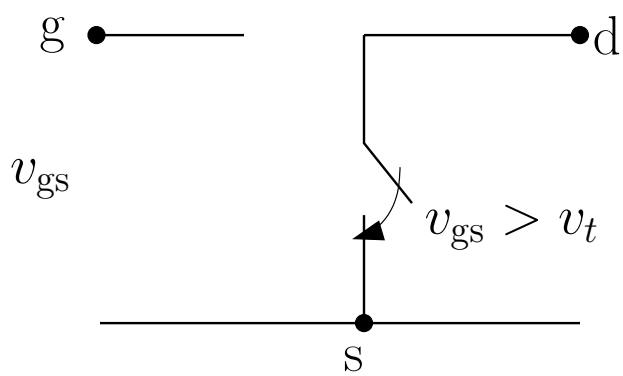


- the drain and source terminals are physically indistiguishable – for nMOS the drain is the terminal of higher potential (when the device is in a circuit), and is the terminal of lower potential for pMOS
- KCL and KVL again give us 2 equations in the 6 voltage and current unknowns (this is why we only show 4 variables)
- MOS transistors are used to build digital circuits, $e.g.$, logic gates (NAND, NOR, inverter,. . .) and memory circuits (latches, SRAM, DRAM), and analog circuits, $e.g.$, op-amps

MOS transistor switch model

to analyze the function of a digital circuit, we use a simple **switch model**, given by:

$i_g = 0$, and



- for $v_{\mathrm{gs}} \leq v_{\mathrm{t}}$ (threshold voltage), the transistor (nMOS or pMOS) is *off*
- for $v_{\mathrm{gs}} > v_{\mathrm{t}}$, the transistor is *on*
- $v_{\mathrm{t}} \approx 0.7\mathrm{V}$ (scales down as technology advances)

First order static model

to analyze analog circuits and signal waveforms in digital circuits we need more complex (accurate) models

the simplest such model is the **first order static model** given by:

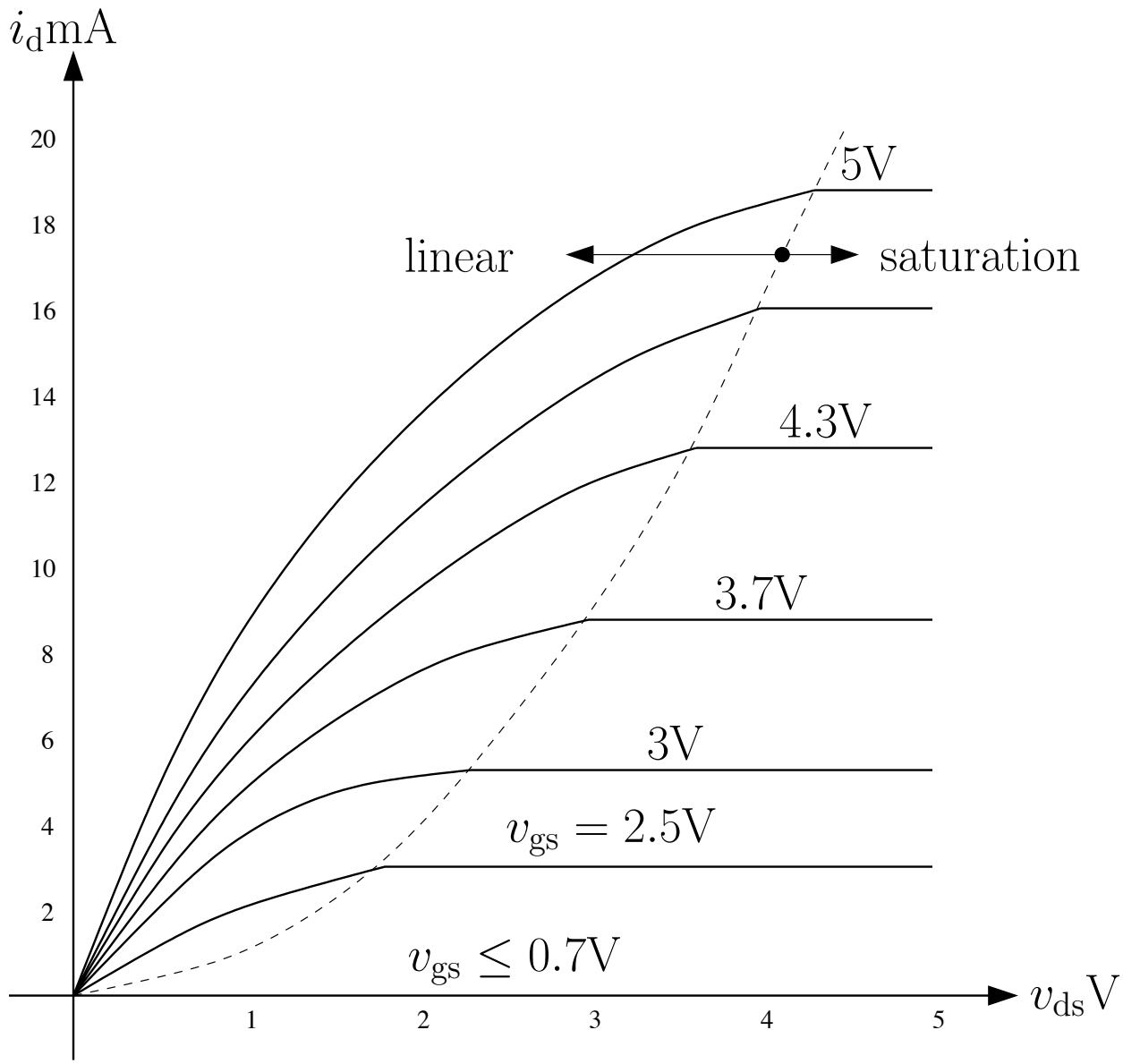
$i_{\mathrm{g}} = 0,$

$$i_{\mathrm{d}} = \begin{cases} 0, & v_{\mathrm{gs}} \leq v_{\mathrm{t}} \quad \text{cutoff} \\ \frac{k}{2} v_{\mathrm{ds}}(2v_{\mathrm{gs}} - 2v_{\mathrm{t}} - v_{\mathrm{ds}}), & 0 \leq v_{\mathrm{ds}} \leq v_{\mathrm{gs}} - v_{\mathrm{t}} \quad \text{'linear'} \\ \frac{k}{2}(v_{\mathrm{gs}} - v_{\mathrm{t}})^2, & 0 < v_{\mathrm{gs}} - v_{\mathrm{t}} < v_{\mathrm{ds}} \quad \text{saturation} \end{cases}$$

- k (transconductance parameter) can vary widely with the size and technology parameters of the transistor
- model derived from device physics
- in saturation region MOS transistor acts as a nonlinear voltage controlled current source VCCS
- in linear region, for very small v_{ds} and fixed v_{gs}, the drain to source circuit can be modelled as a linear resistor with $R_{\mathrm{ds}} = \frac{1}{k(v_{\mathrm{gs}} - v_{\mathrm{t}})}$
- model derived from device physics (discussed in EE 112)

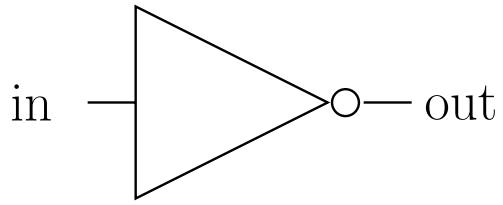
First order model example

let $v_{\mathrm{t}} = 0.7\mathrm{V}$ and $k = 2\mathrm{mA/V}^2$, the following is a plot of the MOS transistor "I – V characteristics" assuming the first order model



The CMOS Inverter

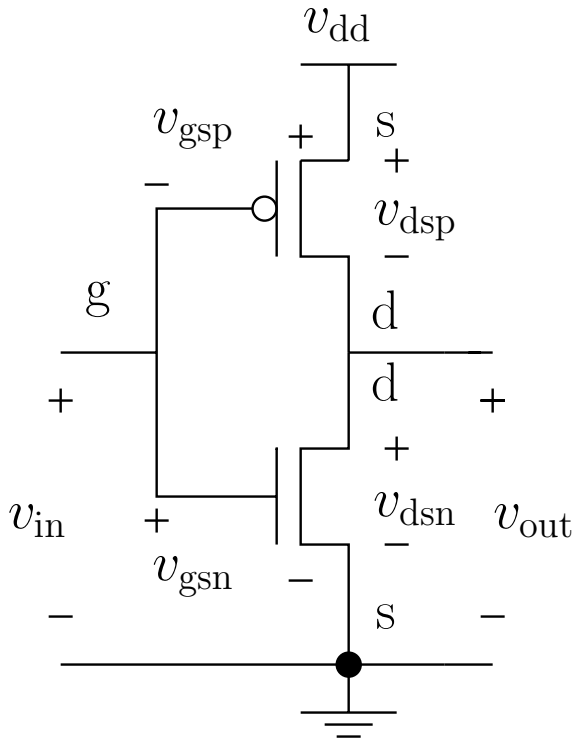
the inverter is the simplest *logic gate*



with the *truth table*

in	out
1	0
0	1

the CMOS inverter is implemented using two transistors

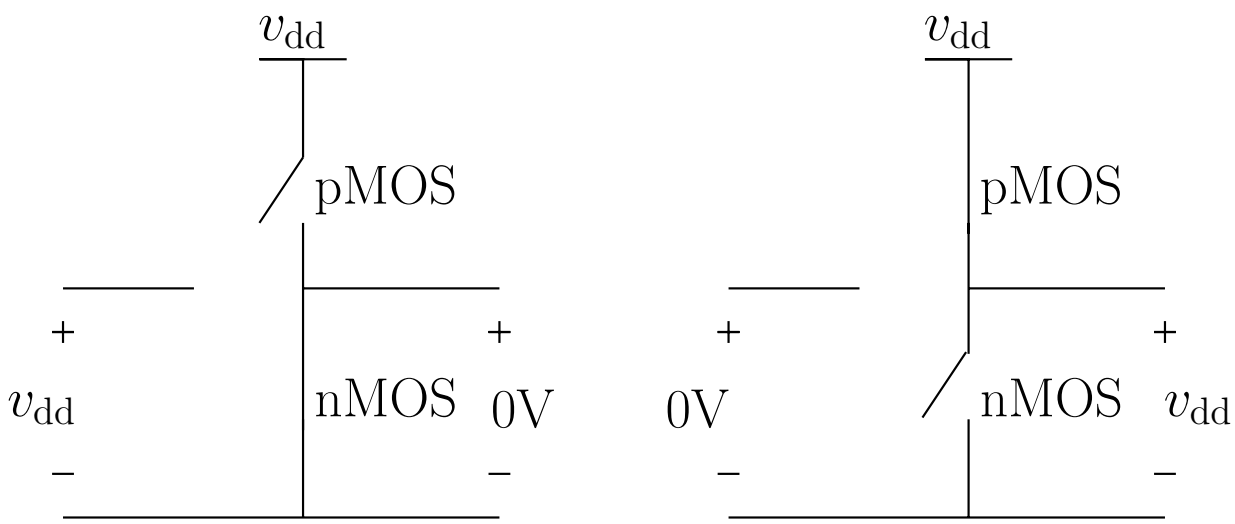


v_{in} ranges from $0\mathrm{V}$ to v_{dd} (typical value $= 3.3\mathrm{V}$, scales down with technology)

Analysis using the MOS switch model

v_{in} takes on one of two values: $0\mathrm{V}$ (logic level 0) or v_{dd} (logic level 1)

assuming the MOS transistor switch model:



- if $v_{\mathrm{in}} = v_{\mathrm{dd}}$ the nMOS device is on, the pMOS device is off, and $v_{\mathrm{out}} = 0\mathrm{V}$
- if $v_{\mathrm{in}} = 0\mathrm{V}$ the nMOS device is off, the pMOS is on, and $v_{\mathrm{out}} = v_{\mathrm{dd}}$

Analysis – contd.

note that:

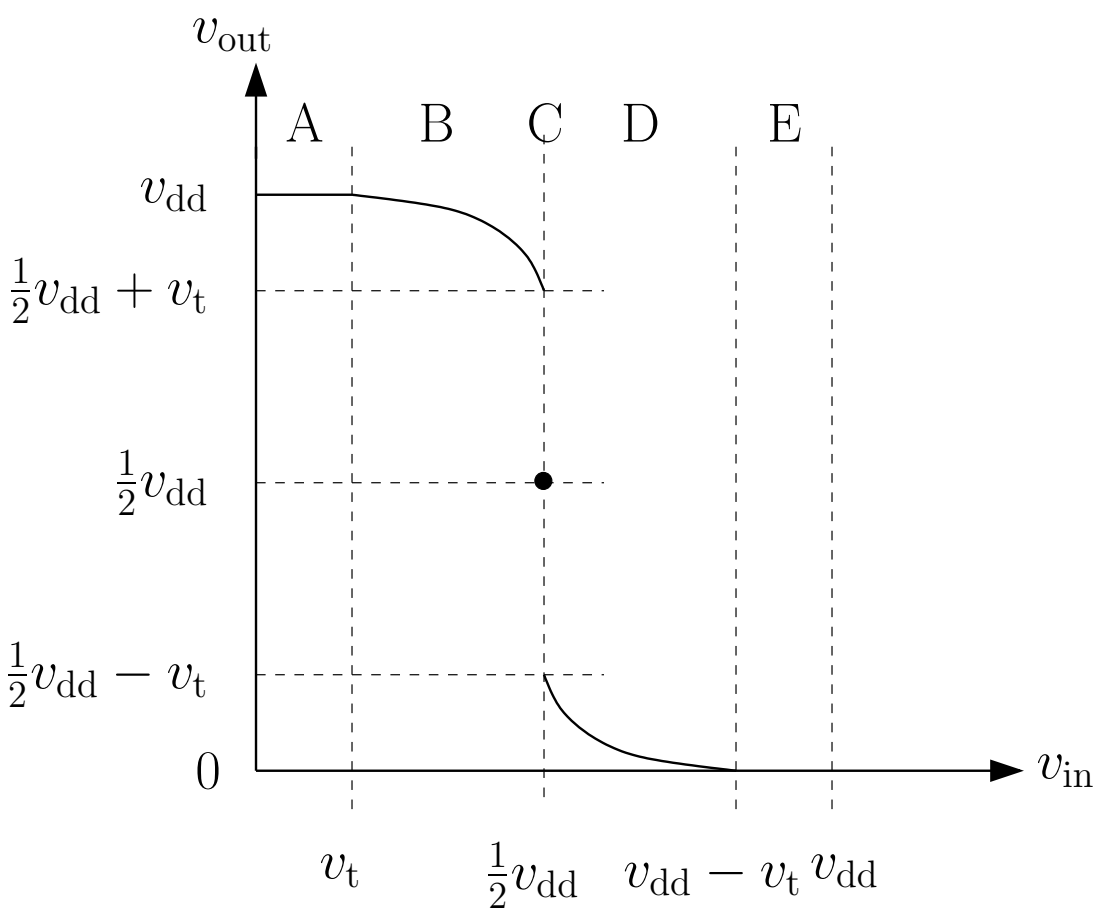
- assuming the MOS switch model, no current flows from v_{dd} to ground, also $i_g = 0$, so the inverter does not dissipate any power !!
- in the real circuit current flows momentarily when the inverter switches and almost no current flows otherwise – inverter dissipates almost no power when its input is not switching
- this very low *static* power consumption is the key advantage of CMOS logic circuits over other types of logic circuits

Analysis using the first order static model

applying KCL and KVL to the inverter circuit we get:

$i_{\mathrm{dn}} = i_{\mathrm{dp}}$,
$v_{\mathrm{gsn}} + v_{\mathrm{gsp}} = v_{\mathrm{dd}}$, and
$v_{\mathrm{dsn}} + v_{\mathrm{dsp}} = v_{\mathrm{dd}}$

using these KCL and KVL equations and the first order model with $v_{\mathrm{dd}} > 2v_{\mathrm{t}}$, we get five regions of operation (we assume here that k and v_{t} are the same for the two transistors, which is not a good assumption, in practice)



Analysis – contd.

region A: $0 \leq v_{\mathrm{in}} < v_{\mathrm{t}}$, the nMOS is in the cutoff region and the pMOS is in the linear region, and $v_{\mathrm{out}} = v_{\mathrm{dd}}$

region B: $v_{\mathrm{t}} \leq v_{\mathrm{in}} < \frac{v_{\mathrm{dd}}}{2}$, the pMOS is in the linear region and the nMOS is in saturation, and
$v_{\mathrm{out}} = (v_{\mathrm{in}} + v_{\mathrm{t}}) + \sqrt{v_{\mathrm{dd}}(v_{\mathrm{dd}} - 2v_{\mathrm{t}} - 2v_{\mathrm{in}}) + 4v_{\mathrm{in}}v_{\mathrm{t}}}$

region C: $v_{\mathrm{in}} = \frac{v_{\mathrm{dd}}}{2}$, both the nMOS and pMOS are in saturation, and $v_{\mathrm{out}} = \frac{v_{\mathrm{dd}}}{2}$

region D: $\frac{v_{\mathrm{dd}}}{2} < v_{\mathrm{in}} \leq v_{\mathrm{dd}} - v_{\mathrm{t}}$, same as region B but with pMOS and nMOS exchanged, and
$v_{\mathrm{out}} = (v_{\mathrm{in}} - v_{\mathrm{t}}) - \sqrt{v_{\mathrm{dd}}(2v_{\mathrm{in}} + 2v_{\mathrm{t}} - v_{\mathrm{dd}}) - 4v_{\mathrm{in}}v_{\mathrm{t}}}$

region E: $v_{\mathrm{dd}} - v_{\mathrm{t}} < v_{\mathrm{in}} \leq v_{\mathrm{dd}}$, same as region A but with pMOS and nMOS exchanged, and $v_{\mathrm{out}} = 0$

Analysis Details

Region A: Here $0 \leq v_{\rm in} \leq v_{\rm t}$. By inspection, the nMOS is off and the pMOS is on. Let's assume that the pMOS is in the linear region. Since (by KCL) $i_{\rm dn} = i_{\rm dp} = 0$,

$$0 = \frac{k}{2} v_{\rm dsp}(2v_{\rm gsp} - 2v_{\rm t} - v_{\rm dsp}).$$

So either

$$v_{\rm dsp} = 2(v_{\rm gsp} - v_{\rm t}) \text{ or } v_{\rm dsp} = 0.$$

The first solution violates our assumption that the pMOS is in the linear region (check that). The second solution is consistent with our assumption. So $v_{\rm out} = v_{\rm dd}$.

Region B: Here $v_{\rm t} \leq v_{\rm in} < \frac{v_{\rm dd}}{2}$. In this case both transistors are on. We assume that the nMOS is in saturation and the pMOS is still in the linear region. Now since $i_{\rm dn} = i_{\rm dp}$,

$$(v_{\rm gsn} - v_{\rm t})^2 = v_{\rm dsp}(2v_{\rm gsp} - 2v_{\rm t} - v_{\rm dsp}).$$

Since we want $v_{\rm out}$ as a function of $v_{\rm in}$ we use the fact that $v_{\rm gsn} = v_{\rm in}$, and the KVL equation $v_{\rm gsn} + v_{\rm gsp} = v_{\rm dd}$ to get a quadratic equation

$$v_{\rm dsp}^2 - 2v_{\rm dsp}(v_{\rm dd} - v_{\rm in} - v_{\rm t}) + (v_{\rm in} - v_{\rm t})^2 = 0$$

with two roots

$$v_{\rm dsp} = (v_{\rm dd} - v_{\rm in} - v_{\rm t}) \pm \sqrt{v_{\rm dd}(v_{\rm dd} - 2v_{\rm t} - 2v_{\rm in}) + 4v_{\rm in}v_{\rm t}}.$$

First check that the discriminant (term under the square root) is nonnegative for the given range of $v_{\rm in}$. Now by the assumption of the pMOS being in the linear region, it must be that

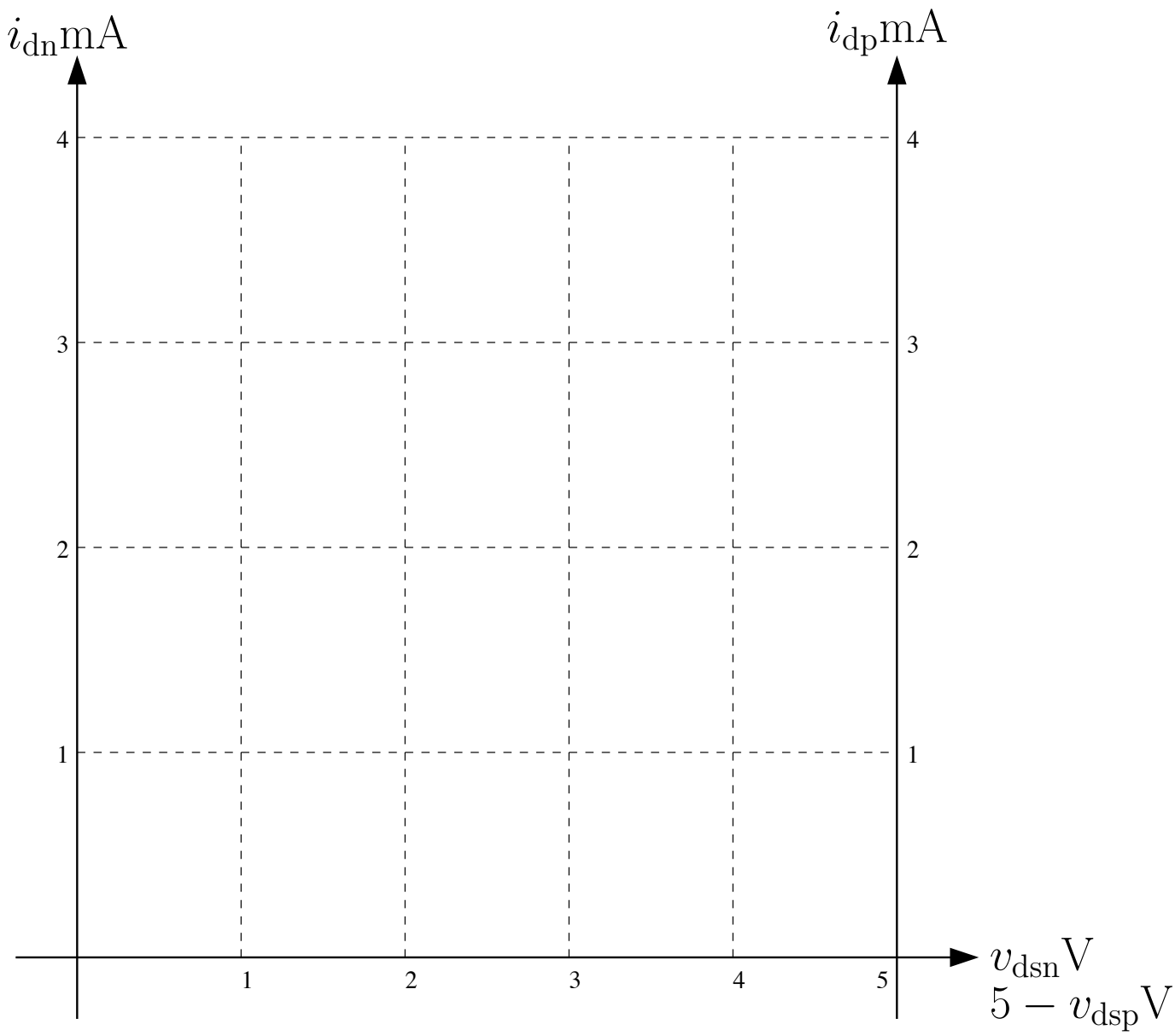
$$\begin{aligned} v_{\rm gsp} - v_{\rm t} &> v_{\rm dsp}, \text{ thus} \\ v_{\rm dd} - v_{\rm in} - v_{\rm t} &> v_{\rm dsp}, \end{aligned}$$

which precludes the root with the + sign. Now using the KVL equation $v_{\rm dsp} = v_{\rm dd} - v_{\rm out}$ we find $v_{\rm out}$.

Region C: Here $v_{\rm in} = \frac{v_{\rm dd}}{2}$. We assume that both transistors are in saturation. This is consistent with $i_{\rm dn} = i_{\rm dp}$. So, what is $v_{\rm out}$ in this case. Any $v_{\rm out}$ that keeps the two transistors in saturation is feasible, *i.e.*, $\frac{v_{\rm dd}}{2} - v_{\rm t} < v_{\rm out} < \frac{v_{\rm dd}}{2} + v_{\rm t}$. By symmetry (the two devices have same k and $v_{\rm t}$), however, we expect that $v_{\rm out} = \frac{v_{\rm dd}}{2}$.

Finding $v_{\mathrm{in}} - v_{\mathrm{out}}$ graphically

assume $v_{\mathrm{dd}} = 5\mathrm{V}$, $v_{\mathrm{t}} = 0.7\mathrm{V}$, and $k = 2\mathrm{mA/V}^2$, find v_{out} for $v_{\mathrm{in}} = 2.7\mathrm{V}$



Lecture Notes 5
Introduction to Circuit Theory

- KCL via node incidence matrix
- KVL via node incidence matrix
- branch relations
- solving the equations

What is circuit theory?

we know that circuit analysis is based *only* on:

- KVL,
- KCL, and
- the device models relations

circuit theory uses an organized (systematic) formulation of KCL, KVL, and the device models relations to

- prove fundamental circuit results, $e.g.$, power conservation
- derive important circuit analysis techniques, $e.g.$, node-voltage method, superposition, and Norton and Thevenin equivalents
- develop methods for solving the equations using computers, $i.e.$, for developing circuit simulators

KCL

we first study an organized way to express KCL

consider a circuit with

- n nodes, labelled $\boxed{1}, \boxed{2}, \ldots, \boxed{\text{n}}$, with $\boxed{\text{n}}$ the ground or common node
- b branches, labelled $1, 2, \ldots, b$

we assume that

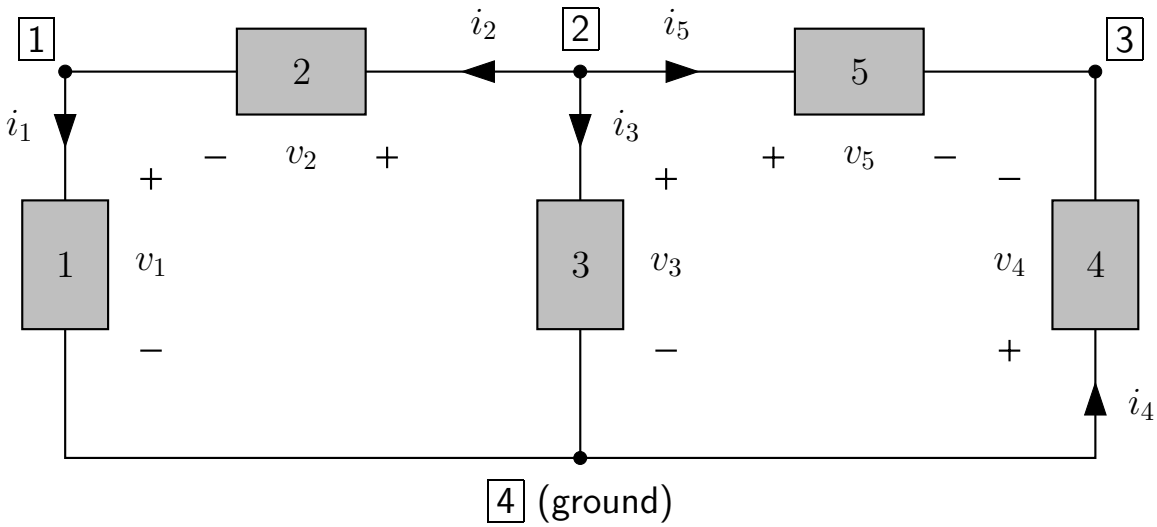
- the circuit is *connected*, $i.e.$, there is a path of branches from any node to any other node
- the branches represent two-terminal elements (for now)

for each branch we assign *associated* current and voltage reference directions and define

- $i_k \triangleq$ current through branch k
- $v_k \triangleq$ voltage across branch k

KCL – contd.

simple example (with 4 nodes and 5 branches):



let's write KCL for each node:

$$
\begin{array}{lrcrcrcrcrcl}
\text{node } \boxed{1}: & i_1 & - & i_2 & & & & & & & = & 0 \\
\text{node } \boxed{2}: & & & i_2 & + & i_3 & & & + & i_5 & = & 0 \\
\text{node } \boxed{3}: & & & & & & - & i_4 & - & i_5 & = & 0 \\
\text{node } \boxed{4}: & - & i_1 & & & - & i_3 & + & i_4 & & = & 0
\end{array}
$$

kth row is total current leaving node $\boxed{\text{k}}$ ($= 0$ by KCL)

in matrix notation:

$$
\begin{bmatrix} 1 & -1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 \\ 0 & 0 & 0 & -1 & -1 \\ -1 & 0 & -1 & 1 & 0 \end{bmatrix}
\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \end{bmatrix}
=
\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}
$$

KCL – contd.

or, very compactly: $\tilde{A}i = 0$, where

$$\tilde{A} \triangleq \begin{bmatrix} 1 & -1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 \\ 0 & 0 & 0 & -1 & -1 \\ -1 & 0 & -1 & 1 & 0 \end{bmatrix}, \quad i \triangleq \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \end{bmatrix}$$

(and 0 on the right-hand side means the zero vector $\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$)

- i is called the *branch current vector*
  (i has b components, $i.e.$, $i \in \mathbf{R}^b$)
- $\tilde{A}$ is called the *node incidence matrix* of the circuit
  ($\tilde{A}$ has n rows and b columns, $i.e.$, $\tilde{A} \in \mathbf{R}^{n \times b}$)

in general the node incidence matrix is given by:

$$\tilde{A}_{jk} \triangleq \begin{cases} +1 & \text{if branch } k \text{ current direction leaves node } j \\ -1 & \text{if branch } k \text{ current direction enters node } j \\ 0 & \text{if branch } k \text{ doesn't touch node } j \end{cases}$$

- $\tilde{A}$ has n rows; each corresponds to a *node*
- $\tilde{A}$ has b columns; each corresponds to a *branch*
- each column has exactly one $+1$ and exactly one -1 entry; the rest are zeros

KCL – contd.

KCL for all nodes can be expressed as the matrix equation $\tilde{A}i = 0$ (which contains n equations in b variables)

are these equations linearly independent?
(or conversely can any of them be written as a linear combination of the others?)

it turns out that the answer to the question is **no**, they are not linearly independent

adding up the equations, we always get the (not so useful) equation:

$$(i_1 - i_1) + (i_2 - i_2) + \cdots + (i_b - i_b) = 0$$

(see our example)

thus, $e.g.$, the last equation is equal to minus the sum of the others

interpretation: if KCL holds at nodes $\boxed{1}$, . . . , $\boxed{\text{n-1}}$, then it automatically holds at node $\boxed{\text{n}}$

fact: if you throw away the KCL equation for node $\boxed{\text{n}}$ (or any other node), the rest are independent (as long as the circuit is connected)

KCL – contd.

let A denote $\tilde{A}$ with the bottom row removed
(A is called the *reduced incidence matrix* of the circuit)

the *independent* KCL equations can then be written as:

$$Ai = 0$$

the number of independent KCL equations is $n - 1$ (and the number of unknowns is $b > n - 1$)

for our example, the independent KCL equations are:

$$\begin{bmatrix} 1 & -1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 \\ 0 & 0 & 0 & -1 & -1 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}$$

(the rows are KCL at the nodes *except* ground)

KVL

how can we express KVL in an organized way?

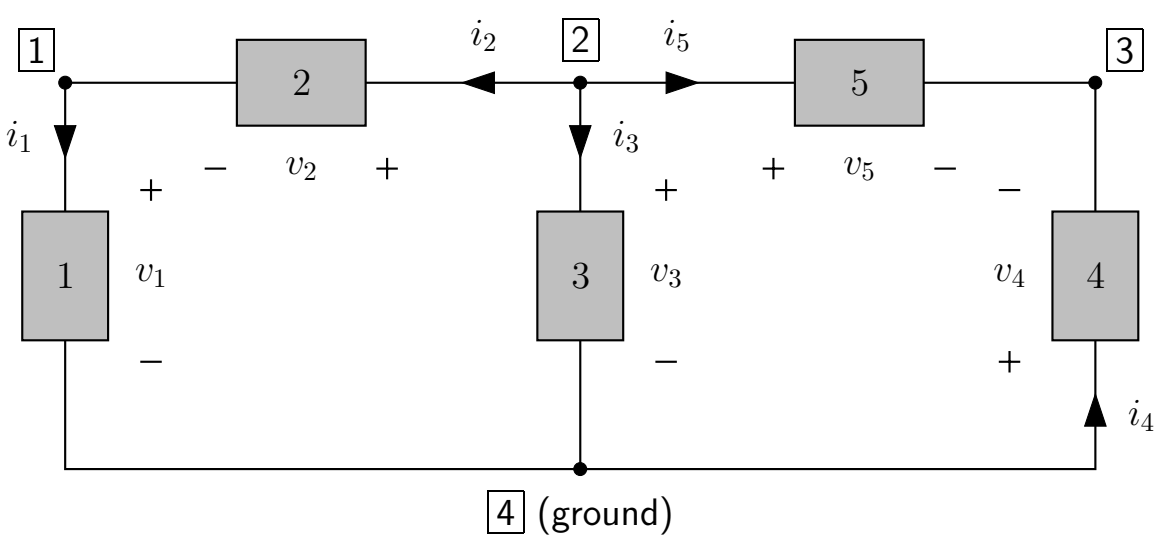
could write KVL for each loop in the circuit, but a more convenient way is based on the *node potentials* or *node voltages* $e_1, \ldots, e_{n-1}$, where

$$e_k \triangleq \text{voltage from node } \boxed{\text{k}} \text{ to ground node } \boxed{\text{n}}$$

(we don't need e_n; it would automatically be zero)

recall one way to express KVL is: the voltage across a branch is the difference between the node voltage at the $+$ end and the node voltage at the $-$ end

let's look at our example again:



KVL – contd.

we can express KVL as:

$$
\begin{array}{lrcrcrcrcr}
\text{branch } 1\text{:} & v_1 & = & & e_1 & & & & & (-\ e_4) \\
\text{branch } 2\text{:} & v_2 & = & - & e_1 & + & e_2 & & & \\
\text{branch } 3\text{:} & v_3 & = & & & & e_2 & & & (-\ e_4) \\
\text{branch } 4\text{:} & v_4 & = & & & & & - & e_3 & (+\ e_4) \\
\text{branch } 5\text{:} & v_5 & = & & & & e_2 & - & e_3 &
\end{array}
$$

(we don't need the last column since $e_4 = 0$)

or, in matrix notation,

$$
\begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \\ v_5 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ -1 & 1 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & -1 \\ 0 & 1 & -1 \end{bmatrix} \begin{bmatrix} e_1 \\ e_2 \\ e_3 \end{bmatrix}
$$

KVL – contd.

looking carefully we see that this matrix is the *transpose* of the reduced incidence matrix A ($i.e.$, the ij entry of A^T is A_{ji}: rows of A become columns of A^T and vice versa)

so KVL can be stated very compactly as:

$$v = A^T e$$

where

- v is the *branch voltage vector* and e is the *node voltage vector*:

$$v = \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \\ v_5 \end{bmatrix}, \quad e = \begin{bmatrix} e_1 \\ e_2 \\ e_3 \end{bmatrix}$$

- A is the reduced incidence matrix

it turns out the b equations in KVL, expressed as $v = A^T e$, are independent

Application: Power conservation

as an application we derive a general power conservation law

in a circuit some elements dissipate power and others supply it, and as we know

total power supplied = total power absorbed
(independent of what the branches are!)

let's derive this from KCL and KVL
(since it cannot depend on branch relations)

power dissipated in branch k is $p_k = v_k i_k$

power conservation can be expressed as

$$p_{\text{total}} = p_1 + \cdots + p_b = 0$$

in matrix form, $p_{\text{total}} = v^T i$

using $v = A^T e$,

$$p_{\text{total}} = v^T i = (A^T e)^T i = e^T A^{T^T} i = e^T A i = 0,$$

since from KCL $Ai = 0$

Summary of KCL, KVL formulation

connected circuit with n nodes, b branches, and reduced node incidence matrix A

circuit variables:

- v is the branch voltage vector (b components)
- i is the branch current vector (b components)
- e is the node potential vector ($n-1$ components)

total number of variables (unknowns): $2b+n-1$

KCL is: $Ai=0$ ($n-1$ equations)

KVL is: $v=A^Te$ (b equations)

total number of KCL, KVL equations: $b+n-1$

the remaining equations necessary to determine the variables come from the branch relations, $i.e.$, the device models

Branch relations

for each branch we have *one* equation that gives the $v - i$ characteristic or relation:

$$f_k(v_k, i_k) = 0, \quad k = 1, 2, \ldots, b$$

some examples:

branch	$v - i$ relation	element
3	$v_3 - 10i_3 = 0$	10Ω resistor
17	$v_{17} - 13 = 0$	$13\mathrm{V}$ voltage source
12	$i_{12} + 7 = 0$	$-7\mathrm{A}$ current source
2	$i_2 - i_0(e^{v_2/v_t} - 1) = 0$	diode

total number of branch equations: b

Variables and equations of circuit theory

variables of circuit theory:

- branch voltages: v
- branch currents: i
- node voltages: e

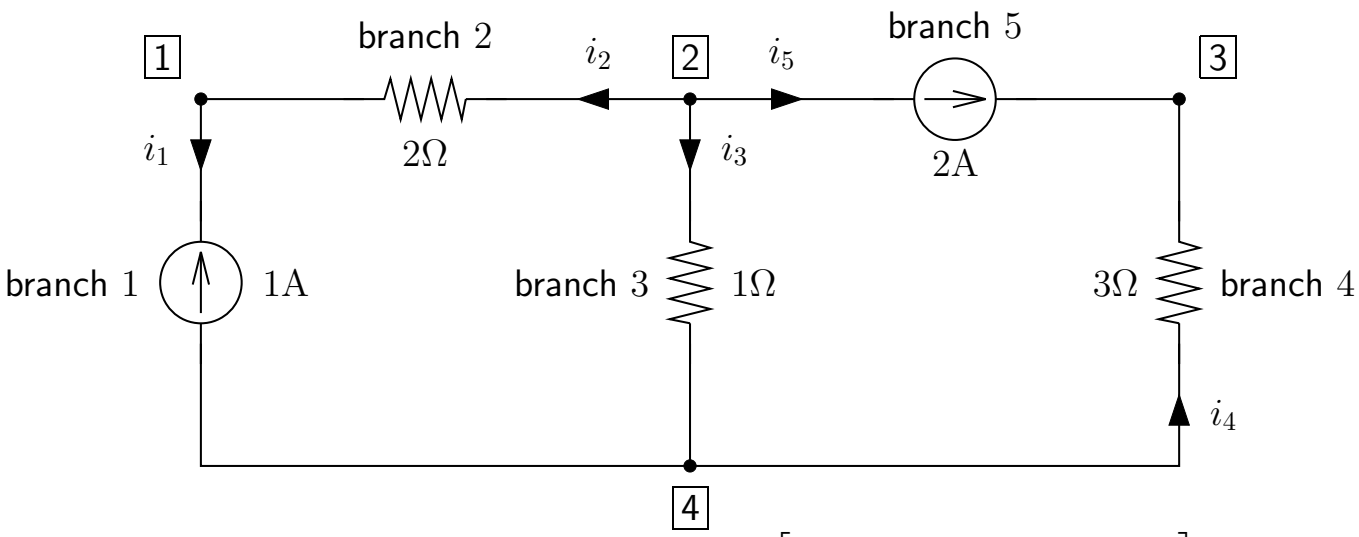
total number of variables: $2b + n - 1$

equations of circuit theory:

- KCL: $Ai = 0$
- KVL: $v = A^T e$
- branch relations: $f_k(v_k, i_k) = 0$, $k = 1, 2, \ldots, b$

total number of equations: $2b + n - 1$

Example



reduced incidence matrix is $A = \begin{bmatrix} 1 & -1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 \\ 0 & 0 & 0 & -1 & -1 \end{bmatrix}$

circuit equations are:

- KCL: $Ai = 0$ (3 equations)
- KVL: $v = A^T e$ (5 equations)
- branch relations: (5 equations total)

$$i_1 + 1 = 0, \quad v_2 - 2i_2 = 0, \quad v_3 - i_3 = 0,$$

$$v_4 - 3i_4 = 0, \quad i_5 - 2 = 0$$

all together: 13 equations in the 13 variables

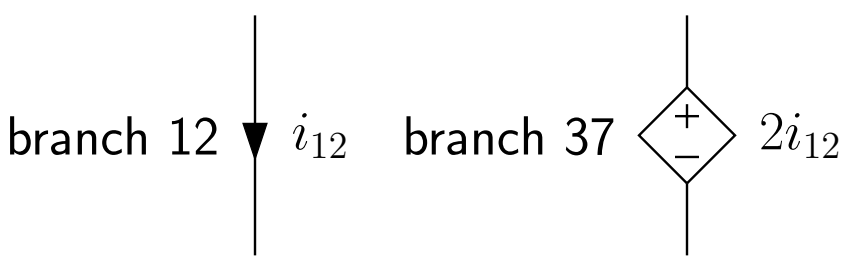
$$v_1, \ldots, v_5, \quad i_1, \ldots, i_5, \quad e_1, e_2, e_3$$

which can be solved (by hand or computer) ...

Multiterminal elements

we can use our formulation as long as we can represent any multi-terminal element using a number of branches and end up with b equations relating the b branch currents $i_1, \ldots, i_b$ to the b branch voltages $v_1, \ldots, v_b$

suppose, for example, we have a CCVS with sense branch 12, source branch 37, transresistance 2Ω, we can represent it using two branches:



with branch relations:

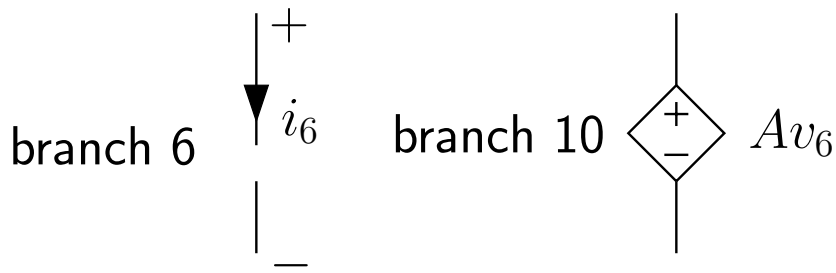
$$v_{12} = 0, \quad v_{37} - 2i_{12} = 0$$

Note: branch 12 does need to be a short circuit (it can have a two-terminal element with some relation)

OK: *two* equations relating the two branch currents i_{12}, i_{37} and the two branch voltages v_{12}, v_{37}

Multiterminal elements – contd.

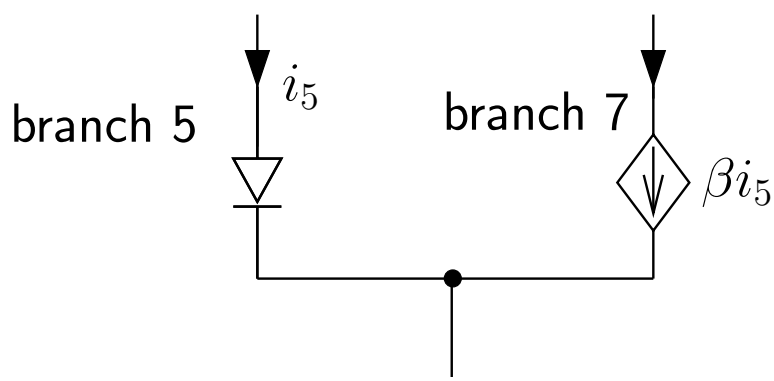
for an op-amp, assuming VCVS model, we can represent it using two branches:



with branch relations:

$$i_6 = 0, \quad v_{10} - Av_6 = 0$$

for a bipolar transistor, we can again represent the model using two branches:



with branch relations:

$$i_5 - i_0(e^{\frac{v_5}{v_T}} - 1) = 0, \quad i_7 - \beta i_5 = 0$$

Solving the circuit equations

- everything you can deduce from a circuit comes from the KCL and KVL equations and the branch relations
- circuit equations can have zero, one, or any number of solutions (zero solutions $\Rightarrow$ bad circuit model!)
- computers can solve these equations directly
- for hand solution, people try to simplify by eliminating variables and equations
- for circuit with ideal sources and linear device models, *e.g.*, resistors, dependent sources, and op-amps, solution can be found by matrix inversion (as we shall discuss in the next lecture notes)

Lecture Notes 6
Circuits with linear elements and sources

- equations for circuits with linear elements and sources
- node voltage analysis
- superposition principle and applications
- Thevenin and Norton equivalents
  - maximum power transfer
  - load line analysis

Equations for circuits with linear elements and sources

we now study circuits with only,

- linear elements, $e.g.$, resistors, linear dependent sources, op-amps, and
- independent voltage and current sources

for such circuits branch relations look like:

- $v_3 - 10i_3 = 0$ (10Ω resistor)
- $i_5 = 0$, $v_{10} - Av_5 = 0$ (op-amp)
- $v_{19} - 2i_8 = 0$
  (CCVS with transresistance 2Ω)
- $v_7 = 10$ ($10\mathrm{V}$ source)
- $i_{10} + 1 = 0$ ($-1\mathrm{A}$ source)

each equation has the general form

$$\alpha_1 i_1 + \cdots + \alpha_b i_b + \beta_1 v_1 + \cdots + \beta_b v_b = \gamma$$

where α_i, β_i, and γ are constants (mostly zero!)

Equations – contd.

we can express all the branch equations in the form

$$Mi + Nv = s$$

where M and N are $b \times b$ matrices and s is a b-vector called the *source vector*:

$$s_k = \begin{cases} v_s & \text{branch } k \text{ is voltage source with value } v_s \\ i_s & \text{branch } k \text{ is current source with value } i_s \\ 0 & \text{otherwise} \end{cases}$$

for the example on page 4-15 of Lecture notes 4, the branch equations are:

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & -2 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & -3 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} .i + \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} .v = \begin{bmatrix} -1 \\ 0 \\ 0 \\ 0 \\ 2 \end{bmatrix}$$

note that most entries of M, N, and s are zero; only a few entries in each row are nonzero

Equations – contd.

putting it all together, our circuit equations are:

$$Ai = 0, \quad v = A^T e, \quad Mi + Nv = s$$

or, in one giant matrix equation,

$$\begin{bmatrix} A & 0_{n-1\times b} & 0_{n-1\times n-1} \\ 0_{b\times b} & I_{b\times b} & -A^T \\ M & N & 0_{b\times n-1} \end{bmatrix} \begin{bmatrix} i \\ v \\ e \end{bmatrix} = \begin{bmatrix} 0_{n-1} \\ 0_b \\ s \end{bmatrix}$$

where

- I means the identity matrix: $I_{ij} = \begin{cases} 1 & i = j \\ 0 & i \neq j \end{cases}$
- 0 means a zero matrix or vector
- the subscripts show the sizes of I and the various 0's (we won't show them henceforth)

$$\begin{bmatrix} A & 0 & 0 \\ 0 & I & -A^T \\ M & N & 0 \end{bmatrix} \begin{bmatrix} i \\ v \\ e \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ s \end{bmatrix}$$

Example

For the circuit on page 4-15 of Lecture notes 4, the giant matrix equation:

$$
\left[\begin{array}{ccccc|ccccc|ccc}
1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & -1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\hline
0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & -1 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & -1 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & -1 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & -1 & 1 \\
\hline
1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & -2 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & -1 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & -3 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
\end{array}\right]
\left[\begin{array}{c}
\\ \\ i \\ \\ \\ \\ \\ \\ v \\ \\ \\ \\ \\ e \\ \\
\end{array}\right]
=
\left[\begin{array}{c}
0 \\ 0 \\ 0 \\ \hline 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ \hline -1 \\ 0 \\ 0 \\ 0 \\ -2
\end{array}\right]
$$

note that for this example $n = 4$, $b = 5$, and
$2b + (n - 1) = 13$

Solving the equations

provided the big $(2b+n-1)\times(2b+n-1)$ matrix can be inverted, we have

$$\begin{bmatrix} i \\ v \\ e \end{bmatrix} = \begin{bmatrix} A & 0 & 0 \\ 0 & I & -A^T \\ M & N & 0 \end{bmatrix}^{-1} \begin{bmatrix} 0 \\ 0 \\ s \end{bmatrix}$$

- an explicit equation giving all branch currents, branch voltages, and node voltages
- a "one-line" solution of our circuit
- shows power of matrix manipulations
- shows that circuit variables are linear in the source variables (more on this later)
- computers don't compute the inverse of the big matrix; they solve the equations

$$\begin{bmatrix} A & 0 & 0 \\ 0 & I & -A^T \\ M & N & 0 \end{bmatrix} \begin{bmatrix} i \\ v \\ e \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ s \end{bmatrix}$$

  directly, using special methods (*sparse matrix techniques*) that exploit the fact that many of the entries are zero

Node voltage method

the node voltage method is an organized way to formulate the circuit equations into $(n-1)$ equations in the $(n-1)$ node voltage variables

- we first derive the method for circuits with only resistors and current sources
- we then show how the method can be extended to circuits that contain voltage sources and dependent sources (in addition to resistors and current sources)
- the node voltage method is very useful in analyzing complex circuits
  - the formulation is done by hand
  - the $(n-1)$ linear equations are solved by hand or by a computer to find the node voltages
  - branch currents and voltages can then be readily found

Basic node voltage method

consider circuit containing only

- resistors, and
- current sources

we label branches containing resistors as $1, 2, \ldots, r$

branches $r+1, r+2, \ldots, b$ are current sources

therefore,

$$\begin{aligned} i_k &= \frac{1}{R_k} v_k, \text{ for } 1 \leq k \leq r \text{ and} \\ i_k &= i^s_{k-r}, \text{ for } r < k \leq b \end{aligned}$$

in matrix form, the branch relations can be expressed as

$$i = Gv + i_{\text{src}},$$

where

$$G \triangleq \begin{bmatrix} \frac{1}{R_1} & & & & & \\ & \ddots & & & & \\ & & \frac{1}{R_r} & & & \\ & & & 0 & & \\ & & & & \ddots & \\ & & & & & 0 \end{bmatrix}, \quad i_{\text{src}} \triangleq \begin{bmatrix} 0 \\ \vdots \\ 0 \\ i^s_1 \\ \vdots \\ i^s_{b-r} \end{bmatrix}$$

Basic node voltage method – contd.

the circuit equations are thus

$$Ai = 0, \quad v = A^T e, \quad i = Gv + i_{\text{src}}$$

let's eliminate v and i from these equations . . .

- multiplying the branch matrix equation by A, we get $A(Gv + i_{\text{src}}) = Ai$
- from KCL, we get $A(Gv + i_{\text{src}}) = 0$, so $AGv = -Ai_{\text{src}}$
- now using KVL, $i.e.$, $v = A^T e$, we get the *node equations*

$$AGA^T e = -Ai_{\text{src}}$$

expresses circuit equations as $n - 1$ equations in $n - 1$ variables (cf. $2b + n - 1$ for the general formulation)

can get v and i once you know e

Writing the node equations by inspection

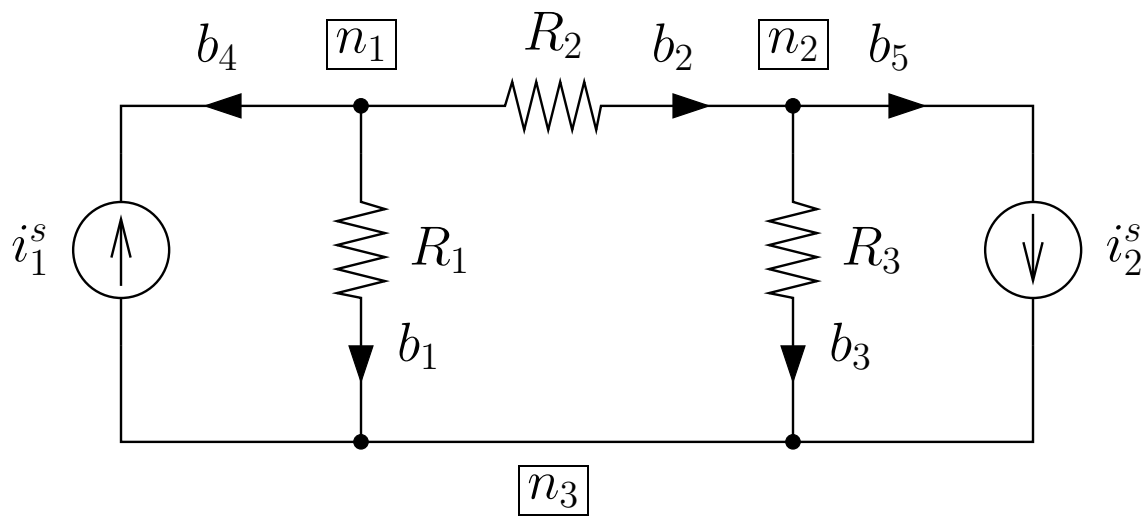
we can rewrite the node voltage equations in the form $Ye = \tilde{i}$, where

$$Y = AGA^T, \quad \tilde{i} = -Ai_{\text{src}}$$

it turned out that the entries of Y and $\tilde{i}$ can be found by inspection:

- $Y_{kk} =$ total conductance of resistors attached to node $\boxed{\text{k}}$
- $Y_{kl} = -$ total conductance of resistors connected directly between node $\boxed{\text{k}}$ and node $\boxed{\text{l}}$ ($= Y_{lk}$ too!)
- $\tilde{i}_k =$ total current from sources injected into node $\boxed{\text{k}}$

Example



let's write the node voltage equations in the form $Ye = \tilde{i}$, by inspection

$$\begin{bmatrix} \frac{1}{R_1} + \frac{1}{R_2} & -\frac{1}{R_2} \\ -\frac{1}{R_2} & \frac{1}{R_2} + \frac{1}{R_3} \end{bmatrix} \begin{bmatrix} e_1 \\ e_2 \end{bmatrix} = \begin{bmatrix} i_1^s \\ -i_2^s \end{bmatrix}$$

let's check this out

- the reduced node incidence matrix is

$$A = \begin{bmatrix} 1 & 1 & 0 & 1 & 0 \\ 0 & -1 & 1 & 0 & 1 \end{bmatrix}$$

Example – contd.

- branch relations are $i = Gv + i_{\text{src}}$, with

$$G = \begin{bmatrix} \frac{1}{R_1} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{R_2} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{R_3} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \quad i_{\text{src}} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ -i_1^s \\ i_2^s \end{bmatrix}$$

- now verify the equations we wrote by inspection

$$Y = AGA^T = \begin{bmatrix} \frac{1}{R_1} + \frac{1}{R_2} & -\frac{1}{R_2} \\ -\frac{1}{R_2} & \frac{1}{R_2} + \frac{1}{R_3} \end{bmatrix}$$

and

$$\tilde{i} = -Ai_{\text{src}} = \begin{bmatrix} i_1^s \\ -i_2^s \end{bmatrix}$$

we can also write the node equations without using the matrix notation:

- the KCL equations are

$$\begin{array}{lrcrcrcrcl} \text{node 1:} & i_1 & + & i_2 & + & & & i_4 & & = & 0 \\ \text{node 2:} & & & -i_2 & + & i_3 & + & & i_5 & = & 0 \end{array}$$

- the branch equations for the circuit are

$i_1 = \frac{v_1}{R_1}$, $i_2 = \frac{v_2}{R_2}$, $i_3 = \frac{v_3}{R_3}$, $i_4 = -i_1^s$, $i_5 = i_2^s$

Example – contd.

- substituting in the KCL equations we get

$$\begin{array}{rcrcrcrcl} \frac{v_1}{R_1} & + & \frac{v_2}{R_2} & - & & & i_1^s & = & 0 \\ & - & \frac{v_2}{R_2} & + & \frac{v_3}{R_3} & + & i_2^s & = & 0 \end{array}$$

- KVL gives

  $v_1 = e_1$, $v_2 = e_1 - e_2$, $v_3 = e_2$

- substituting, we get the node voltage equations

$$\begin{array}{rcrcl} (\frac{1}{R_1} + \frac{1}{R_2})e_1 & - & \frac{1}{R_2}e_2 & = & i_1^s \\ -\frac{1}{R_2}e_1 & + & (\frac{1}{R_1} + \frac{1}{R_3})e_2 & = & -i_2^s \end{array}$$

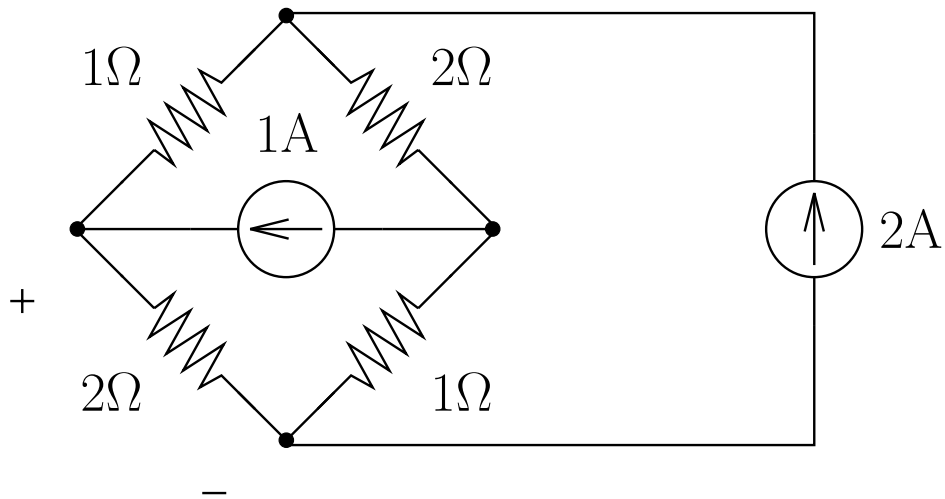
  the same as before

note that:

- for this example, node voltage method requires solving 2 equations in 2 unknowns; general method requires solving 12 equations in 12 unknowns
- sometimes it's actually easier for a computer to solve a larger set of equations ($e.g.$, if they are more sparse)

Another Example

let's write the node voltage equations for the circuit



$$\begin{bmatrix} \quad & \quad & \quad \\ \quad & \quad & \quad \\ \quad & \quad & \quad \end{bmatrix} \begin{bmatrix} \quad \\ \quad \\ \quad \end{bmatrix} = \begin{bmatrix} \quad \\ \quad \\ \quad \end{bmatrix}$$

Circuits with voltage sources

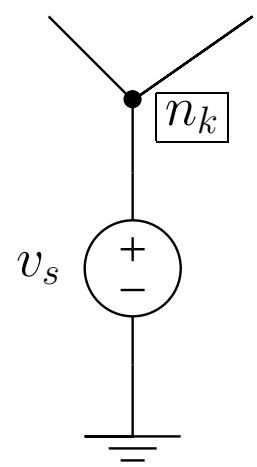
let's consider a circuit with resistors, current sources, and voltage sources

we look at three case:

Case 1: voltage source in series with a resistor

here we simply perform source transformation

Case 2: voltage source with one grounded node

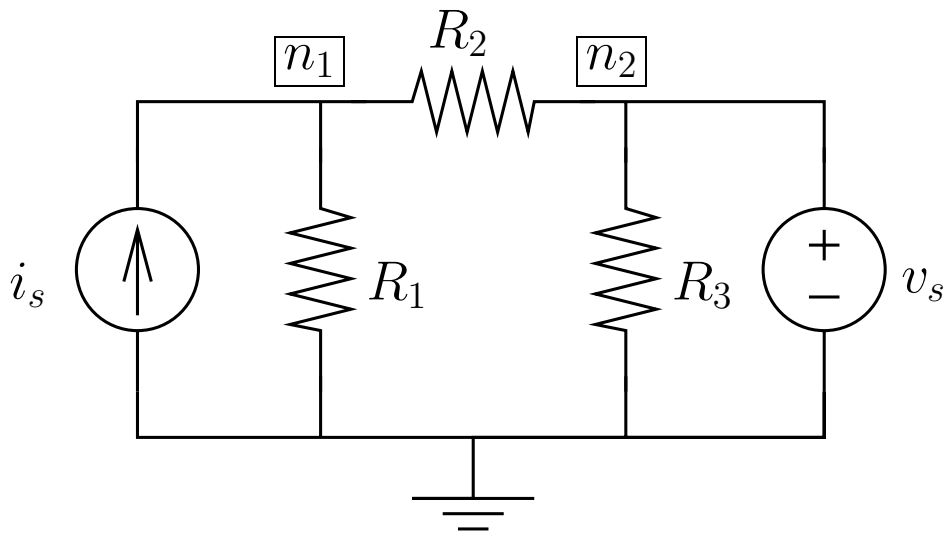


to write the node voltage equations:

- we write the node voltage equations for all nodes other than the grounded voltage source, which gives us $(n-2)$ equations in $(n-1)$ unknowns (assuming only one such voltage source in the circuit)
- the missing equation is simply: $e_k = v_s$

Circuits with voltage sources – contd.

Example:

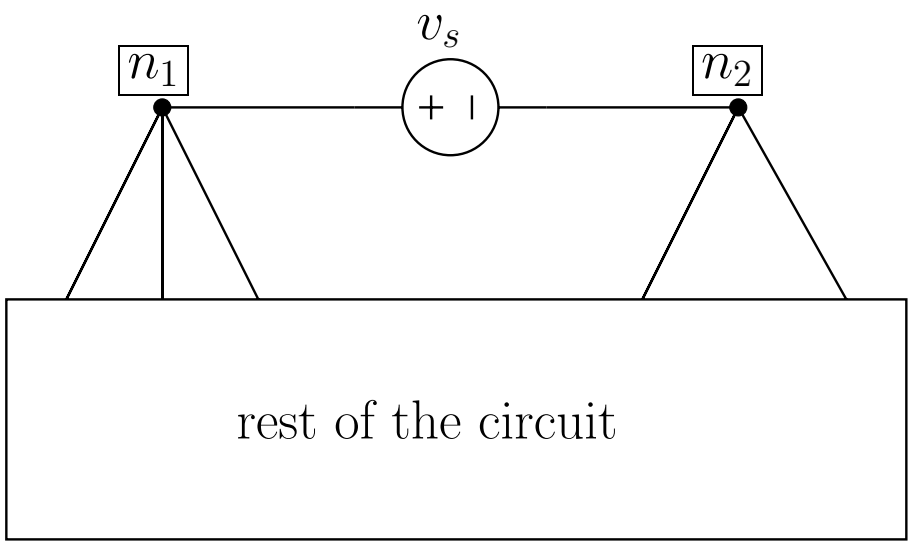


write the node voltage equations in the form $Ye = \tilde{i}$

$$\begin{bmatrix} & & \\ & & \\ & & \end{bmatrix} \begin{bmatrix} \\ \\ \\ \end{bmatrix} = \begin{bmatrix} \\ \\ \\ \end{bmatrix}$$

Circuits with voltage sources – contd.

Case 3: voltage source with no grounded node



to write the node voltage equations:

- we write the node voltage equations for all nodes other than the voltage source nodes, which gives us $(n-3)$ equations in $(n-1)$ unknowns (assuming only one such voltage source in the circuit)
- we know that $e_1 - e_2 = v_s$, so we need one more equation

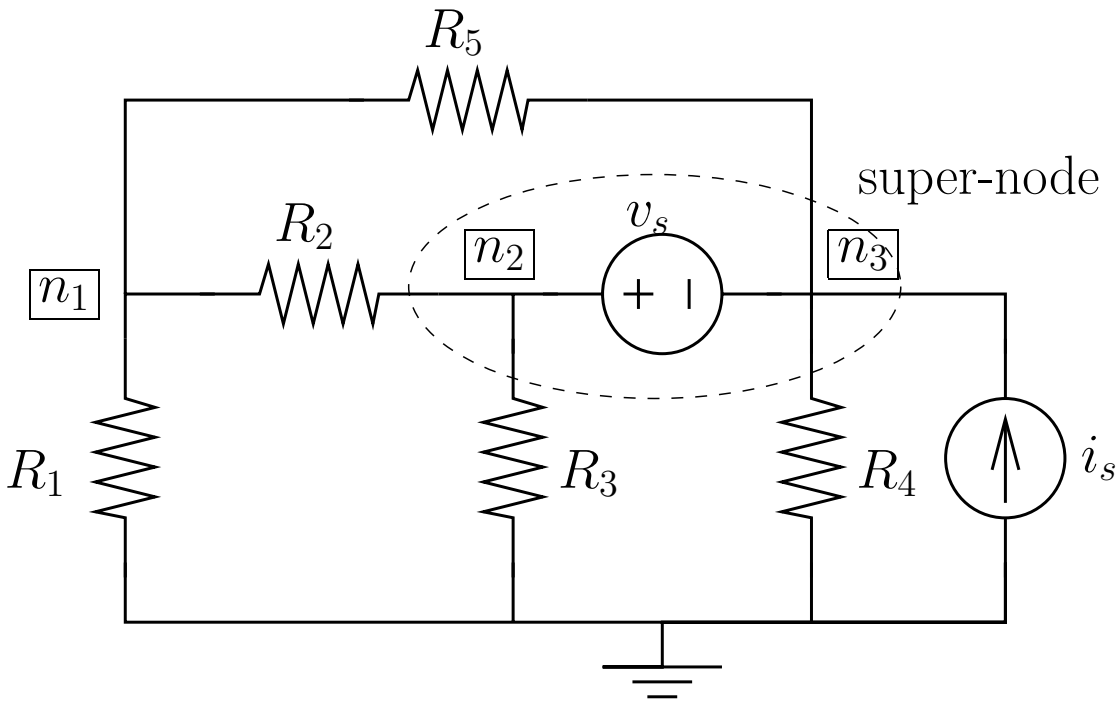
Circuits with voltage sources – contd.

- now we consider the voltage source nodes as a single *super-node*
  - by KCL we know that the sum of the currents leaving the super-node is zero
  - using branch equations we substitute into this KCL equation to find the missing equation
- the super-node equation can be found by inspection:

  denote the super-node by N

  - if node k is inside the super-node: $Y_{Nk} =$ total conductance of all resistors connected between node k and nodes outside the super-node
  - if node k is outside the super-node: $Y_{Nk} =$ $-$ total conductance of all resistors connected between the super-node and node k
  - $\tilde{i}_N =$ total current from sources injected into the super-node

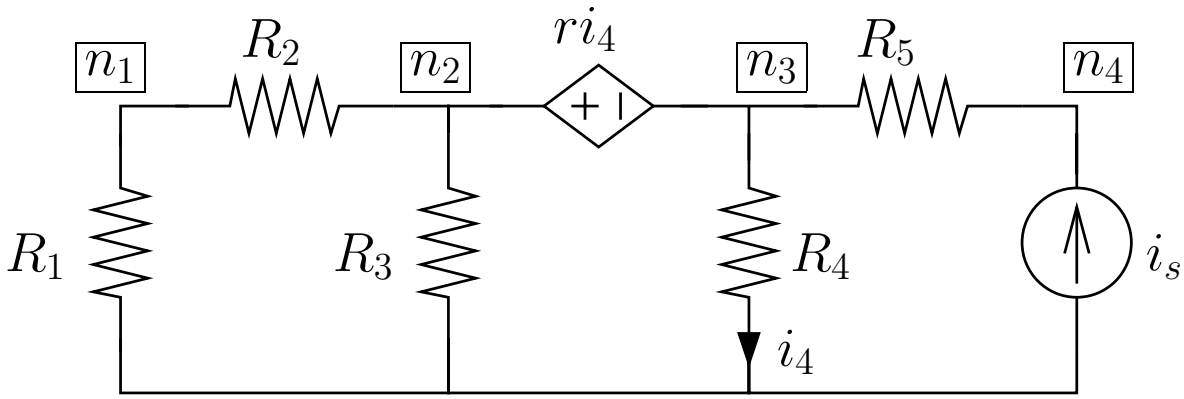
Example



$$\begin{bmatrix} \quad & \quad & \quad \\ \quad & \quad & \quad \\ \quad & \quad & \quad \end{bmatrix} \begin{bmatrix} \quad \\ \quad \\ \quad \end{bmatrix} = \begin{bmatrix} \quad \\ \quad \\ \quad \end{bmatrix}$$

Circuits with dependent sources

we explain this using an example



$$\begin{bmatrix} \quad & \quad & \quad & \quad \\ \quad & \quad & \quad & \quad \\ \quad & \quad & \quad & \quad \\ \quad & \quad & \quad & \quad \end{bmatrix} \begin{bmatrix} \quad \\ \quad \\ \quad \\ \quad \end{bmatrix} = \begin{bmatrix} \quad \\ \quad \\ \quad \\ \quad \end{bmatrix}$$

Superposition

back to general circuits with linear elements and sources

from the one-line formula

$$\begin{bmatrix} i \\ v \\ e \end{bmatrix} = \begin{bmatrix} A & 0 & 0 \\ 0 & I & -A^T \\ M & N & 0 \end{bmatrix}^{-1} \begin{bmatrix} 0 \\ 0 \\ s \end{bmatrix}$$

we see that the circuit variable vector is a *linear function* of the source vector s, so each circuit variable, $e.g.$, $v_k = \Sigma_i \, c_{ik} s_i$, for some constant coefficients c_{ik}

this means two things: scaling and superposition

Scaling: if α is any scaling factor, and v, i, and e are the circuit variables when the source vector is s, then: αv, αi, and αe are the circuit variables when the source vector is αs

if you scale all the sources by a fixed factor α, then every branch voltage, branch current and node voltage also scales by α

Superposition – contd.

Superposition: if

- i, v, and e are the circuit variables when s is the source vector
- $\tilde{i}$, $\tilde{v}$, and $\tilde{e}$ are the circuit variables when $\tilde{s}$ is the source vector

then, when the source vector is $s + \tilde{s}$, the circuit variables are $i + \tilde{i}$, $v + \tilde{v}$, $e + \tilde{e}$

or, in words:

suppose you analyze the circuit for two sets of source values, and then set the source values equal to the sum of these values

then every branch voltage, branch current and node voltage is the sum of what it was with the first set of source values, and what it was with the second set of source values

Superposition – contd.

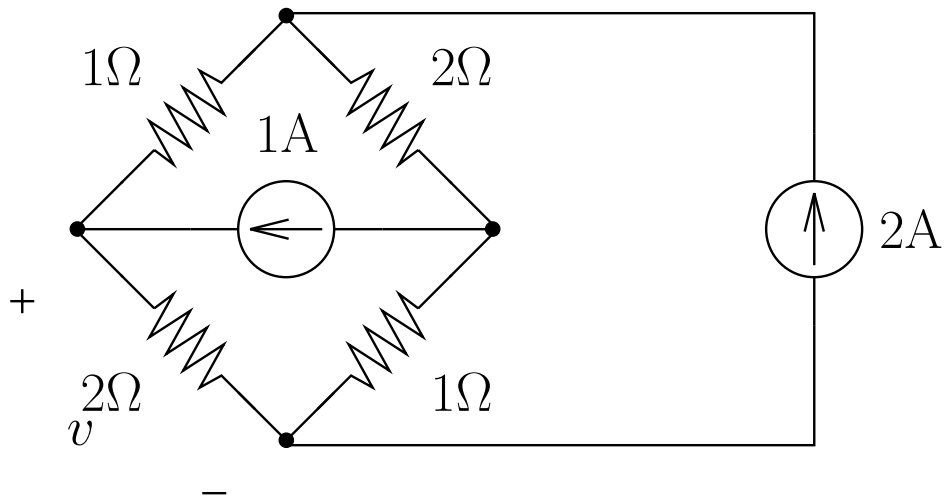
special case: turning sources on and off

any circuit variable (branch current, branch voltage, or node voltage) can be found as follows:

- find the value when all sources except one are turned off (when turned off replace voltage source by short circuit and current source by open circuit)
- to find the circuit variable values add up their values for all sources

(thus, we can speak of the 'contribution' of a circuit variable from any source in the circuit)

Example



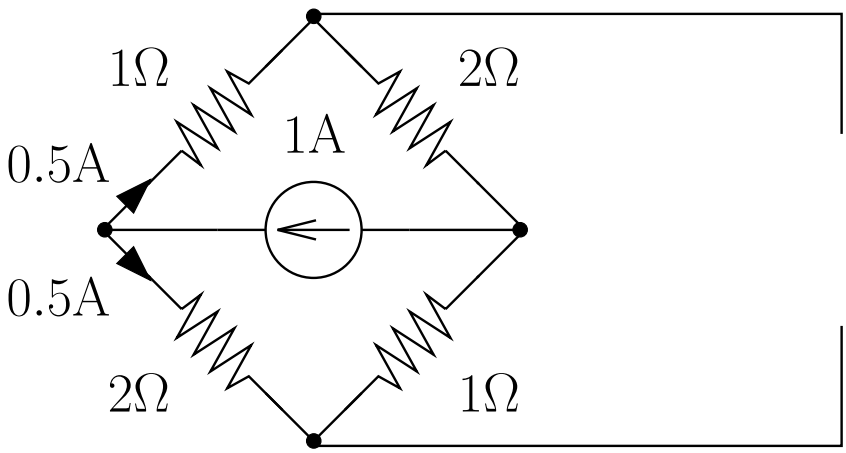
Find v, using superposition

$$v(\text{with both sources on}) = v(1\text{A source on; } 2\text{A source off}) + v(1\text{A source off; } 2\text{A source on})$$

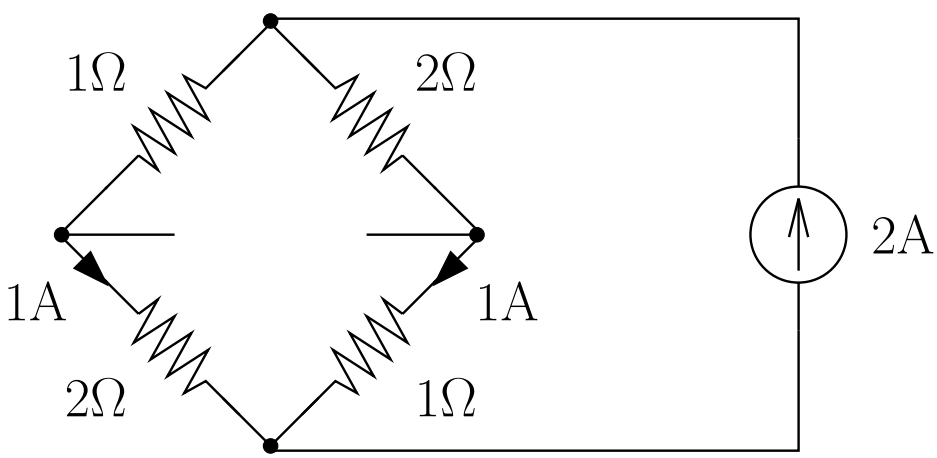
we'll analyze the two cases separately, then add

Example – contd.

start with the $1\mathrm{A}$ source on, $2\mathrm{A}$ source off:



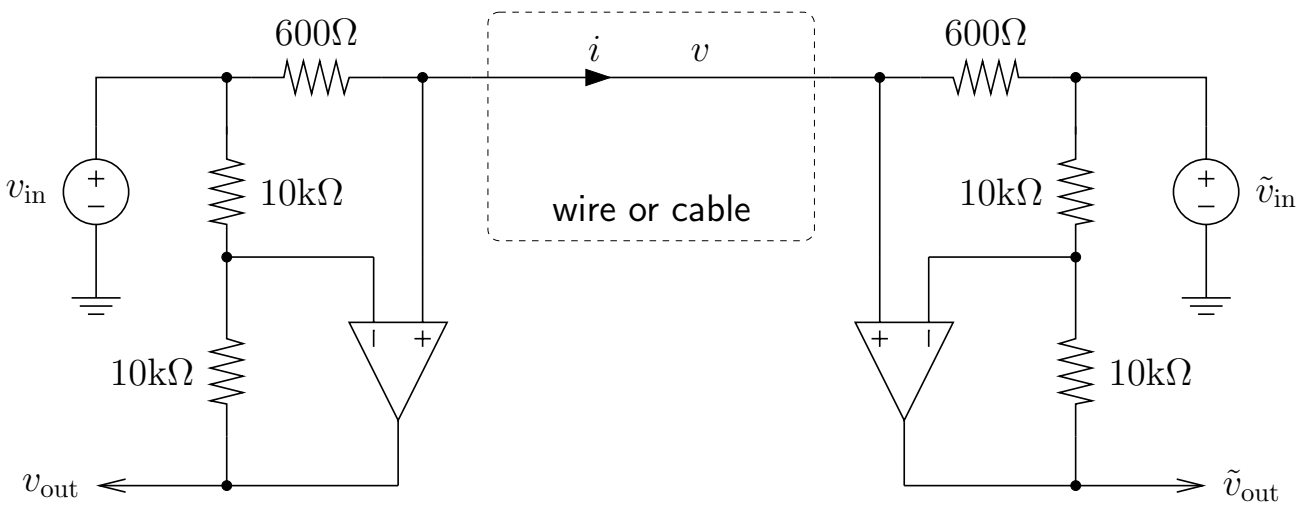
the current source sees two 3Ω resistances in parallel, so $\frac{1}{2}\mathrm{A}$ flows each direction; hence $v = 1\mathrm{V}$
now set the $1\mathrm{A}$ source off, the $2\mathrm{A}$ source on:



$1\mathrm{A}$ flows through each leg, so $v = 2\mathrm{V}$
now add the voltages for each case to get $v = 3\mathrm{V}$ (with both sources on)
question: What would v be if the $1\mathrm{A}$ source became a $10\mathrm{A}$ source?

Single-wire duplex transmission

this is an important application of superposition: transmitting signals in two directions, on a single wire, simultaneously



analysis:

- first assume that $\tilde{v}_{\rm in} = 0$ (turn the source off)
- then $v = v_{\rm in}/2$, so (check me!) $v_{\rm out} = 0$ and $\tilde{v}_{\rm out} = v_{\rm in}$
- now assume $v_{\rm in} = 0$
- then $v = \tilde{v}_{\rm in}/2$, so $\tilde{v}_{\rm out} = 0$ and $v_{\rm out} = \tilde{v}_{\rm in}$

Duplex transmission – contd.

by superposition we conclude that we always have

$$v_{\text{out}} = \tilde{v}_{\text{in}}, \quad \tilde{v}_{\text{out}} = v_{\text{in}}$$

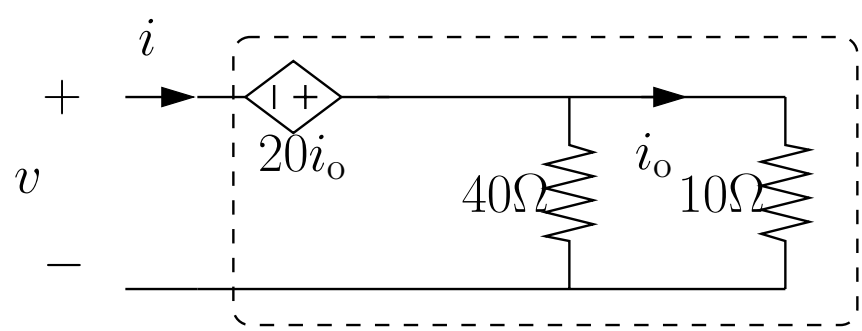
$i.e.$, each (voltage source) signal appears at the other side's output

- this is basic idea behind telephones, which use a special transformer called a hybrid
- circuit above is sometimes called an *active hybrid*

Thevenin and Norton equivalents

we have already seen many examples of the Thevenin and Norton equivalents:

- equivalent resistance — any two-terminal circuit consisting only of resistors is equivalent to a single resistor
- source transformation — voltage source v_s in series with resistor R_s equivalent to current source $\frac{v_s}{R_s}$ in parallel with R_s
- in HW2 we found that the following circuit is equivalent to a negative resistor



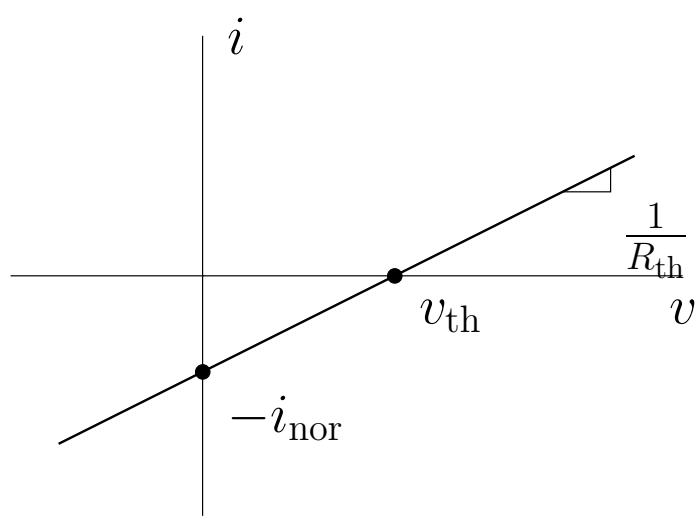
in all of these examples the two-terminal circuit $v - i$ relation is a straight line

Thevenin and Norton – contd.

in general, any two-terminal circuit consisting only of:

- linear elements (*e.g.*, resistors, dependent sources, op-amps, . . .), and
- (independent) voltage and current sources

has a $v - i$ relation that is a straight line:



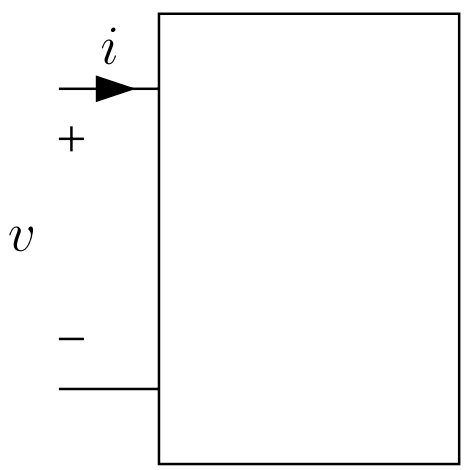
- R_{th} is called the Thevenin equivalent resistance
- v_{th} is called the Thevenin equivalent voltage
- $i_{\text{nor}} = v_{\text{th}}/R_{\text{th}}$ is called the Norton equivalent current

in equation form, the Thevenin equivalence says that:

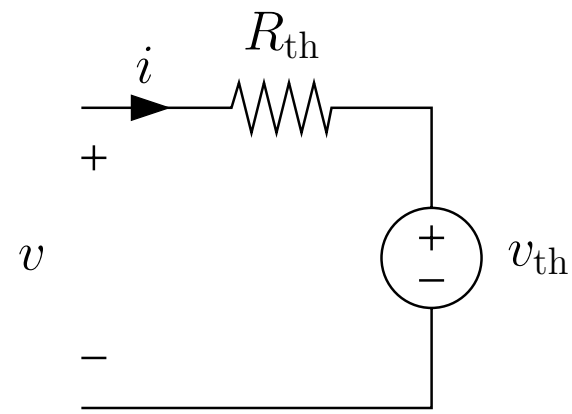
$$v = v_{\text{th}} + iR_{\text{th}}$$

Thevenin and Norton – contd.

schematically, the Thevenin equivalent circuit:

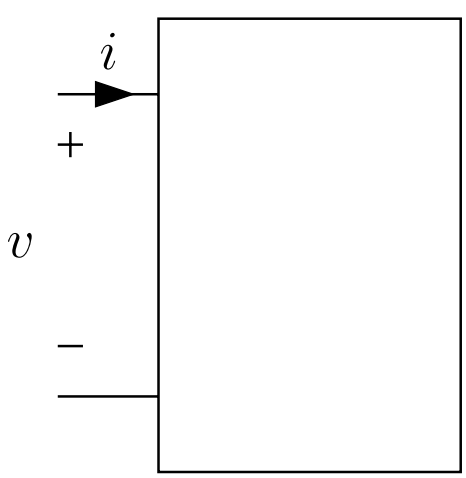


Two-terminal circuit

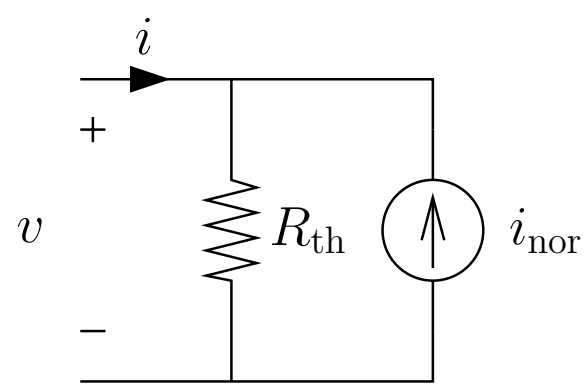


Thevenin equivalent

and by source transformation, the Norton equivalent circuit:



Two-terminal circuit

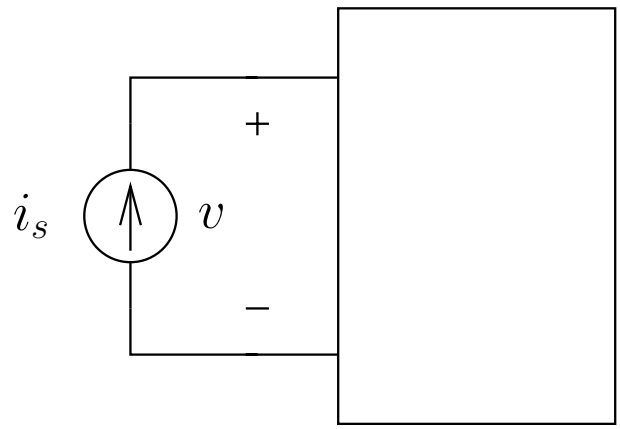


Norton equivalent

Proof of Thevenin equivalence

the proof follows from the giant matrix formula:
consider a two-terminal circuit with only linear elements and sources

- connect a current source i_s to the two terminals



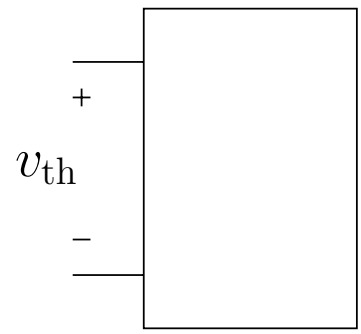
- to find v we use superposition:
  - turn off all sources inside the circuit: from the giant matrix formula, the contribution of the current source to v, denoted by v_1, is linear in i_s and we can write: $v_1 = R_{\text{th}} i_s$, for some constant that we denote by R_{th}
  - now turn off i_s and turn on all the sources in the circuit: denote the contribution to v by v_{th}
- by superposition: $v = v_{\text{th}} + i_s R_{\text{th}}$, which proves Thevenin equivalence

Finding Thevenin/Norton equivalents

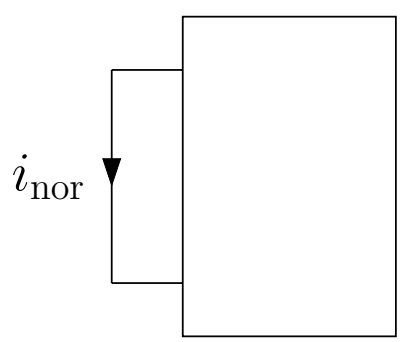
we describe two methods

Method 1: since the $v - i$ relation is a straight line, it can be determined if we know two points on it
two convenient points are when $i = 0$ and when $v = 0$:

- set $i = 0$, $i.e.$, open circuit and find $v_{\rm th}$ (open-circuit voltage)



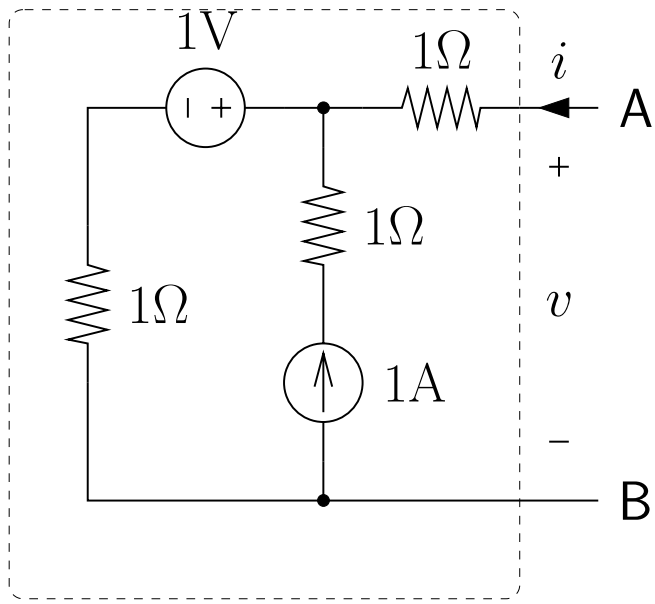
- set $v = 0$, $i.e.$, short circuit and find $i_{\rm nor}$ (short circuit current)



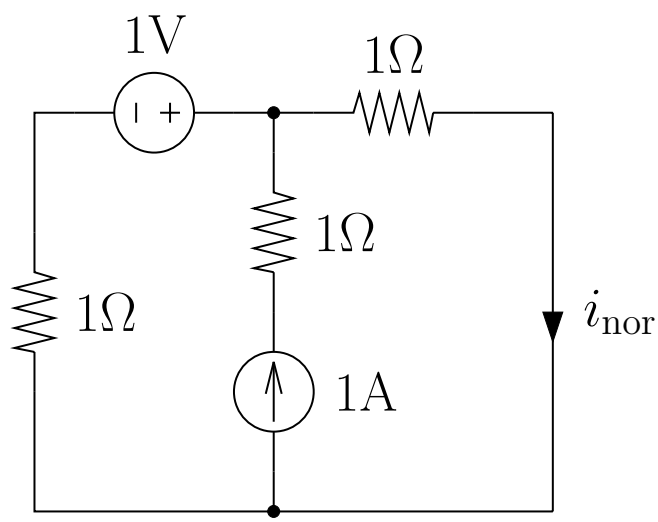
and $R_{\rm th} = v_{\rm th}/i_{\rm nor}$

Finding Thevenin equivalent – contd.

Example:



- open circuit voltage? $v_{\text{th}} = 2\text{V}$ (easy!)
- short circuit current?



$i_{\text{nor}} = 1\text{A}$ (not so easy)

so $R_{\text{th}} = 2\Omega$

Finding Thevenin equivalent – contd.

Method 2: the first method does not work when the circuit does not contain independent sources, since the v – i line goes through the origin, $i.e.$, $v_{\rm th} = 0$

the idea behind the second method is that the v–i relation, which is a straight line, can be determined by its slope and a single point on it

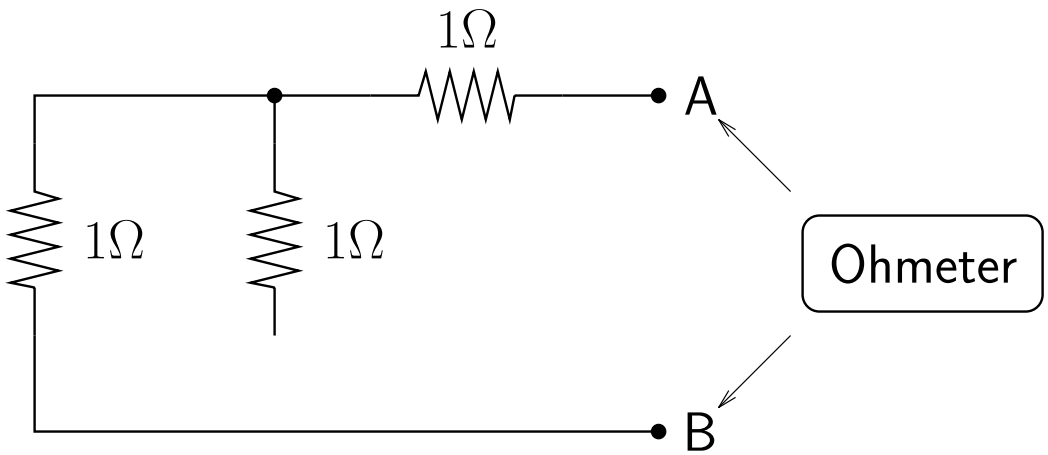
for example we can:

- find $v_{\rm th}$ (open circuit voltage)
- then turn off all independent sources in the circuit and find the equivalent resistance $R_{\rm th}$ (either using equivalent resistance or by applying a test voltage v and finding i as a function of v)

Finding Thevenin equivalent – contd.

let's try this on the previous example

we turn off the sources



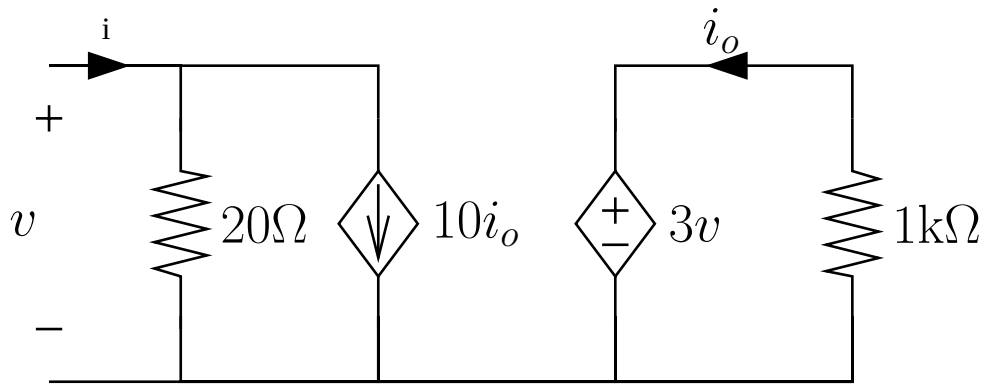
$R_{\text{th}} = 2\Omega$ (easy!)

so for this example this method is easier to apply than the first method

the second method works even if there are no sources, $e.g.$, circuit with only linear elements

in this case we know that $v_{\text{th}} = 0$ and we only need to find the equivalent resistance

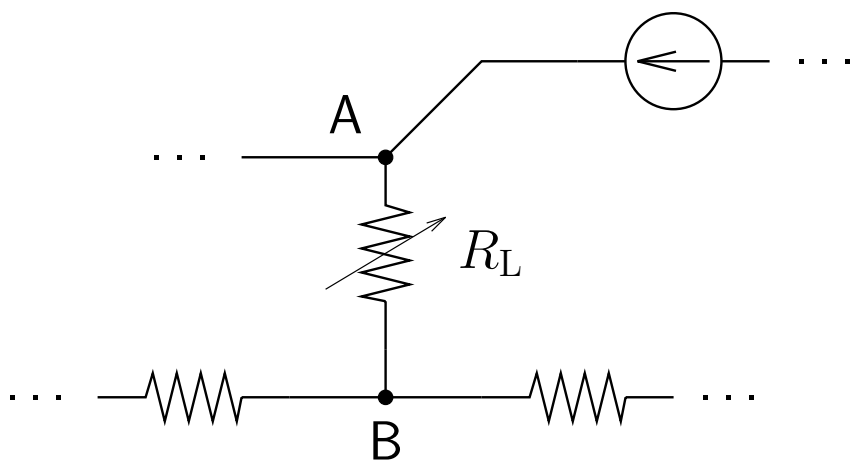
Example



find the Thevenin equivalent circuit

Application: maximum power transfer

consider a circuit containing only linear elements, sources, and a 'load' resistor R_{L}

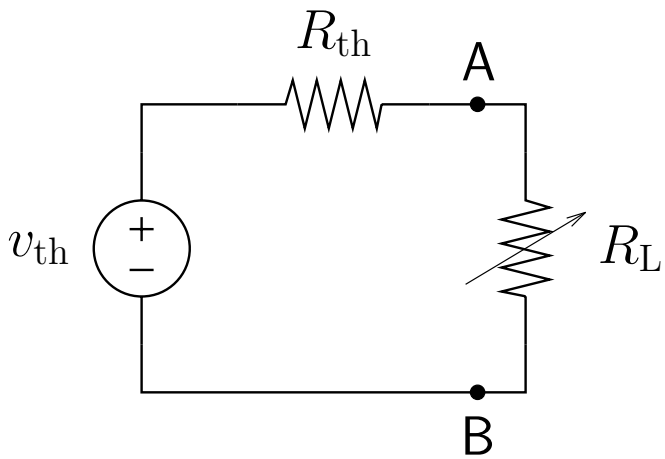


how do we choose $R_{\mathrm{L}} \geq 0$ to maximize its power dissipation?

- R_{L} small $\Rightarrow$ load voltage is small $\Rightarrow$ power dissipation is small
- R_{L} large $\Rightarrow$ load current is small $\Rightarrow$ power dissipation is small
- R_{L} somewhere in between is right ...

Maximum power transfer – contd.

use Thevenin equivalent of circuit w.r.t. A & B
(not including R_{L}):



. . . now it's easy to analyze!

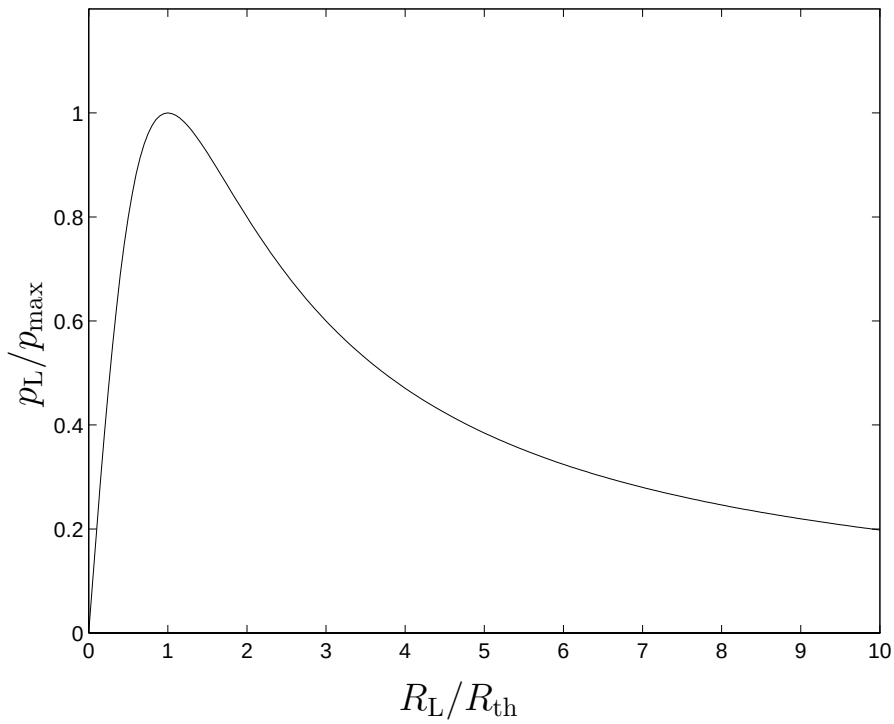
$$v_{\mathrm{L}} = v_{\mathrm{th}} \frac{R_{\mathrm{L}}}{R_{\mathrm{L}} + R_{\mathrm{th}}}$$

so power dissipated in R_{L} is

$$p_{\mathrm{L}} = \frac{v_{\mathrm{L}}^2}{R_{\mathrm{L}}} = \frac{v_{\mathrm{th}}^2}{R_{\mathrm{th}}} \frac{\frac{R_{\mathrm{L}}}{R_{\mathrm{th}}}}{(1 + \frac{R_{\mathrm{L}}}{R_{\mathrm{th}}})^2}$$

need to maximize w.r.t. R_{L}

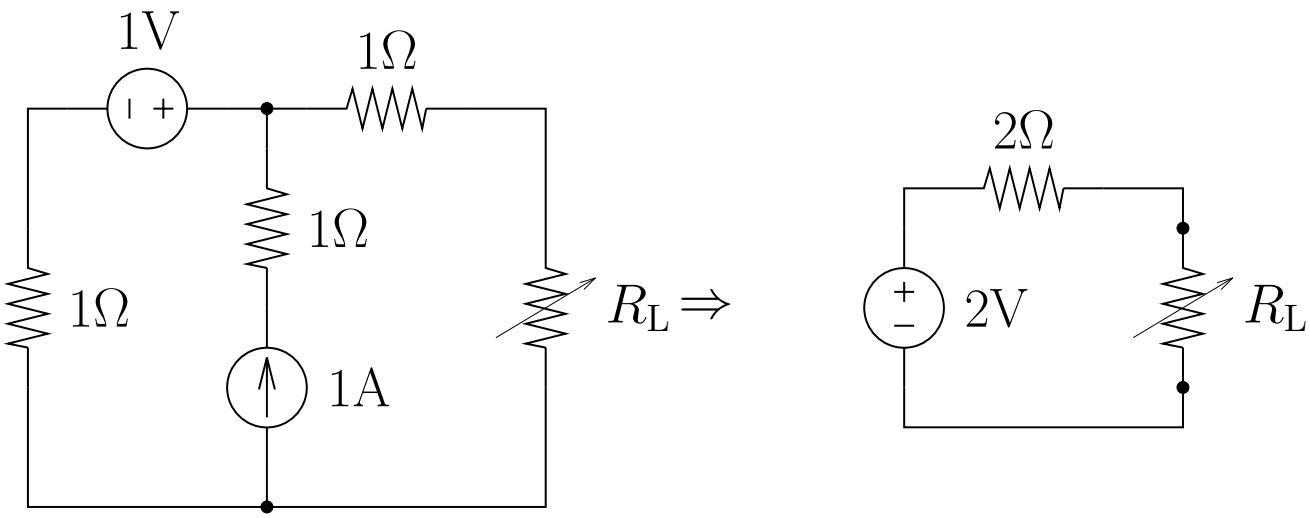
Maximum power transfer – contd.



- p_{L} is maximum when $R_{\mathrm{L}} = R_{\mathrm{th}}$
- max value is $p_{\mathrm{max}} = v_{\mathrm{th}}^2/(4R_{\mathrm{L}})$
- when $R_{\mathrm{L}} = R_{\mathrm{th}}$ we say that the source and load resistances are *matched*
- in practice, other considerations often limit selection of load resistance

Example

what value of R_{L} maximizes its power dissipation?

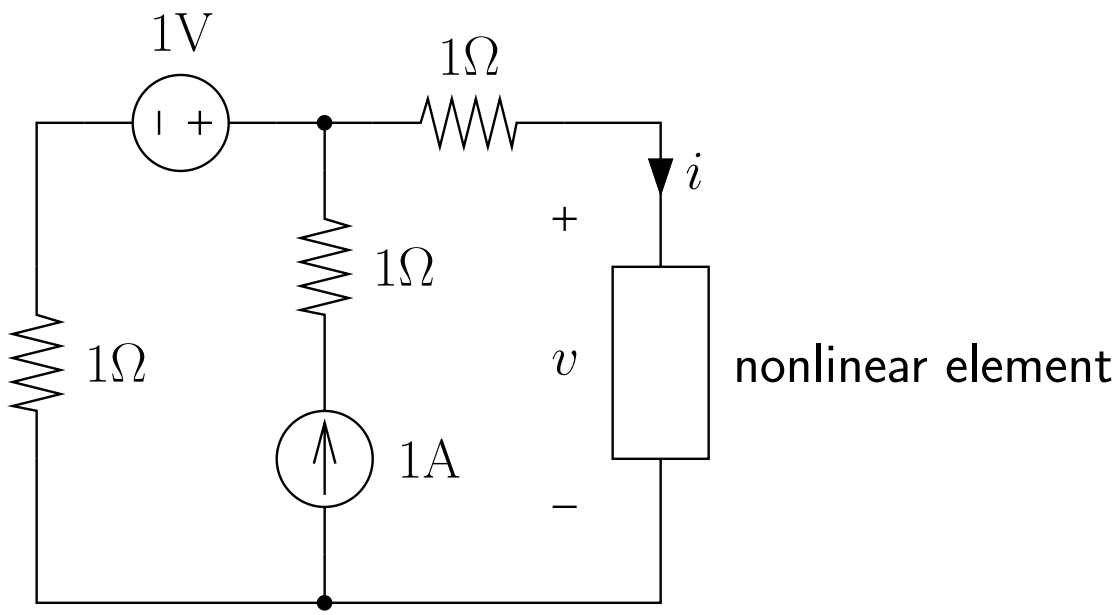


optimum load: $R_{\mathrm{L}} = 2\Omega$

Question: does the optimum R_{L} depend on the voltage and current source values?

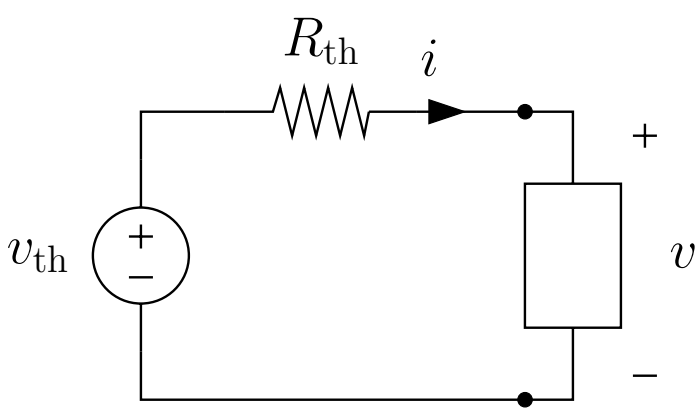
Another application: Load-line analysis

consider circuit containing only linear elements, sources, and one nonlinear element, *e.g.*



what are the voltages and currents in the circuit?

replace circuit (except nonlinear element) with Thevenin equivalent:

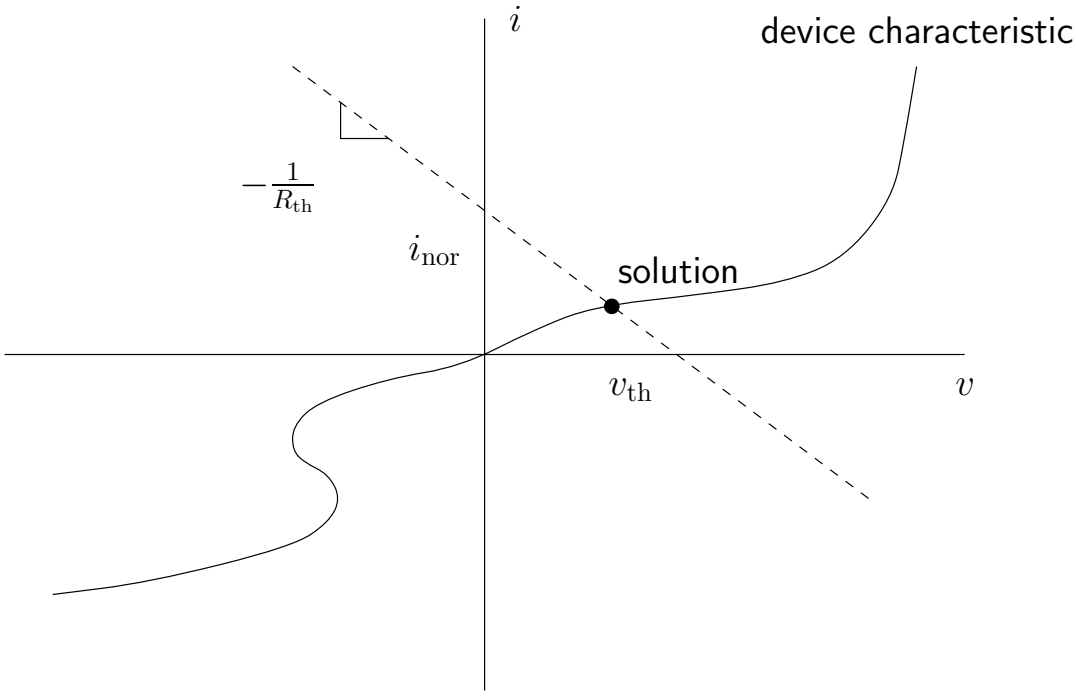


Load-line analysis – contd.

we seek solution of

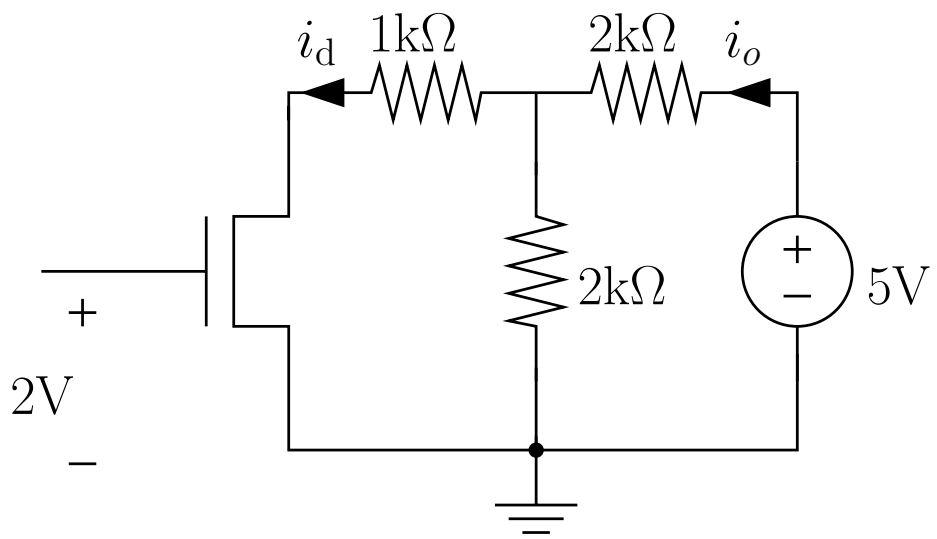
- nonlinear characteristic: $i = f(v)$
- from Thevenin equivalent: $v = v_{\rm th} - iR_{\rm th}$

load line analysis: we can solve these equations graphically (same as what we did in the analysis of the CMOS inverter . . .)
on v – i plane, plot nonlinear device characteristic, and also the 'load line' $v = v_{\rm th} - iR_{\rm th}$
intersection(s) give solutions



to find the voltages and currents in the rest of the circuit we can now replace the nonlinear element by either a voltage source $v_{\rm solution}$ or a current cource $i_{\rm solution}$

Example



assuming first order model with $v_\mathrm{t} = 0.7\mathrm{V}$ and $k = 2\mathrm{mA/V}^2$, find i_d and i_o

Lecture Notes 7
Small Signal Circuit Analysis

- linearized element model
- diode linearized and small signal models
- small signal circuit analysis
- MOS transistor small signal model
- Example: MOS amplifier

Small signal circuit analysis

in many cases the input to a circuit, $e.g.$, an amplifier, is the sum of:

- a constant (dc) voltage v_{bias} (*bias* is a traditional term for constant value around which a voltage or current fluctuates), and
- a *very small* signal (perturbation) v_{s}

the small signal may be the output from an antenna, a microphone, or a noise source (values ranging from $\mu\mathrm{V}$s to $\mathrm{m}\mathrm{V}$s)

we wish to find the change in the circuit branch voltages/ currents due to the small input signal source v_{s}, $i.e.$, contributions of v_{s} to the branch voltages/ currents

if the circuit consists only of linear elements and sources, we can use superposition:

turn off all sources in the circuit (including the dc input voltage v_{bias}) and find the contributions of the small signal source v_{s} to the branch voltages/ currents

Small signal circuit analysis – contd.

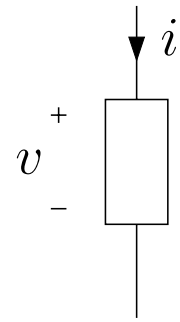
what if the circuit contains nonlinear elements, $e.g.$, diodes, transistors ?

we show that good *approximations* of the contributions of the small signal input to the branch voltages and currents can be found by:

- substituting *linearized* models for the nonlinear elements to obtain a circuit with only linear elements and sources (the result is called the *linearized circuit model*), and
- using superposition to simplify the circuit model ($i.e.$, obtain the *small signal circuit model*), which consists only of linear elements and the small signal source(s)

Linearized model of nonlinear element

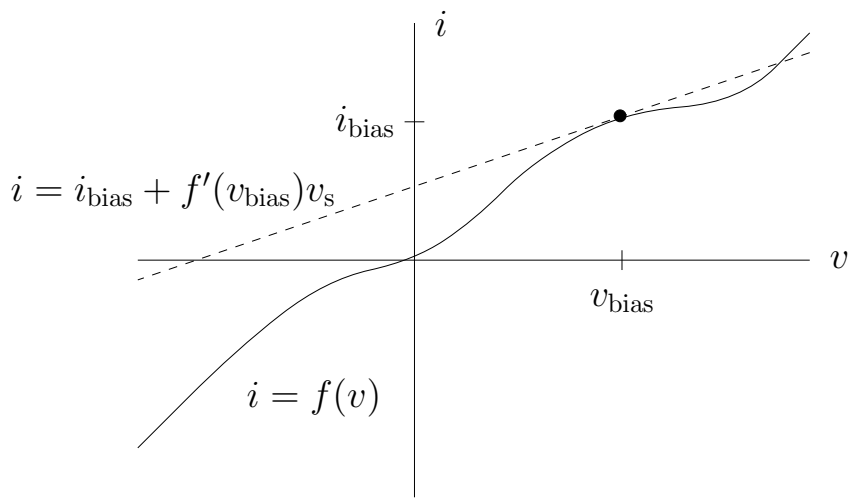
consider nonlinear element characterized by $i = f(v)$



suppose that $v = v_{\text{bias}} + v_{\text{s}}$
if $|v_{\text{s}}|$ is sufficently small, then by the Taylor Series expansion a good approximation of i is:

$$i \approx f(v_{\text{bias}}) + f'(v_{\text{bias}})(v - v_{\text{bias}}) = i_{\text{bias}} + f'(v_{\text{bias}})v_{\text{s}},$$

where $f'(v_{\text{bias}}) = (di/dv)\,|_{v=v_{\text{bias}}}$

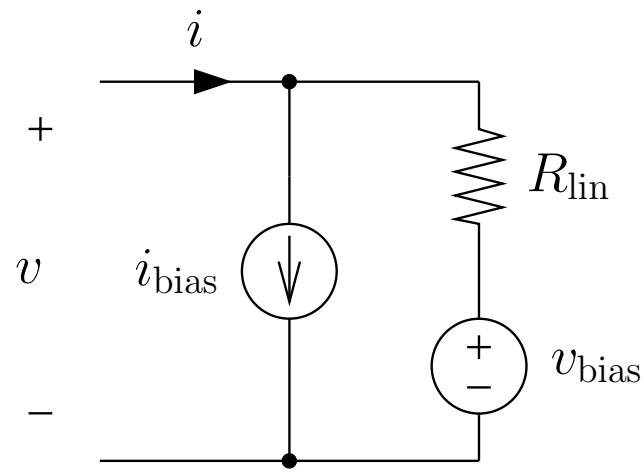


this is called the *linearized model* of the nonlinear element (around its bias point or condition v_{bias})

Linearized model – contd.

define $R_{\text{lin}} = 1/f'(v_{\text{bias}})\Omega$

the circuit representation of the linearized model:



the linearized model is very good approximation of nonlinear element for $v \approx v_{\text{bias}}$, is exact for $v = v_{\text{bias}}$

small signal model: the 'contribution' of the small signal v_{s} to the element current

$$i_{\text{s}} \triangleq i - i_{\text{bias}} \approx v_{\text{s}}/R_{\text{lin}}$$

the *linear* relation: $i_{\text{s}} = v_{\text{s}}/R_{\text{lin}}$ is called the *small signal model* of the nonlinear element around its bias point

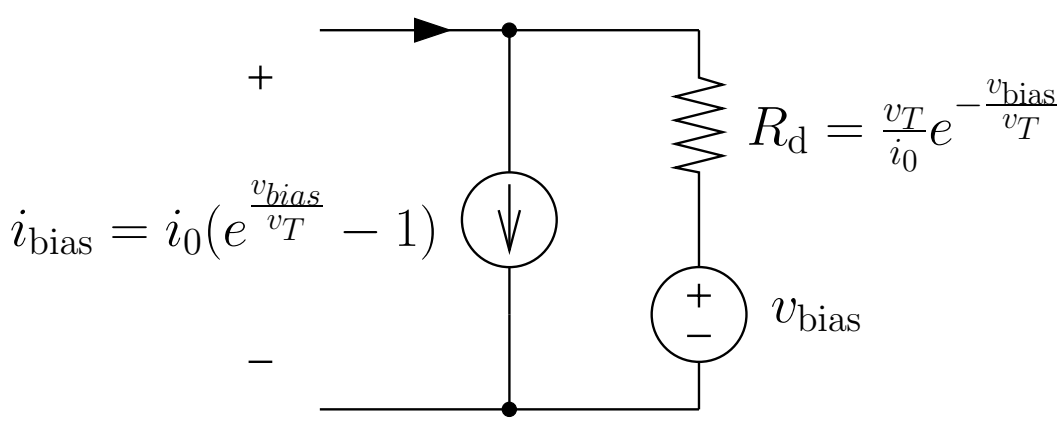
Diode linearized and small signal models

consider the exponential diode model:

$$i = i_0(e^{\frac{v}{v_T}} - 1)$$

now let $v = v_{\text{bias}} + v_{\text{s}}$, where again $|v_{\text{s}}|$ is small

the linearized diode model is given by:

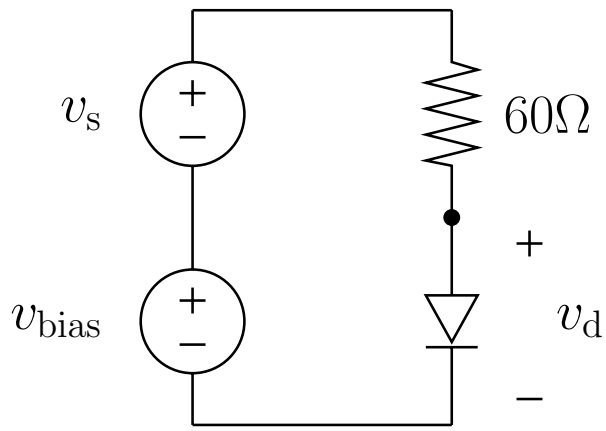


and the **small signal diode model** is:

$$i_{\text{s}} = v_{\text{s}}/R_{\text{d}}$$

Example

consider the diode circuit



find $v_{\rm d}$, assuming $i_0 = 10^{-14}{\rm A}$, $v_T = 26{\rm mV}$, $v_{\rm bias} = 1{\rm V}$ and $v_{\rm s} = 0.05{\rm V}$

we can find $v_{\rm d}$ directly, but let's do it using the linearized diode model:

to determine the parameters of the linearized diode model: $v_{\rm d}^{\rm bias}$, $i_{\rm d}^{\rm bias}$, and $R_{\rm d}$ at $v_{\rm bias} = 1{\rm V}$, we turn off $v_{\rm s}$ and analyze the circuit, and we get:

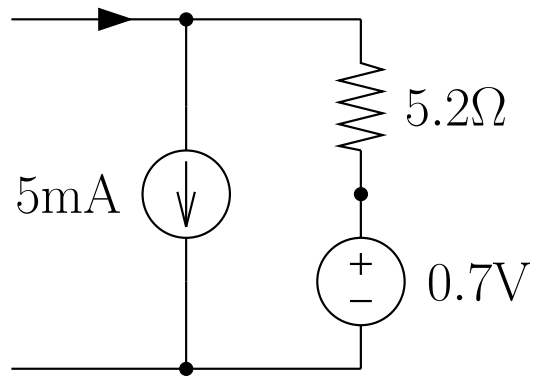
$$\begin{aligned} v_{\rm d}^{\rm bias} &= 0.7{\rm V}, \\ i_{\rm d}^{\rm bias} &= 5{\rm mA}, \text{ and} \\ R_{\rm d} &= 5.2\Omega \end{aligned}$$

this step is called **large signal** or **dc** circuit analysis

Example – contd.

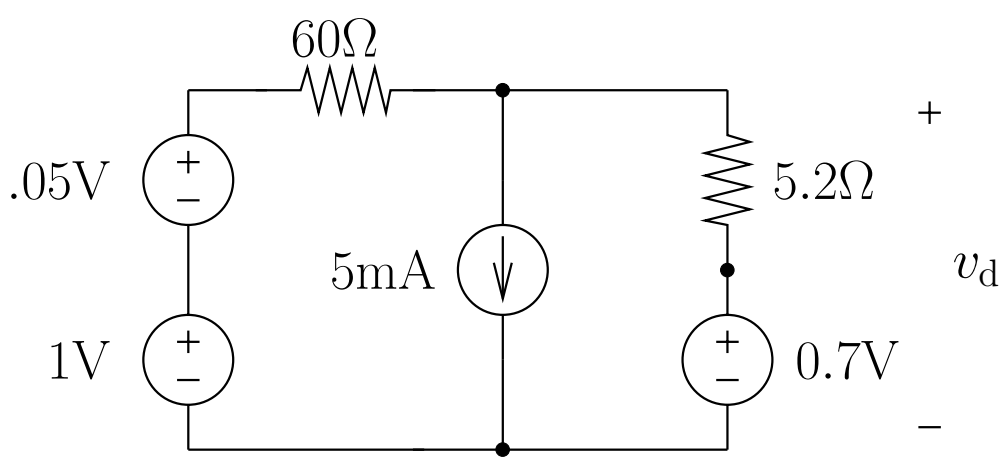
the linearized diode model near $v_{\mathrm{d}}^{\mathrm{bias}}$:

$$i \approx 5\mathrm{mA} + (1/5.2\Omega)(v_{\mathrm{d}} - 0.7\mathrm{V})$$



...this agrees with exponential diode when $v_{\mathrm{d}} = 0.7\mathrm{V}$, and is very good approximation for $v_{\mathrm{d}} \approx 0.7$

to address our question, we replace the diode in the circuit by its linearized model:

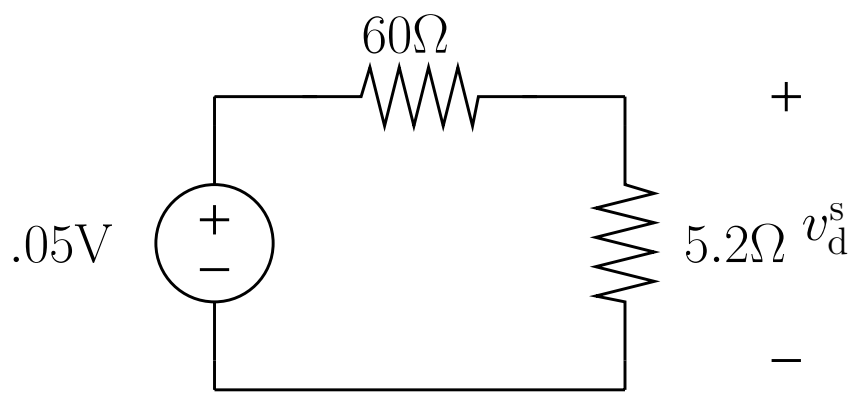


Example – contd.

we can analyze this circuit using superposition:

first we turn off the small signal source (and leave all other sources on) – we already know that $v_{\mathrm{d}}^{\mathrm{bias}} = 0.7\mathrm{V}$

now we turn off all sources except the small signal source:



the voltage on the diode due to the small signal, $v_{\mathrm{d}}^{\mathrm{s}} = 0.004\mathrm{V}$

so $v_d \approx 0.7 + 0.004\mathrm{V}$

the above circuit is called the **small signal circuit model** (of the original circuit) – when analyzing the effect of v_s on v_{d} we can simply replace the diode by its small signal model ($R = 5.2\Omega$ in this example) and turn off all sources other than v_{s}

Small signal circuit analysis

static circuit consisting of:

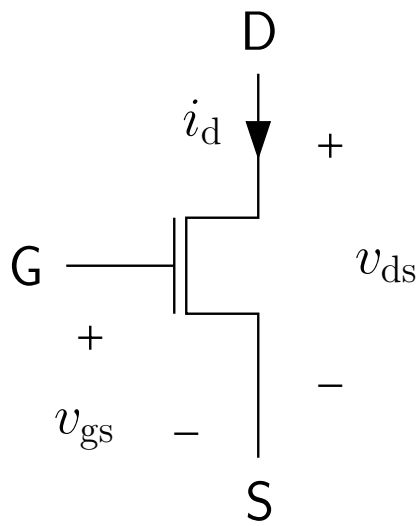
- linear and nonlinear elements and sources
- small signal source voltage or current source

to find the effect of the small signal source on the branch voltages and currents, we:

- turn off the small signal source and perform large signal (dc) analysis to find the voltages and currents (bias conditions) of the nonlinear elements
- turn off all sources, except the small signal source, and replace each nonlinear element by its small signal model around its bias point – the result is the small signal model of the circuit
- analyze the small signal circuit model to find the effect of the small signal source on the branch voltages/currents
- if we have more than one small signal source we can use superposition, since the small signal circuit consists only of linear elements and sources

MOS transistor small signal model

consider an nMOS transistor:



assume that it is in saturation, so

$$v_{\mathrm{ds}}^{\mathrm{bias}} > v_{\mathrm{gs}}^{\mathrm{bias}} - v_{\mathrm{t}}, \text{ and } i_{\mathrm{d}}^{\mathrm{bias}} = \frac{k}{2}(v_{\mathrm{gs}}^{\mathrm{bias}} - v_{\mathrm{t}})^2$$

let's develop linearized model when v_{gs} is very close to the bias voltage $v_{\mathrm{gs}}^{\mathrm{bias}}$

again using the Taylor Series expansion:

$$\begin{aligned} i_{\mathrm{d}} &\approx i_{\mathrm{d}}^{\mathrm{bias}} + \left.\frac{di_{\mathrm{d}}}{dv_{\mathrm{gs}}}\right|_{\mathrm{bias}} (v_{\mathrm{gs}} - v_{\mathrm{gs}}^{\mathrm{bias}}) \\ &= i_{\mathrm{d}}^{\mathrm{bias}} + k(v_{\mathrm{gs}}^{\mathrm{bias}} - v_{\mathrm{t}})(v_{\mathrm{gs}} - v_{\mathrm{gs}}^{\mathrm{bias}}) \end{aligned}$$

MOS small signal model – contd.

we define the *small signal transconductance* (in A/V) as:

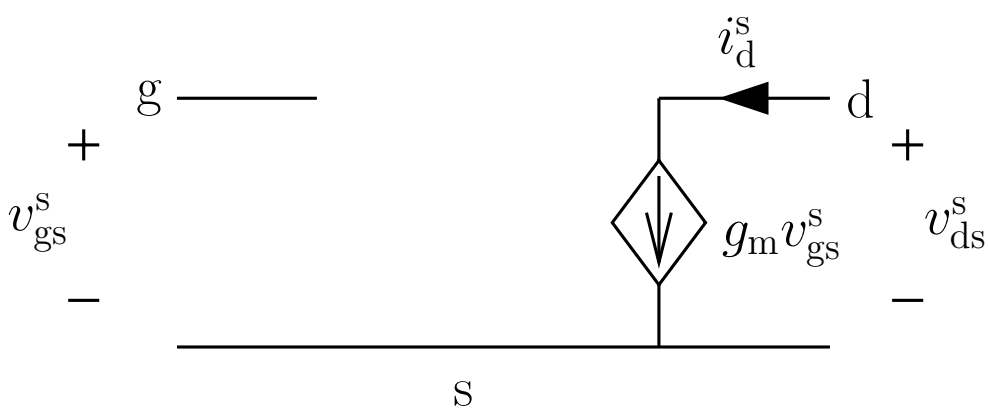
$$g_{\mathrm{m}} = k(v_{\mathrm{gs}}^{\mathrm{bias}} - v_{\mathrm{t}}) = \sqrt{2ki_{\mathrm{d}}^{\mathrm{bias}}},$$

a function of the drain bias current $i_{\mathrm{d}}^{\mathrm{bias}}$

the small signal model for the MOS transistor:

$$i_{\mathrm{d}}^{\mathrm{s}} \triangleq i_{\mathrm{d}} - i_{\mathrm{d}}^{\mathrm{bias}} = g_{\mathrm{m}} v_{\mathrm{gs}}^{s},$$

i.e., a linear VCCS



so in the small signal regime, an MOS transistor in saturation is a linear VCCS – desired transconductance value achieved by appropriately setting $v_{\mathrm{gs}}^{\mathrm{bias}}$

MOS small signal model – contd.

now let's plug in some numbers . . .

let $k = 2\mathrm{mA/V}^2$ and $v_\mathrm{t} = 0.7\mathrm{V}$,
and assume that $v_\mathrm{gs}^\mathrm{bias} = 1.7\mathrm{V}$ and $v_\mathrm{ds} > 1\mathrm{V}$ (so the transistor is in saturation)

the drain bias current:

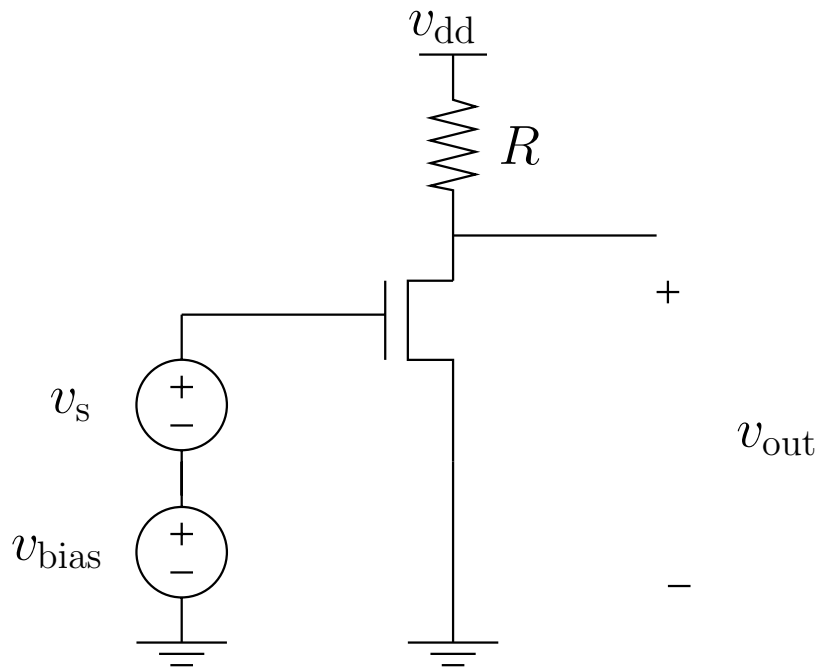
$$i_\mathrm{d}^\mathrm{bias} = \frac{k}{2}(v_\mathrm{gs}^\mathrm{bias} - v_\mathrm{t})^2 = 1\mathrm{mA}$$

so, the small signal transconductance

$$g_\mathrm{m} = \sqrt{2ki_\mathrm{d}^\mathrm{bias}} = 2\mathrm{mA/V}$$

Example: MOS amplifier

consider the simple MOS circuit:

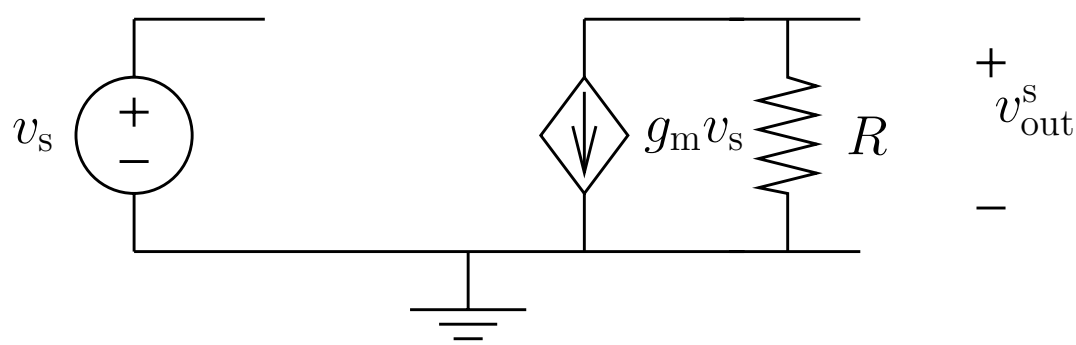


we wish to find the small signal $v_{\mathrm{s}} - v_{\mathrm{out}}^{\mathrm{s}}$ relation (you already analyzed the large signal model of this circuit under the name nMOS inverter in HW 3)

MOS amplifier – contd.

we find the small signal circuit model by replacing the MOS transistor by its small signal model (at its bias point), and turning off all sources in the circuit, except v_{s}

so we get:



the $v_{\mathrm{s}} - v_{\mathrm{out}}^{\mathrm{s}}$ relation is given by:

$$v_{\mathrm{out}}^{\mathrm{s}} = -g_{\mathrm{m}} R v_{\mathrm{s}}$$

and the circuit is an inverting linear amplifier with gain $g_{\mathrm{m}} R$ (in small signal regime around the bias point)

MOS amplifier – contd.

now let's plug in some numbers ...

let $k = 2\mathrm{mA/V}^2$, $v_\mathrm{t} = 0.7\mathrm{V}$, $v_\mathrm{dd} = 5\mathrm{V}$, $v_\mathrm{bias} = 1.7\mathrm{V}$ and $R = 3.5\mathrm{k}\Omega$

first we turn off the small signal source v_s and perform dc analysis

assuming that the MOS transistor is in saturation, $i_\mathrm{d}^\mathrm{bias} = 1\mathrm{mA}$

let's verify that it is in saturation:

by KVL: $v_\mathrm{ds}^\mathrm{bias} = 5 - 1\mathrm{mA} \times 3.5\mathrm{k}\Omega = 1.5\mathrm{V} > v_\mathrm{gs}^\mathrm{bias} - v_\mathrm{t}$

the small signal transconductance $g_\mathrm{m} = 2\mathrm{mA/V}$

so the amplifier relation is: $v_\mathrm{out}^\mathrm{s} = -7v_\mathrm{s}$

Question: How does the amplifier gain depend on:

- $v_\mathrm{gs}^\mathrm{bias}$?
- R ?
- v_dd ?

Summary and comments

- small signal analysis performed by:
  - finding the bias conditions of the nonlinear elements in the circuit (dc analysis)
  - replacing each nonlinear element in the circuit by its (linear) small signal model around its bias point
  - turning off all sources in the circuit, except the small signal source, and analyzing the resulting small signal circuit model
- small signal circuit analysis is a very important application of superposition
- circuit simulators use linearized models to iteratively solve the equations of circuits with nonlinear elements
- linearizing the nonlinear behavior of systems around *opertaing points* is widely used in engineering – linear systems are much easier to understand and analyze

Lecture Notes 8
Basic dynamic element models

- time varying sources
- capacitor
- application: the integrating amplifier
- capacitors in series and parallel
- inductor

Dynamic circuit models

- in *static* circuits voltages and currents do not change with time
- in *dynamic* circuits voltages and currents can change with time, $e.g.$,

  $v_{17}(t) = 3\cos(8t + 45°)$

  $$i_3(t) = \begin{cases} 0 & t < 2 \\ e^{-\frac{t}{2}} & t \geq 2 \end{cases}$$

- KCL and KVL hold for dynamic circuits *instantaneously*, at *all times*, $i.e.$,

  $$\begin{array}{ll} Ai(t) = 0 & \text{for all } t \\ v(t) = A^T e(t) & \text{for all } t \end{array}$$

  so power is conserved at all times

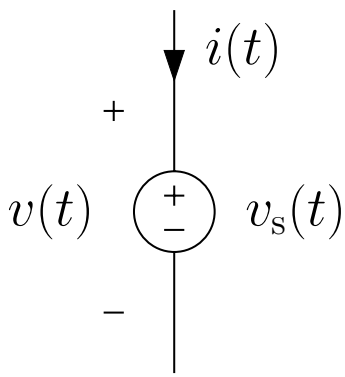
- a static circuit or element model is a *special case* of a dynamic model where branch relations do not vary with time, $e.g.$,

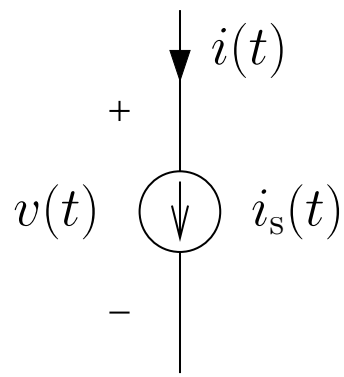
  $$\begin{array}{lll} 8\Omega \text{ resistor:} & v_7(t) = 8i_7(t) & \text{for all } t \\ 10\text{V source:} & v_{10}(t) = 10 & \text{for all } t \end{array}$$

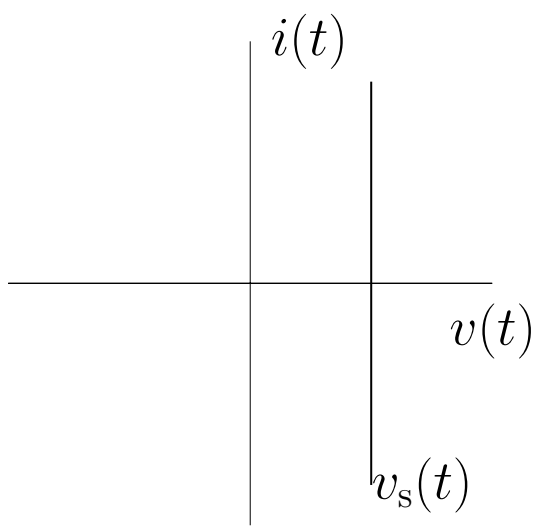
- a device, $e.g.$, transistor or op-amp, can have both static and dynamic models — static models used when voltages and currents change *very slowly* with time (examples of this later)

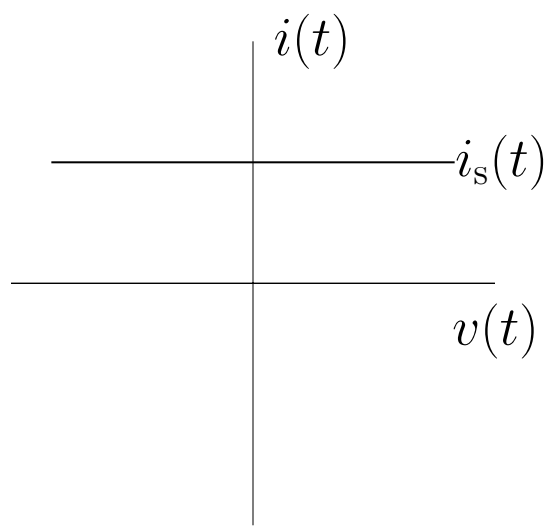
Time varying sources

we often encounter voltage and current sources that vary with time:





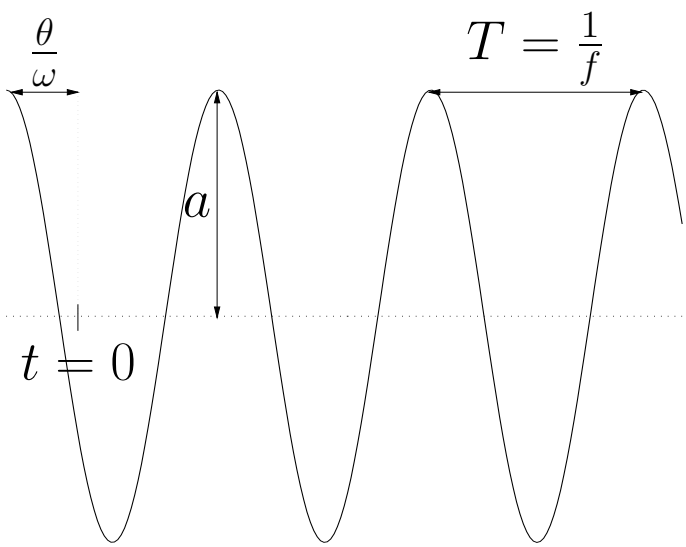




Examples of time varying sources

Sinusoidal source:

$v_{\mathrm{s}}(t) = a\cos(\omega t + \theta)$



- $a \geq 0$ is the *amplitude*
- $\omega \geq 0$ is the *frequency* in radian/sec $= 2\pi f$, f is the frequency in Hz
- θ is the *phase angle* or *phase shift* (in radians)
- sinusoidal signal is an example of a *periodic signal*, $i.e.$, a function $f(t)$ such that for some *period* T, $f(t+T) = f(t)$ for all t

Examples – contd.

good model for:

- AC power sources, *e.g.*,

$$v_{\mathrm{s}}(t) = 167\cos(120\pi t)$$

  how come it is $167\mathrm{V}$ not 120 ?

- *carrier* signals in communication systems, *e.g.*, radio, TV, wireless, cable

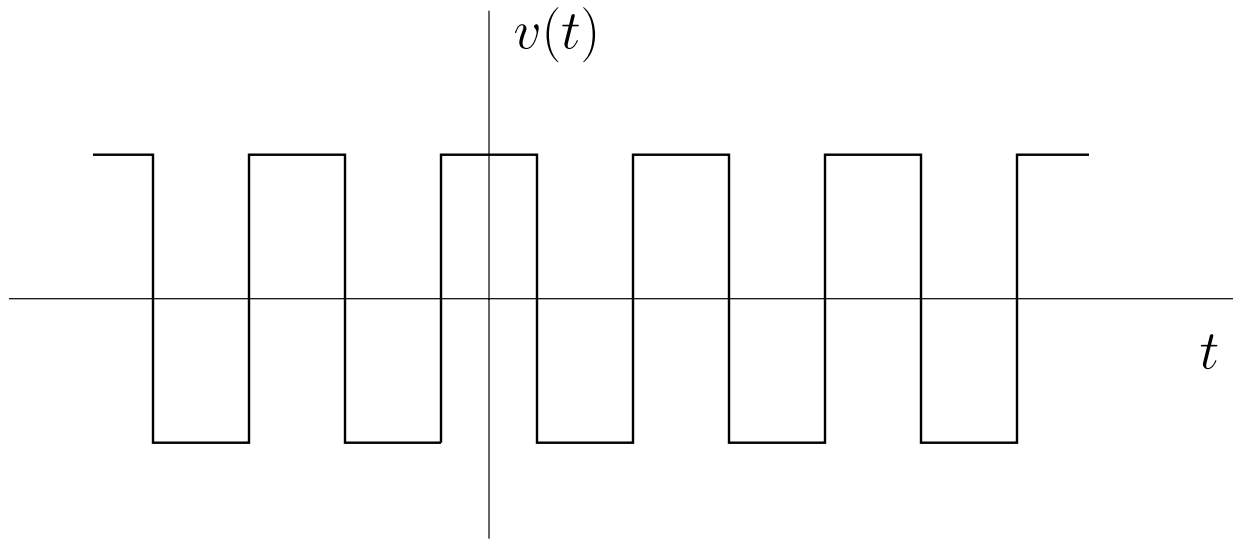
  Examples:

AM radio	500kHz – 1.5MHz
FM radio	$90 - 110$MHz
VHF TV	$50 - 200$MHz
UHF TV	500MHz – GHz
Cell phone	several GHz

as you will find out when you study Fourier Series and Transform (in EE 102 and beyond) almost all signals we encounter can be expressed as a linear combination (weighted sum) of sinusoidal signals with different frequencies

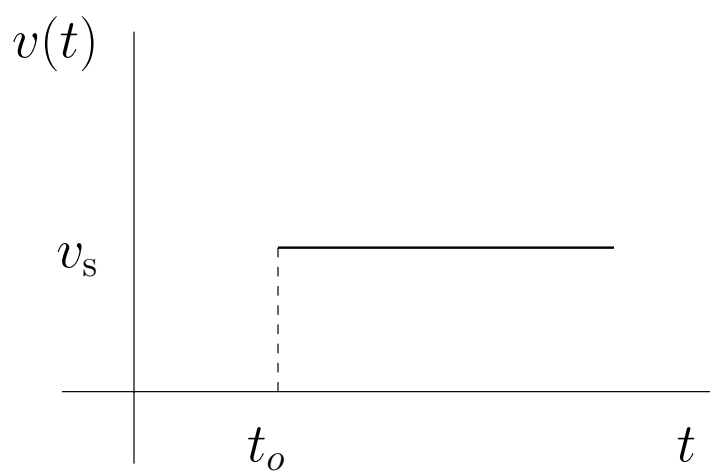
Examples – contd.

Square wave source:



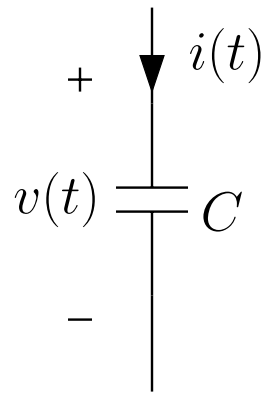
another example of a periodic signal
good model for clock signals in digital systems

Step function source:



good model for signals in digital circuits

Capacitor



- the fundamental *linear* capacitor relation is:

$$Q(t) = Cv(t)$$

  - $Q(t)$ is the charge stored on the capacitor at time t
  - $v(t)$ is the voltage on the capacitor
  - C is its *capacitance* in coul/$\mathrm{V} \triangleq$ Farad(F)

- taking derivatives, we get the more commonly used relation:

$$i(t) = C\frac{dv}{dt}$$

- capacitor is a linear *dynamic* element – both its relations (charge and current) satisfy scaling and superposition

Capacitor – contd.

- we encounter capacitances over a very wide range, from $\mathrm{fF}(10^{-15}\mathrm{F})$ to mF:

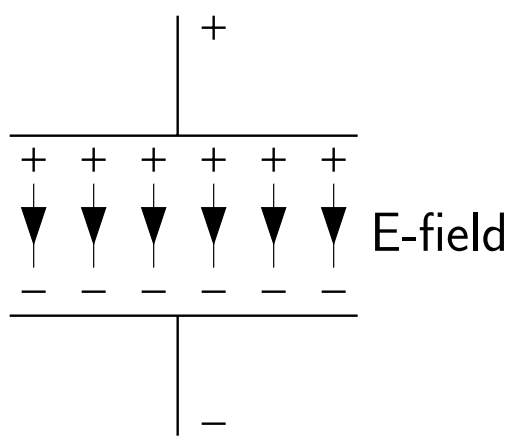
  Examples:

DRAM cell	$25\mathrm{fF}$
signal wire in an IC	$1\mathrm{fF}$ to $10\mathrm{pF}$
power supply capacitor	few mF

- in steady state (static condition), the capacitor acts as an *open circuit*, since:

$$v(t) \text{ const.} \;\Rightarrow\; \frac{dv}{dt} = 0 \;\Rightarrow\; i(t) = C\frac{dv}{dt} = 0.$$

- capacitor *stores* energy in the form of E-field:



Capacitor – contd.

the *instantaneous* power entering a capacitor at t is:

$$p(t) = i(t)v(t) = C\frac{dv}{dt}v(t) = \frac{d}{dt}(\frac{1}{2}Cv^2(t) + \text{constant})$$

so the energy stored in a capacitor

$$w(t) = \frac{1}{2}Cv^2(t) + \text{constant}$$

but by the fundamental capacitor relation:

$$v(t) = 0 \;\Rightarrow\; Q(t) = 0 \;\Rightarrow\; \text{no E-field} \;\Rightarrow\; w(t) = 0$$

and the stored energy is:

$$w(t) = \frac{1}{2}Cv^2(t)\text{J}$$

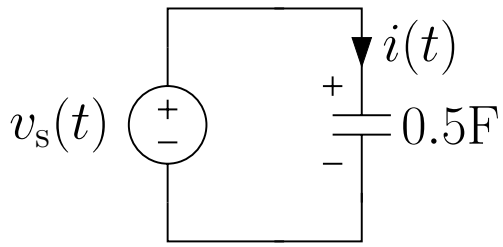
- capacitor is *lossless*, $i.e.$, it does not dissipate energy – energy/charge is *stored* and can be retrieved later (this is the basic idea behind DRAM operation)

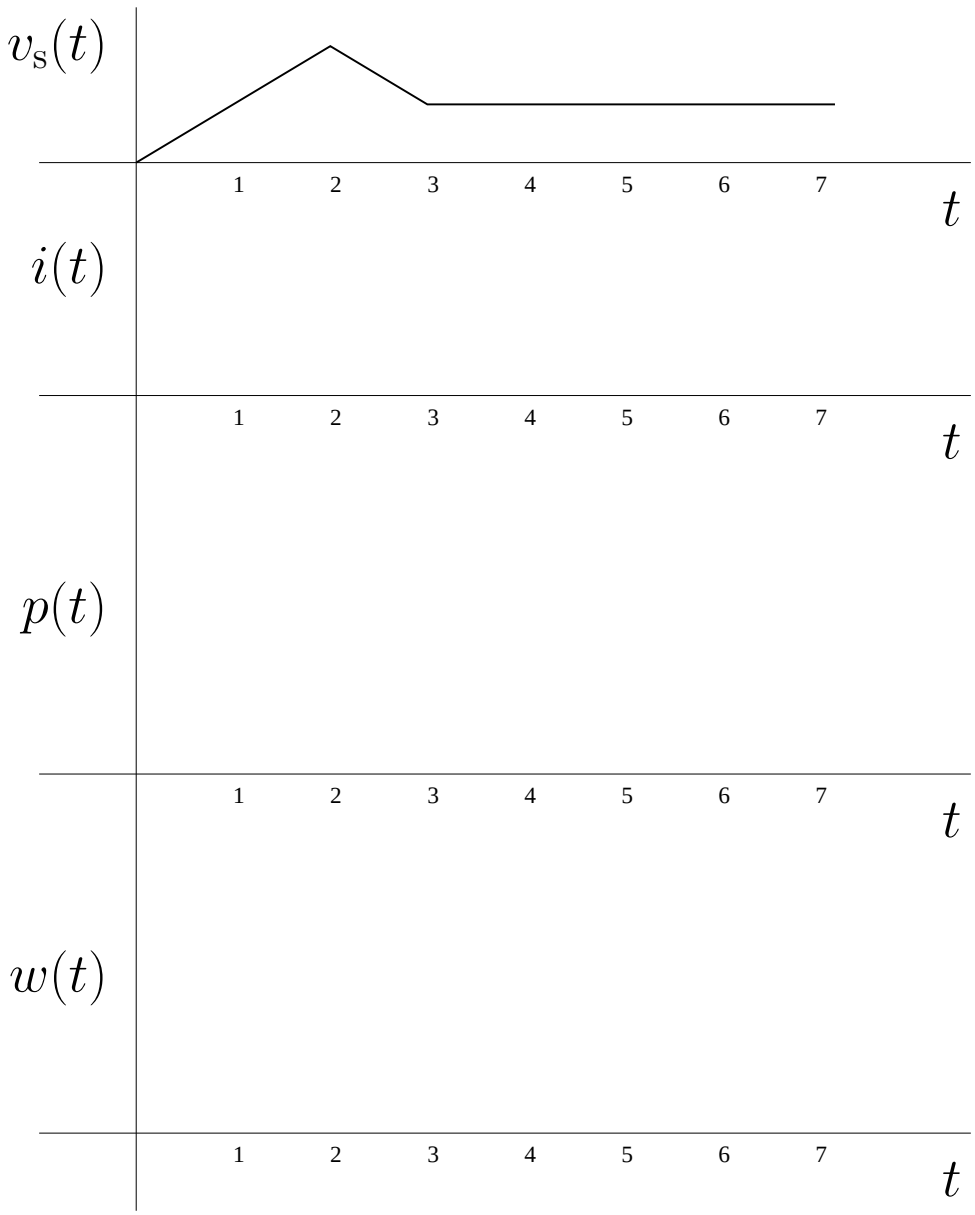
  to see why, note that the energy supplied to the capacitor from t_1 to t_2 (by the circuit),

$$\begin{aligned}\int_{t_1}^{t_2} i(t)v(t)\,dt &= \int_{v(t_1)}^{v(t_2)} Cv\,dv \\ &= \frac{1}{2}Cv^2(t_2) - \frac{1}{2}Cv^2(t_1),\end{aligned}$$

  is the same as the change in the energy stored in the capacitor from t_1 to t_2

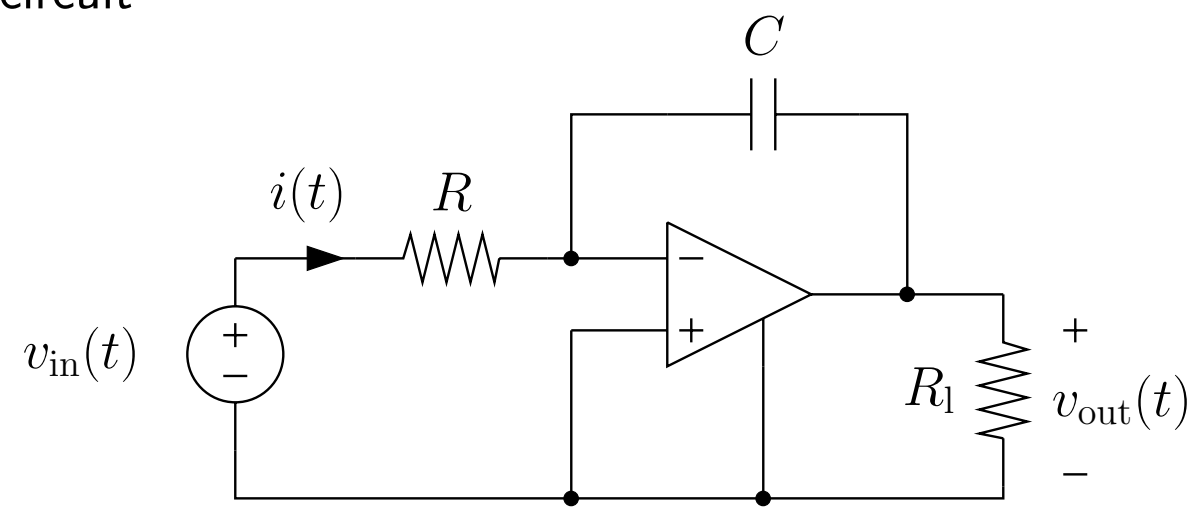
Example





Application: The integrating amplifier

let's use the capacitor relation to analyze an important circuit



assuming the ideal op-amp model, we want to find $v_{\rm out}$

- since $i_- = 0$ and by the capacitor relation $i(t)dt = Cdv_{\rm c}$
- integrating both sides from $\tau = 0$ to t, we get:

$$C(v_{\rm c}(t) - v_{\rm c}(0)) = \int_0^t i(\tau)d\tau$$

- since $v_- = v_+ = 0$, $i(t) = v_{\rm in}(t)/R$
  thus $v_{\rm c}(t) = -v_{\rm out}(t)$, and we get:

$$v_{\rm out}(t) = -v_{\rm c}(0) - \frac{1}{RC}\int_0^t v_{\rm in}(\tau)d\tau$$

  thus the output voltage (assuming $v_{\rm c}(0) = 0$) is proportional to the integral of the input voltage

The integrating amplifier – contd.

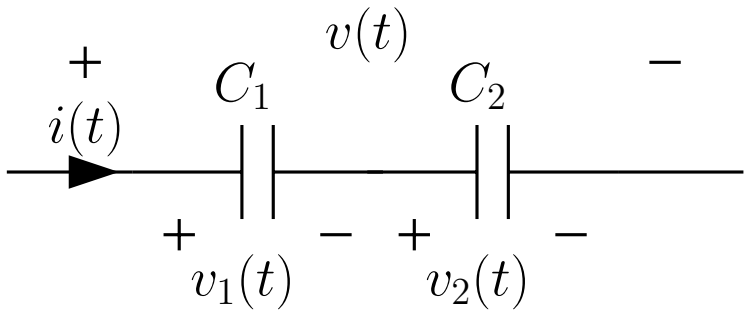
Example:

let $v_{\mathrm{in}}(t) = \begin{cases} 0 & t < 0 \\ v_{\mathrm{s}} & t \geq 0 \end{cases}$

find v_{out} for $t \geq 0$ asuming that $v_{\mathrm{c}}(0) = 0$

Capacitors in series

series connection:



- from the capacitor relation and KCL:

$$i(t) = C_1 \frac{dv_1}{dt} = C_2 \frac{dv_2}{dt}$$

- by KVL: $v(t) = v_1(t) + v_2(t)$, thus

$$\frac{dv}{dt} = \frac{dv_1}{dt} + \frac{dv_2}{dt}$$

- substituting from the capacitor relation and KCL:

$$i(t) = \frac{C_1 C_2}{C_1 + C_2} \frac{dv}{dt}$$

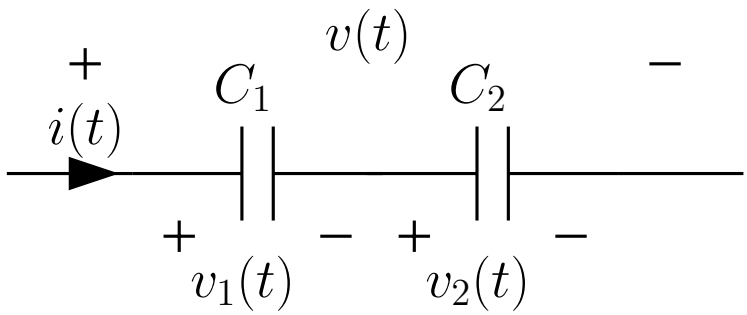
  conclusion:

  – two capacitors in series equivalent to a single (smaller) capacitor

  – capacitors in series like resistors in parallel

Voltage divider

for two capacitors in series:



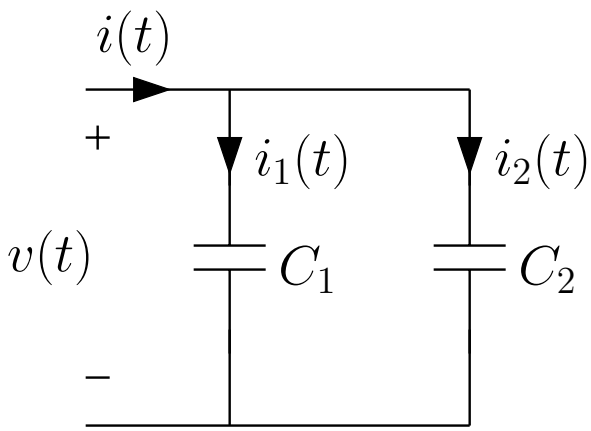
$$v_1(t) = \frac{C_2}{C_1 + C_2} v(t)$$

and

$$v_2(t) = \frac{C_1}{C_1 + C_2} v(t)$$

Capacitors in parallel

parallel connection:



- by KCL: $i(t) = i_1(t) + i_2(t)$
- by capacitor relation:

$$i_1 = C_1 \frac{dv}{dt}, \; i_2 = C_2 \frac{dv}{dt}$$

- thus:

$$i = (C_1 + C_2) \frac{dv}{dt},$$

  $i.e.$, capacitors C_1, C_2 in parallel add (similar to resistors in series)

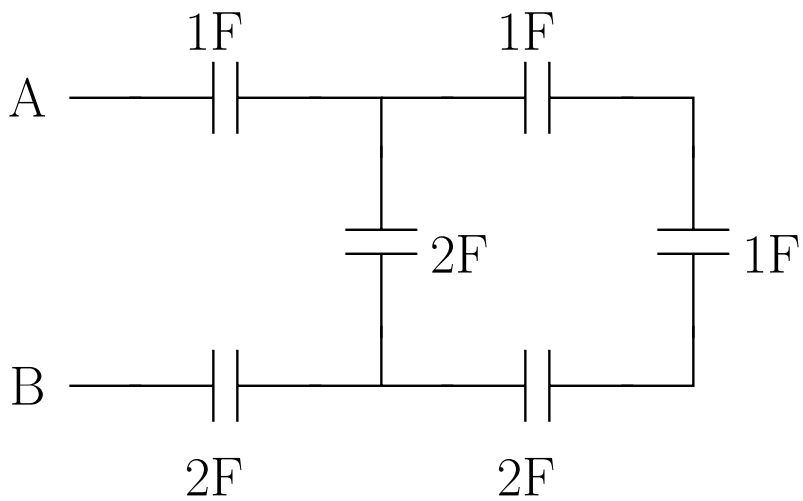
current divider: for two capacitors in parallel

$$i_1(t) = \frac{C_1}{C_1 + C_2} i(t), \quad i_2(t) = \frac{C_2}{C_1 + C_2} i(t)$$

Capacitance equivalence

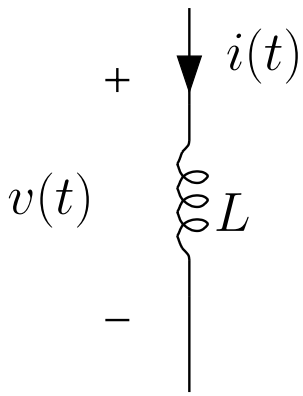
any two-terminal circuit consisting only of capacitors is electrically equivalent to a single capacitor

Example:



find the equivalent capacitance

Inductor



- the fundamental relation of a (linear) inductor is:

$$\Phi(t) = Li(t)$$

  - $\Phi(t)$ is the magnetic flux (in Weber)
  - L is the inductance in $\frac{\text{volts}}{\text{amp/sec}} = \frac{\Omega}{\text{sec}} \triangleq$ Henry(H)

- taking derivatives we get the more familiar relation:

$$v(t) = L\frac{di}{dt}$$

- inductor is a linear dynamic element
- we encounter inductances ranging from nHs to mHs:

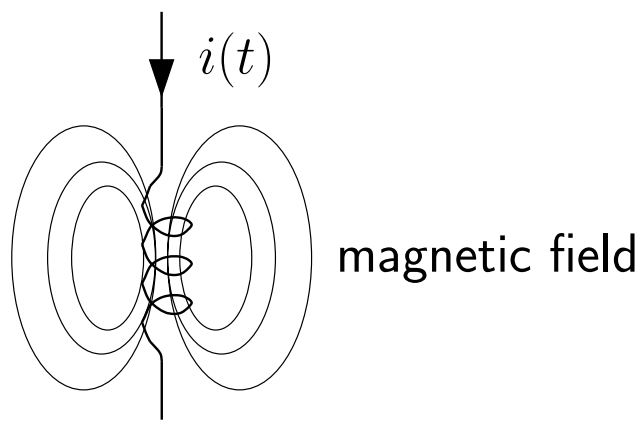
inductance of a wire in an IC	too small (usually ignored)
inductance of a pin on an IC	$10\mathrm{nH}$
inductance of an MRI magnet	$15\mathrm{mH}$

Inductor – contd.

- in steady state, $i.e.$, *steady* current flow, the inductor acts as a short circuit, since:

$$i(t) \text{ const.} \Rightarrow \frac{di}{dt} = 0 \Rightarrow v(t) = L\frac{di}{dt} = 0$$

- inductor *stores* energy in the form of magnetic field:



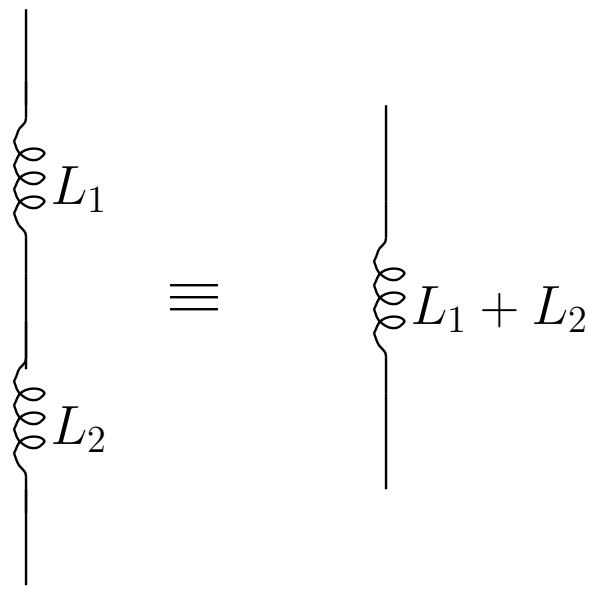
energy stored at t:

$$w(t) = \frac{1}{2}Li^2(t)$$

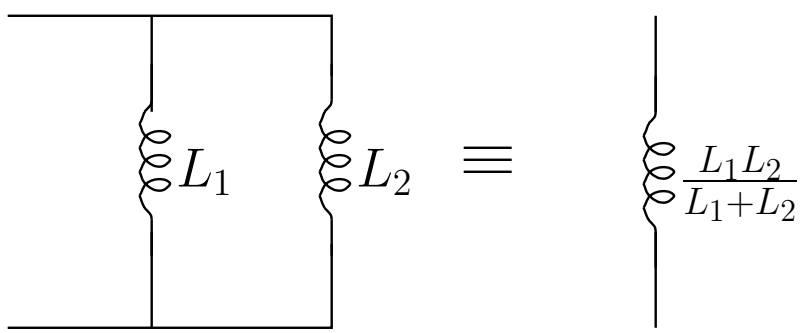
- inductor is a lossless element
- inductor is the *dual* of a capacitor (magnetic field versus electric field, current versus voltage)

Inductor – contd.

- inductors in series:



- inductors in parallel:



inductors in series and parallel are like resistors (dual of capacitors)

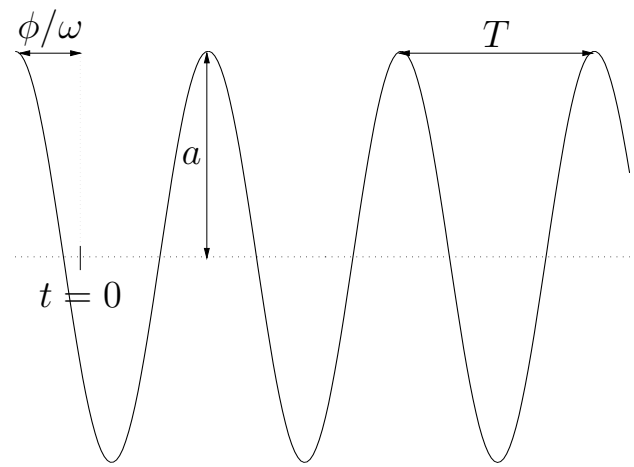
Lecture Notes 9
Sinusoidal Steady-State Circuit Analysis

- phasor representation of sinusoidal signals
- branch equations, KCL, and KVL via phasors
- hand analysis techniques
  - series/parallel reductions, voltage/current dividers
  - source transformation
- general SSS circuit equations
  - node voltage analysis
  - superposition
  - Thevenin and Norton
- small signal SSS circuit analysis

Sinusoidal Signals

a sinusoidal signal (or waveform, or function of t) u has the form

$$u(t) = a\cos(\omega t + \phi)$$



- $a \geq 0$ is the *amplitude*
- $\omega \geq 0$ is the *frequency* in radians/sec
- $f = \omega/(2\pi) = 1/T$ is the frequency in Hz
- ϕ is the *phase angle* or *phase shift* in radians – common conventions: $-\pi < \phi \leq \pi$, or $0 \leq \phi < 2\pi$

Sinusoidal steady state

consider a circuit consisting only of:

- capacitors and inductors,
- linear static elements, and
- sinusoidal sources with the same frequency ω

Fact: if the circuit is stable (EE 102), then in steady state all its branch voltages and currents are sinusoidal with the same frequency ω,

and the circuit is said to be in *sinusoidal steady-state* (SSS)

note: static (dc) circuit is a special case of a SSS circuit (where $\omega = 0$)

Sinusoidal steady state circuit analysis

we show that SSS response can be found by:

- representing sinusoidal signals as *phasors*, $i.e.$, complex numbers
- *transforming* the circuit from the *time domain*, where circuit equations are linear differential equations, to the *phasor domain*, where all circuit equations become linear algebraic equations involving complex numbers
- using the static circuit analysis techniques we learned to find the SSS response in the phasor domain
- transforming the phasor responses back to the time domain to get the branch voltages and currents

why study circuits in SSS ?

- some circuits and systems operate (approximately) in SSS, $e.g.$, electric power and communication systems
- using SSS analysis and superposition we can determine responses to more general (nonsinusoidal) sources, $e.g.$, periodic sources
- to find the *frequency response* of a circuit, which is key to designing *filters*

Phasor representation of sinusoids

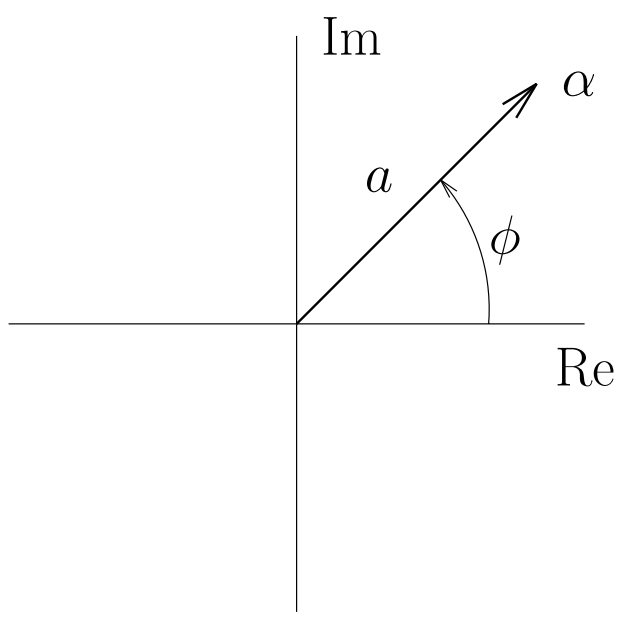
recall for θ real,

$$e^{j\theta} = \cos\theta + j\sin\theta, \text{ where } j = \sqrt{-1}$$

so we can express a sinusoid as

$$\begin{aligned} u(t) = a\cos(\omega t + \phi) &= a\,\mathrm{Re}(e^{j(\omega t+\phi)}) \\ &= \mathrm{Re}\left((ae^{j\phi})(e^{j\omega t})\right) \\ &= \mathrm{Re}(\alpha e^{j\omega t}) \end{aligned}$$

where $\alpha = ae^{j\phi}$ (which is complex) is called the *phasor* associated with the sinusoid u
phasor (complex number) $\alpha = x + jy$ can be represented by a vector:



where $a = |\alpha| = \sqrt{x^2 + y^2}$ is the *magnitude* and
$\phi = \angle\alpha = \arctan(y/x)$ is the *phase*

Phasor representation – contd.

phasor α encodes the magnitude and phase shift of the sinusoid
(its *frequency* must be separately specified)

there is a one-to-one correspondence between the set of phasors (complex numbers) and the set of sinusoidal signals with the same frequency

$$\mathrm{Re}(\alpha e^{j\omega t}) = |\alpha| \cos(\omega t + \angle\alpha) \leftrightarrow \alpha$$

this correspondence is *linear*, $i.e.$, it satisfies:

superposition: if α and β are the phasor representations of two sinusoidal signals, then $\alpha + \beta$ is the phasor representation of the sinusoidal signal $\mathrm{Re}((\alpha + \beta)e^{j\omega t})$

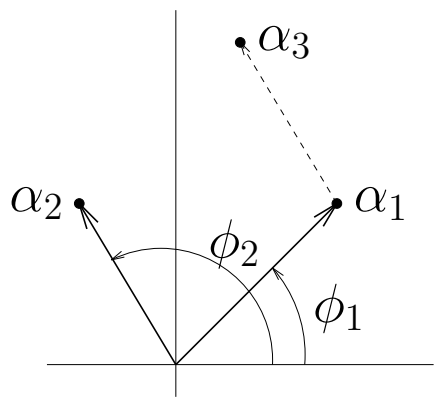
scaling: if γ is a real number then $\gamma\alpha$ is the phasor representation of the sinusoidal signal $\mathrm{Re}(\gamma\alpha e^{j\omega t})$

thus we can view the addition of two sinusoids as complex addition:

$$\alpha_1 + \alpha_2 = \alpha_3 \quad \text{or} \quad a_1 e^{j\phi_1} + a_2 e^{j\phi_2} = a_3 e^{j\phi_3}$$

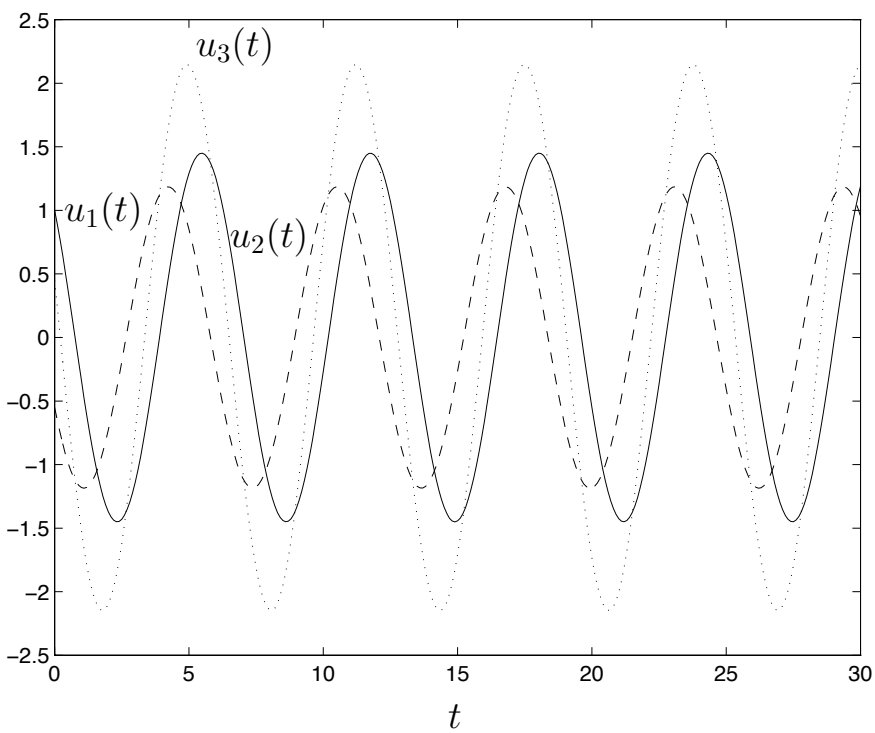
Phasor representation – contd.

or view addition of sinusoids as (vector) addition



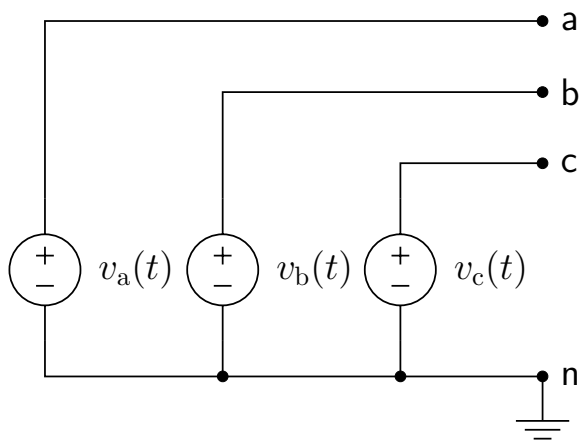
and the result is the sinusoid:

$$u_3(t) = a_1 \cos(\omega t + \phi_1) + a_2 \cos(\omega t + \phi_2)$$

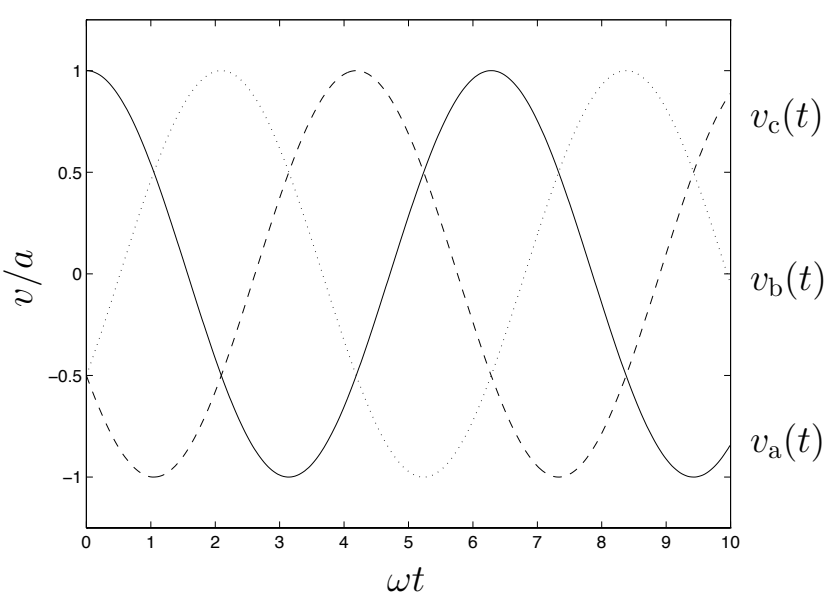


Example: Three-phase power

most power systems use a *three-phase* arrangement



$$
\begin{aligned}
v_a(t) &= a\cos(120\pi t) \\
v_b(t) &= a\cos(120\pi t - 120^\circ) \\
v_c(t) &= a\cos(120\pi t + 120^\circ)
\end{aligned}
$$

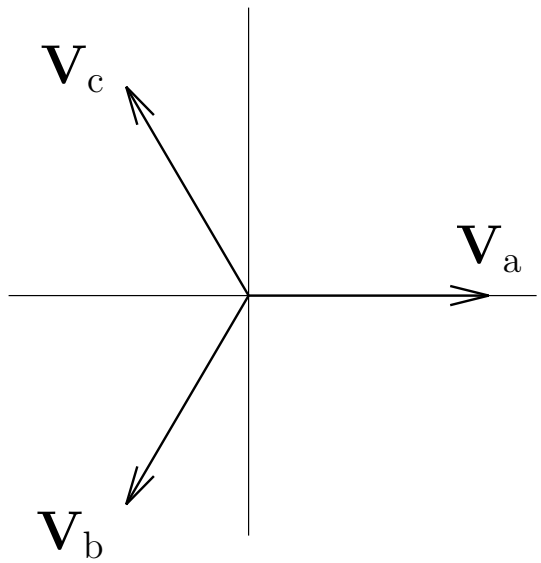


Three-phase power – contd.

in phasor representation we get

$$\mathbf{V}_{\mathrm{a}} = a, \quad \mathbf{V}_{\mathrm{b}} = ae^{-j2\pi/3}, \quad \mathbf{V}_{\mathrm{c}} = ae^{+j2\pi/3}$$

three-phase phasor diagram:



leg-to-leg voltage: what is the voltage from phase a to phase b? from b to c?

could use trigonometric identities, but let's use phasors:

$$\begin{aligned} \mathbf{V}_{\mathrm{a}} - \mathbf{V}_{\mathrm{b}} &= a - ae^{-j2\pi/3} \\ &= a(3/2 + j\sqrt{3}/2) \\ &= a\sqrt{3}e^{j30^\circ} \end{aligned}$$

thus $v_{\mathrm{a}}(t) - v_{\mathrm{b}}(t) = a\sqrt{3}\cos(120\pi + 30^\circ)$

Derivatives and Phasors

the time derivative of a sinusoidal signal is also sinusoidal with the same frequency:

$$\begin{aligned}\frac{d}{dt}a\cos(\omega t+\phi) &= -a\omega\sin(\omega t+\phi)\\ &= a\omega\cos(\omega t+\phi+90^\circ)\end{aligned}$$

thus differentiation yields amplitude scaling by ω, and 90° phase shift

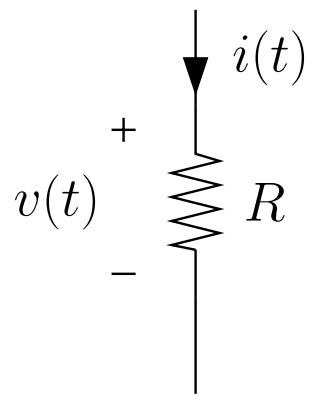
in phasor representation:

$$\frac{d}{dt}\operatorname{Re}(\alpha e^{j\omega t}) = \operatorname{Re}((\alpha j\omega)e^{j\omega t}) \leftrightarrow (j\omega)\alpha$$

$i.e.$, time derivative of sinusoidal signal corresponds to multiplication of associated phasor by $j\omega$

Branch relations via phasors

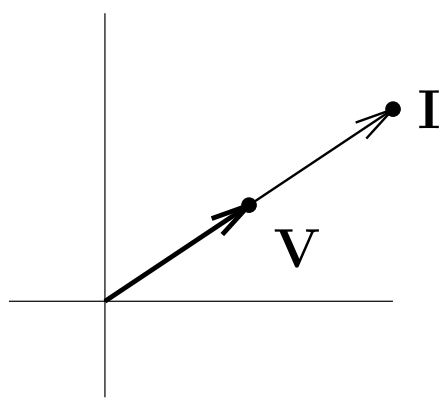
resistor: $v(t) = Ri(t)$



if $i(t) = a\cos(\omega t + \phi)$, then $v(t) = Ra\cos(\omega t + \phi)$

if $\mathbf{I} = ae^{j\phi}$ is phasor associated with i,
then phasor associated with v is $\mathbf{V} = \mathbf{I}R$

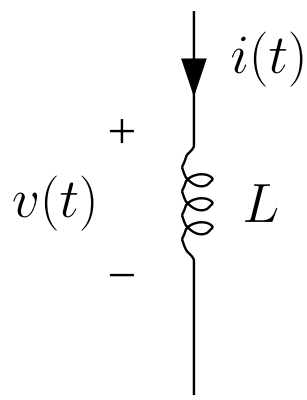
here $\mathbf{V}$ and $\mathbf{I}$ are complex numbers, R is real



$\angle\mathbf{V} = \angle\mathbf{I}$, *i.e.*, v and i are 'in phase'
(have same phase shift)

Branch relations via phasors – contd.

inductor: $v(t) = L\frac{di}{dt}$

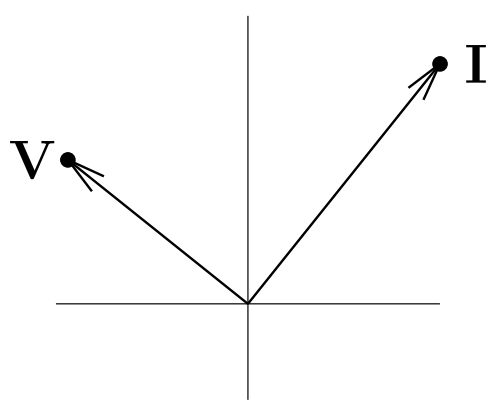


if $i(t) = a\cos(\omega t + \phi)$, then $v(t) = -La\omega\sin(\omega t + \phi)$

if $\mathbf{I}$ is current phasor, voltage phasor is $\mathbf{V} = (j\omega L)\mathbf{I}$

like a sort of Ohm's law for an *inductor*

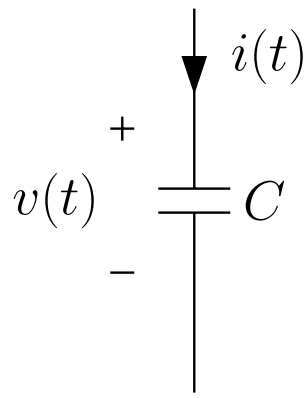
$j\omega L = \mathbf{V}/\mathbf{I}$ is called the *impedance* of the inductor (at frequency ω) and has units of Ω



$\angle\mathbf{V} = \angle\mathbf{I} + 90°$, *i.e.*, voltage *leads* current by $90°$

Branch relations via phasors – contd.

capacitor: $i(t) = C\frac{dv}{dt}$

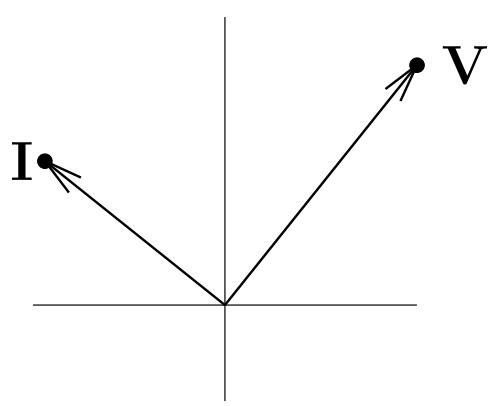


if $v(t) = a\cos(\omega t + \phi)$ then $i(t) = -Ca\omega\sin(\omega t + \phi)$

in terms of phasors:

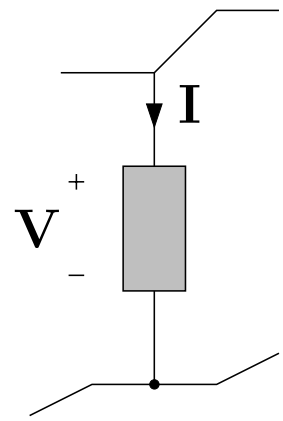
$$\mathbf{I} = j\omega C\mathbf{V}, \quad \text{or,} \quad \mathbf{V} = \left(\frac{1}{j\omega C}\right)\mathbf{I}$$

$i.e.$, impedance of capacitor is $1/(j\omega C)\ \Omega$



$\angle\mathbf{V} = \angle\mathbf{I} - 90°$, $i.e.$, voltage *lags* current by $90°$

Impedance



consider a two terminal circuit in SSS with the phasor relation

$$\mathbf{V} = Z\mathbf{I},$$

where Z is a complex number (that can depend on ω)

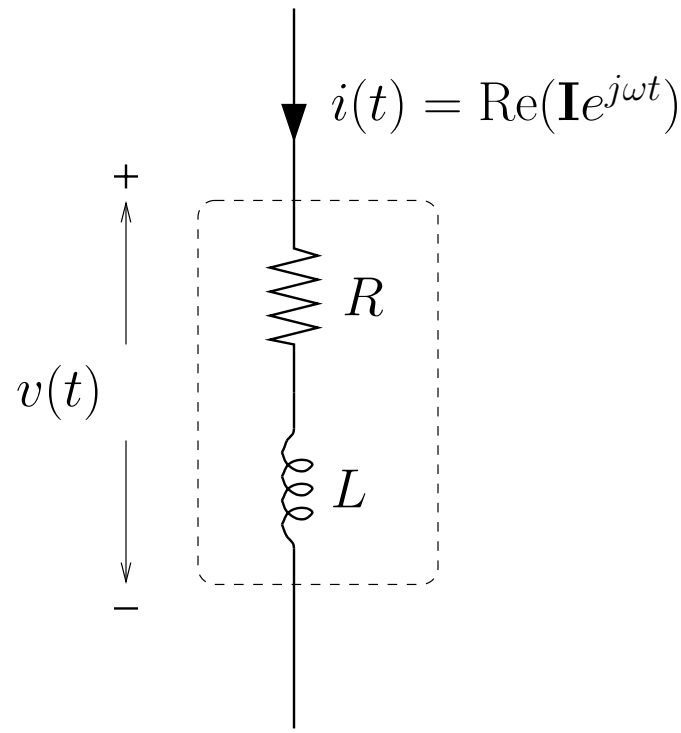
we say that Z is the *impedance* of the circuit (in Ω)

examples:

- resistor: $Z = R$ (which is real)
- inductor: $Z = j\omega L$ (imaginary)
- capacitor: $Z = 1/(j\omega C)$ (imaginary)

Impedance – contd.

another example:



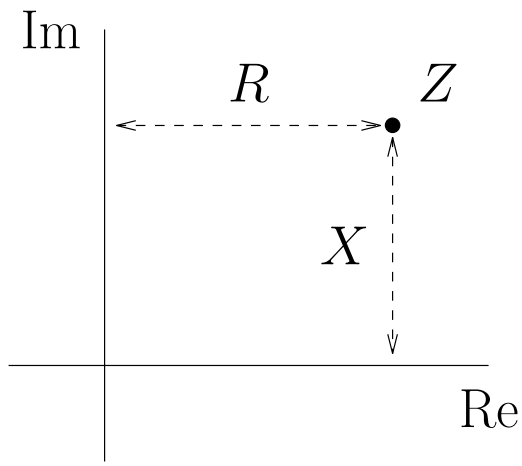
$$
\begin{aligned}
v(t) &= i(t)R + \frac{di}{dt}L \\
&= \mathrm{Re}(\mathbf{I}e^{j\omega t})R + \mathrm{Re}(\mathbf{I}j\omega e^{j\omega t})L \\
&= \mathrm{Re}((\mathbf{I}R + \mathbf{I}j\omega L)e^{j\omega t}) \\
&= \mathrm{Re}(\mathbf{V}e^{j\omega t})
\end{aligned}
$$

where $\mathbf{V} = (R + j\omega L)\mathbf{I}$

so impedance $Z = R + j\omega L$ is complex and depends on frequency

Real and reactive components

in general we can write impedance as $Z = R + jX$ (R, X are real)



- R is the *resistive component* of Z, and determines the 'in phase' voltage
- X is the *reactive component* of Z, and determines the '$\pm 90°$ out of phase' voltage
  - $X > 0$: inductive
  - $X < 0$: capacitive

Admittance

we can rewrite the impedance relation for an element as $\mathbf{I} = Y\mathbf{V}$

we call $Y = G + jB$ the *admittance* (units: $1/\Omega$)

- G is called the *conductance* of Y and determines the 'in phase' current
- B is the *susceptance* of Y and determines the '$\pm 90°$ out of phase' current
- can relate G and B to R and X by finding the reciprocal of Y:

$$Y = \frac{1}{Z} = \frac{R}{R^2 + X^2} - j\frac{X}{R^2 + X^2}$$

(not so simple as $G = 1/R \ldots$)

KCL and KVL via phasors

consider a circuit in SSS

KCL: suppose currents $i_1(t), \ldots, i_k(t)$ enter a node

KCL says that: $i_1(t) + \cdots + i_k(t) = 0$ (for all t)

in complex exponential representation, this becomes

$\mathrm{Re}((\mathbf{I}_1 + \cdots + \mathbf{I}_k)e^{j\omega t}) = 0$ (for all t)

where, $\mathbf{I}_1, \ldots, \mathbf{I}_k$ are the phasors corresponding to the currents $i_1, \ldots, i_k$

the only way this can hold for all t is if:

$$\mathbf{I}_1 + \cdots + \mathbf{I}_k = 0,$$

so KCL holds for phasors

KVL: suppose branch k points from node p into node q

KVL says that: $v_k(t) = e_p(t) - e_q(t)$ (for all t)

in complex exponential representation, this becomes
$\mathrm{Re}((\mathbf{V}_k - \mathbf{E}_p + \mathbf{E}_q)e^{j\omega t}) = 0$ (for all t)

which leads to a KVL for phasors:

$$\mathbf{V}_k = \mathbf{E}_p - \mathbf{E}_q$$

conclusion: for circuit in SSS, KCL and KVL apply, without change, to phasors

SSS circuit analysis via phasors

consider a circuit consisting only of:

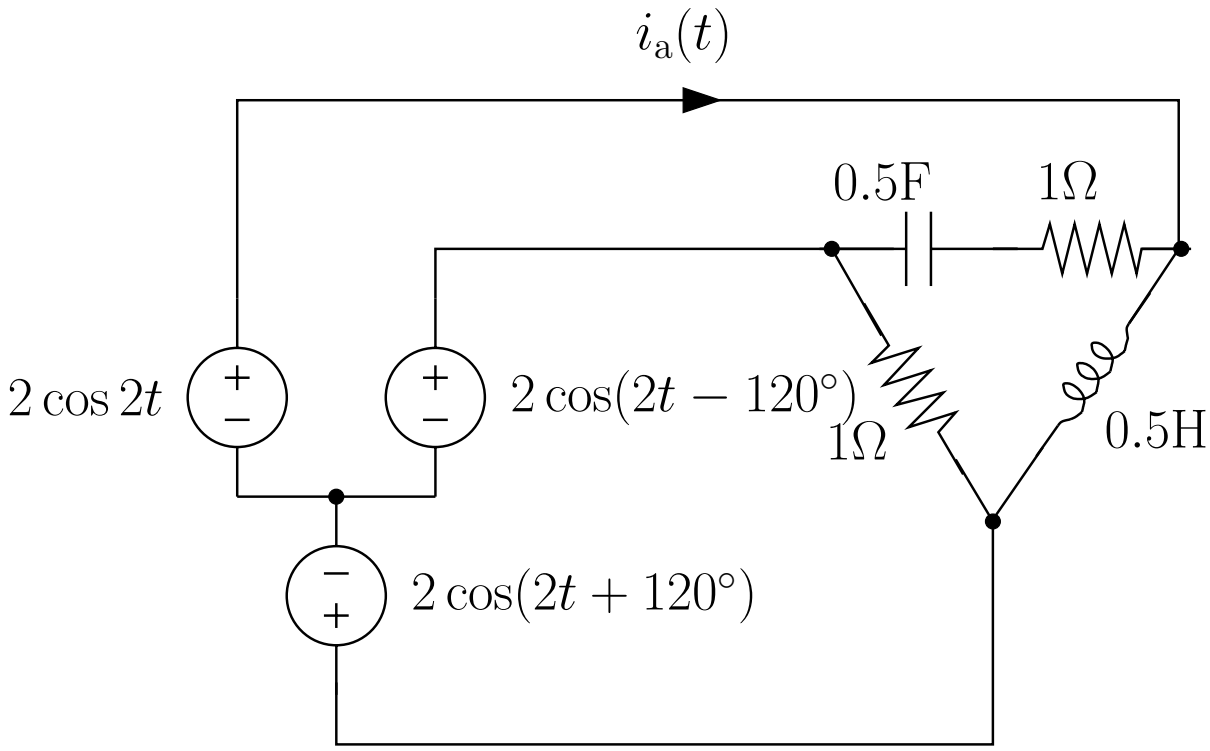
- inductors and capacitors,
- linear static elements, and
- sinusoidal sources (of same frequency)

to analyze its SSS response:

- we transfrom the branch relations to the phasor domain
- analyze the circuit to find the branch current and voltage phasors
- transform the phasors back to the time domain

since in the phasor domain all branch relations are linear algebraic equations and KCL and KVL hold the same way, we can use the analysis techniques for static circuits

Example (three phase circuit)

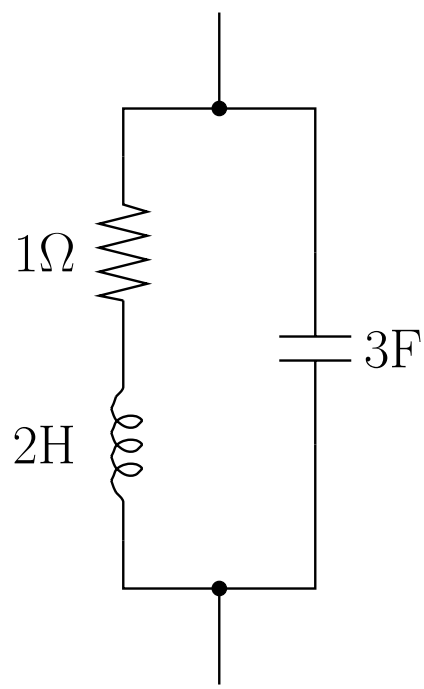


assuming the circuit is in SSS, find $i_a(t)$.

Series and parallel connections

formulas are the same as for the static case, substituting impedance for resistance and admittance for conductance, *e.g.*, two impedences Z_1 and Z_2 in series is equivalent to one impedence $Z = Z_1 + Z_2$, ...

Example: $\omega = 1$



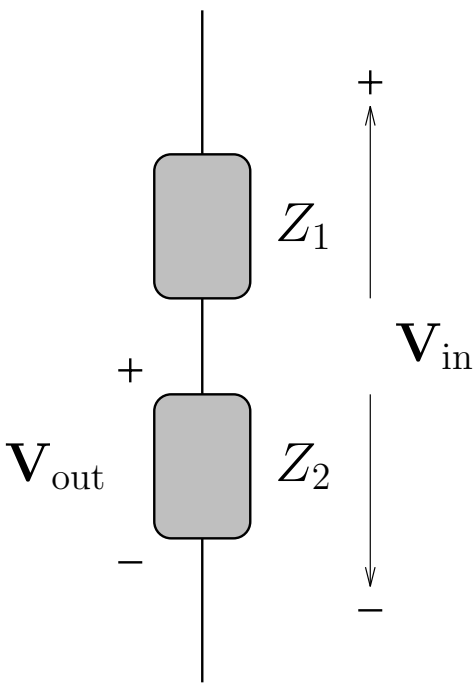
total impedance is:

$$Z = (1+2j)\|(\frac{1}{3j}) = \frac{(1+2j)(\frac{1}{3j})}{1+2j+\frac{1}{3j}} = \frac{1}{34} - j\frac{13}{34}$$

Voltage and current division

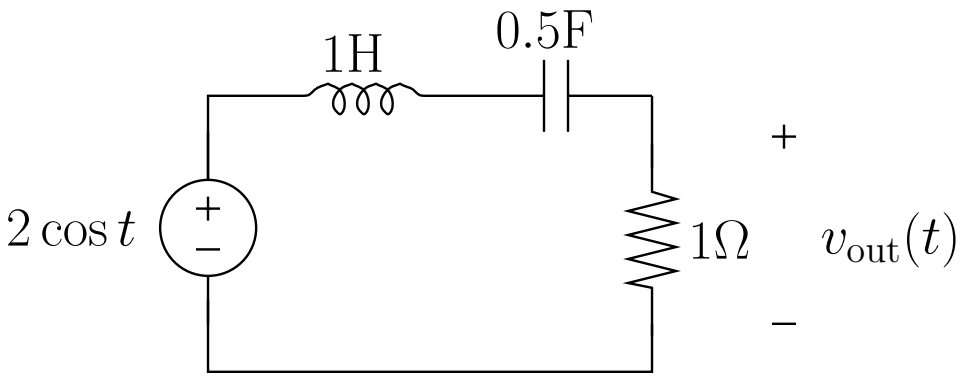
voltage and current divider rules are the same as static case, with impedance substituted for resistance and admittance substituted for conductance

so for two impedences in series



$$\mathbf{V}_{\text{out}} = \frac{Z_2}{Z_1 + Z_2}\mathbf{V}_{\text{in}}$$

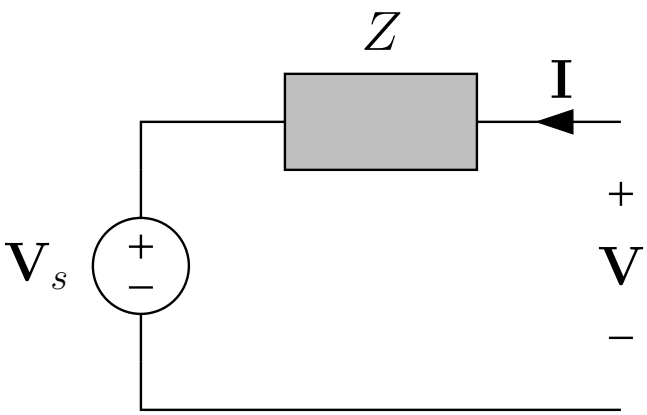
Example

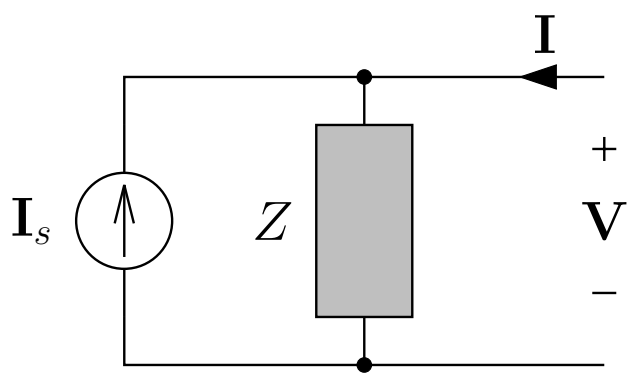


find $v_{\text{out}}(t)$ assuming the circuit is in SSS

Source transformation

same as static case . . .





circuits are equivalent if $\mathbf{I}_s = \mathbf{V}_s/Z$

each is characterized by $\mathbf{V} = \mathbf{V}_s + Z\mathbf{I}$

General SSS circuit equations

consider circuit consisting only of:

- inductors and capacitors
- linear static elements ($i.e.$, resistors, op-amps, dependent sources ...)
- independent sinusoidal sources with the same frequency ω

we assume SSS: all voltages and currents are sinusoidal

- $\mathbf{V}$ is vector of branch voltage *phasors*
- $\mathbf{I}$ is vector of branch current *phasors*
- $\mathbf{E}$ is vector of node voltage *phasors*
- A is reduced node incidence matrix

($\mathbf{V}$, $\mathbf{I}$, and $\mathbf{E}$ are *complex vectors*)

KCL and KVL are:

$$A\mathbf{I} = 0, \quad \mathbf{V} = A^T\mathbf{E}$$

General SSS circuit equations – contd.

branch relations look like, $e.g.$,

$\mathbf{V}_3 = 1 - j$	voltage source $v_3(t) = 1.41\cos(\omega t - 45°)$
$\mathbf{V}_{13} = 12\mathbf{I}_{13}$	12Ω resistor
$\mathbf{V}_7 = (j\omega 3)\mathbf{I}_7$	$3\mathrm{H}$ inductor
$\mathbf{I}_9 = (j\omega 10^{-8})\mathbf{V}_9$	$0.01\mu\mathrm{F}$ capacitor

these are (complex) linear equations in the $\mathbf{V}_i$'s and $\mathbf{I}_i$'s

can express branch relations in matrix form:

$$M\mathbf{I} + N\mathbf{V} = \mathbf{S}$$

where

- M and N can have *complex* entries
- $\mathbf{S}$ is vector of phasors of sources

SSS circuit equations are thus:

$$A\mathbf{I} = 0, \quad \mathbf{V} = A^T\mathbf{E}, \quad M\mathbf{I} + N\mathbf{V} = \mathbf{S}$$

General SSS circuit equations – contd.

SSS circuit equations in 'giant' matrix form:

$$\begin{bmatrix} A & 0 & 0 \\ 0 & I & -A^T \\ M & N & 0 \end{bmatrix} \begin{bmatrix} \mathbf{I} \\ \mathbf{V} \\ \mathbf{E} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ \mathbf{S} \end{bmatrix}$$

solution is:

$$\begin{bmatrix} \mathbf{I} \\ \mathbf{V} \\ \mathbf{E} \end{bmatrix} = \begin{bmatrix} A & 0 & 0 \\ 0 & I & -A^T \\ M & N & 0 \end{bmatrix}^{-1} \begin{bmatrix} 0 \\ 0 \\ \mathbf{S} \end{bmatrix}$$

exactly the same form as static case

differences:

- variables are phasors (complex numbers)
- branch relations use (complex) impedances/admittances
- branch relations change with frequency ω

Consequences

- node voltage method same with conductance replaced by admittance

- scaling and superposition hold exactly the same as in the static case

  if source vector $\mathbf{S}$ yields ($\mathbf{I}$, $\mathbf{V}$, and $\mathbf{E}$), then for any complex number α, $\alpha\mathbf{S}$ yields ($\alpha\mathbf{I}$, $\alpha\mathbf{V}$, and $\alpha\mathbf{E}$)

  if source vector $\mathbf{S}$ yields ($\mathbf{I}$, $\mathbf{V}$, and $\mathbf{E}$), and $\tilde{\mathbf{S}}$ yields ($\tilde{\mathbf{I}}$, $\tilde{\mathbf{V}}$, and $\tilde{\mathbf{E}}$), then $\mathbf{S}+\tilde{\mathbf{S}}$ yields ($\mathbf{I}+\tilde{\mathbf{I}}$, $\mathbf{V}+\tilde{\mathbf{V}}$, and $\mathbf{E}+\tilde{\mathbf{E}}$)

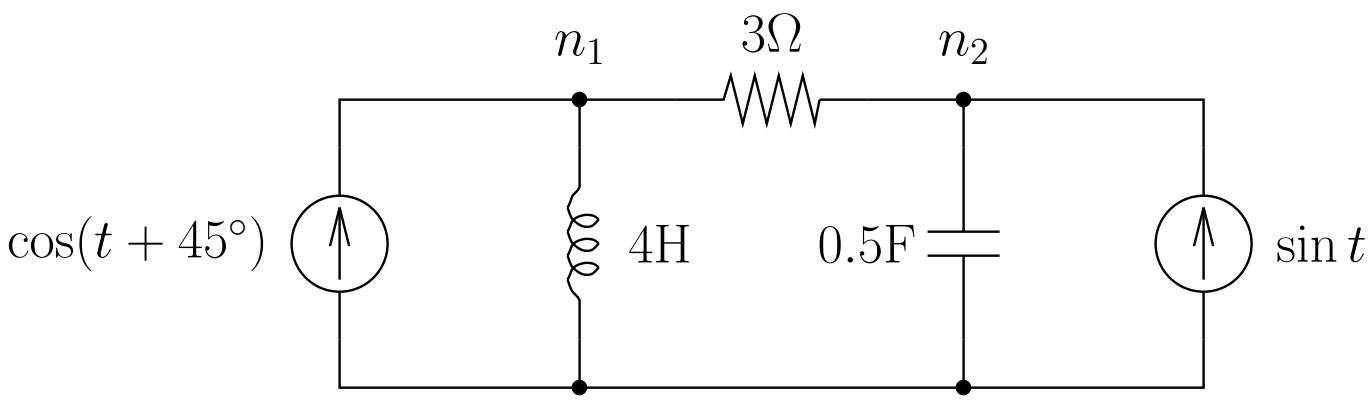
- Thevenin and Norton equivalents also hold

  any two terminal circuit in SSS is equivalent to voltage source $\mathbf{V_{th}}$ in series with impedence $\mathbf{Z_{th}}$

Node voltage method

same as static case, using admittance instead of conductance . . .

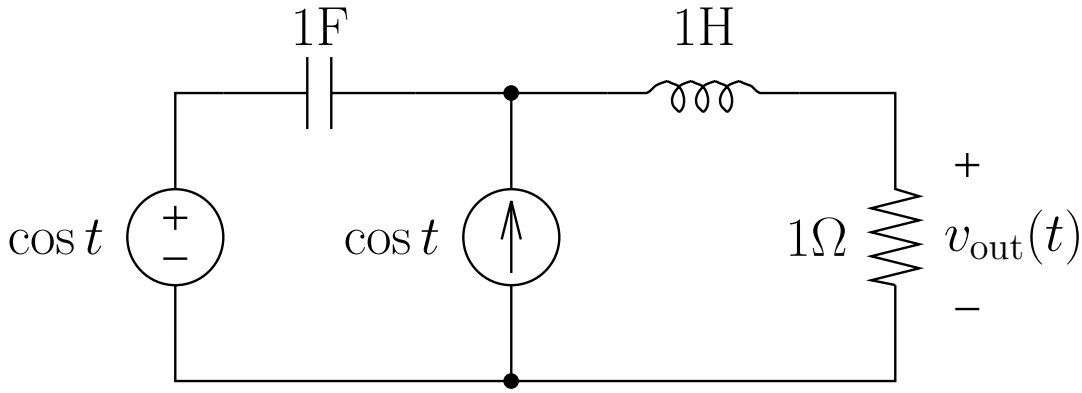
Example:



Superposition

same as static case . . .

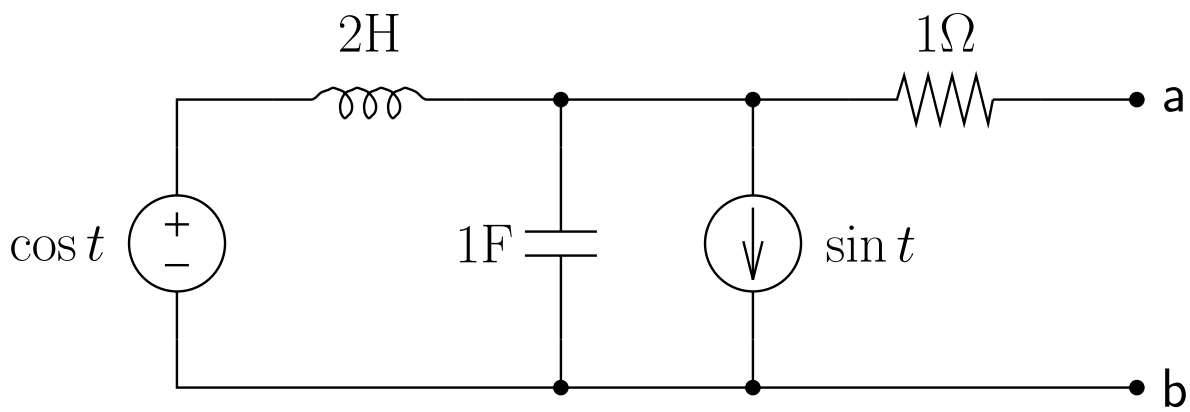
Example: what is $v_{\text{out}}(t)$?



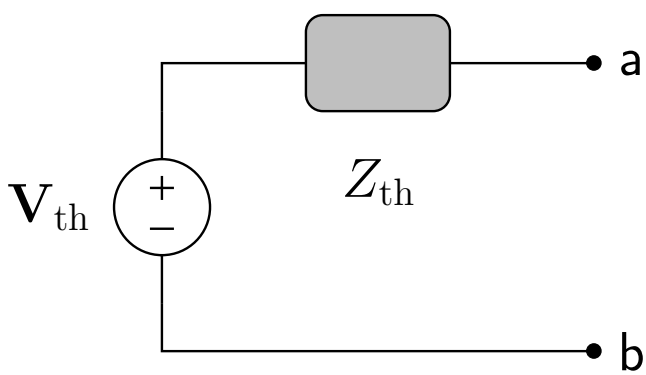
Thevenin and Norton equivalents

same as static case . . .

Example:



what is Thevenin equivalent, $i.e.$



Small signal SSS circuit

circuit in steady state consisting only of:

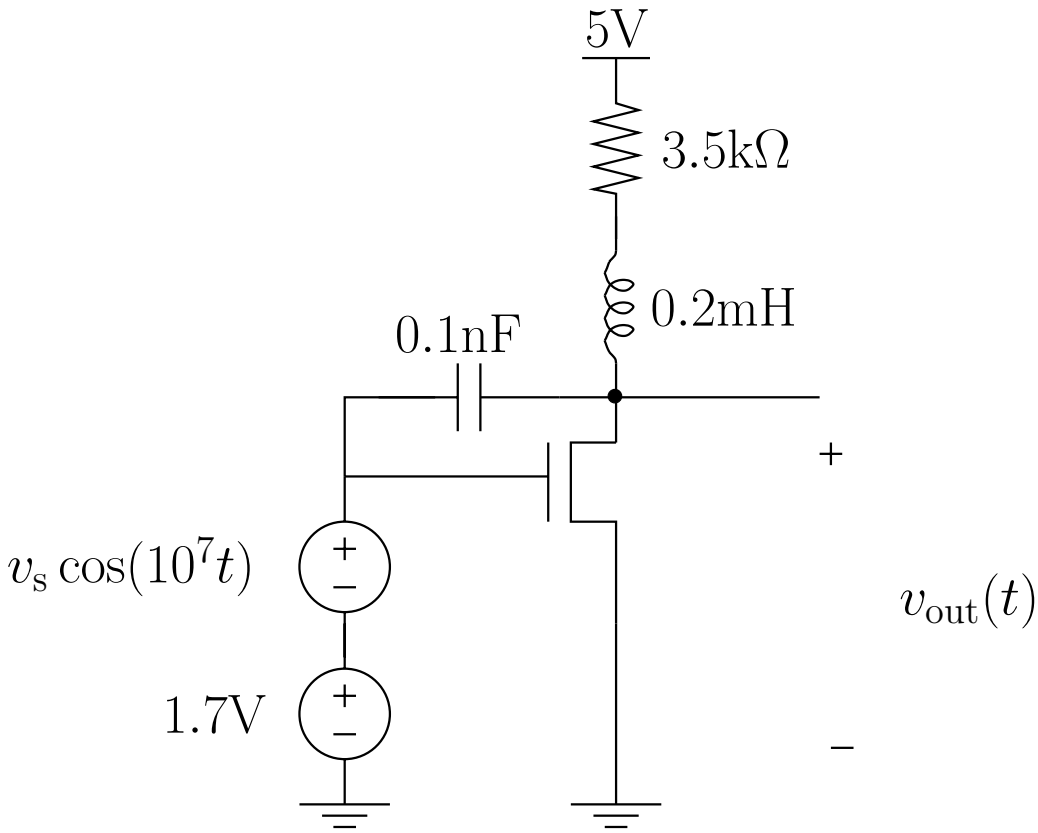
- capacitors and inductors,
- linear static elements,
- constant sources (bias voltages and currents),
- small signal sinusoidal source, and
- one or more nonlinear static elements

small signal analysis done as before:

- we perform dc analysis to find the bias conditions for each nonlinear element – here we turn off the small signal source and replace the capacitors by open circuits and the inductors by short circuits
- we construct the small signal model by turning off all dc sources and replacing the nonlinear elements by their small signal models around their bias points
- we use phasors to analyze the small signal circuit . . .

Example

the nMOS circuit in the figure is in steady state and $v_{\mathrm{s}} << 1.7\mathrm{V}$



assuming the first order dynamic MOS transistor model with $k = 2\mathrm{mA/V}^2$, $v_{\mathrm{t}} = 0.7\mathrm{V}$, $C_{\mathrm{g}} = 0.1\mathrm{nF}$, and $C_{\mathrm{d}} = 0.05\mathrm{nF}$, find the small signal $\mathbf{V}^s_{\mathrm{in}}$ - $\mathbf{V}^s_{\mathrm{out}}$ (phasor) relation

Lecture Notes 10
Power and Energy in SSS Circuits

- instantaneous, and average power
- maximum average power transfer
- power conservation
- stored energy

Instantaneous and average power in SSS

consider element in SSS with:

$$\begin{aligned} i(t) &= a\cos(\omega t + \phi), \text{ and} \\ v(t) &= b\cos(\omega t + \psi) \end{aligned}$$

where $a, b > 0$

assuming associated reference directions, the power flowing into the element is:

$$\begin{aligned} p(t) &= i(t)v(t) \\ &= ab\cos(\omega t + \phi)\cos(\omega t + \psi) \\ &= \frac{ab}{2}\cos(2\omega t + \phi + \psi) + \frac{ab}{2}\cos(\phi - \psi) \end{aligned}$$

last equality follows from the trigonometric equality:

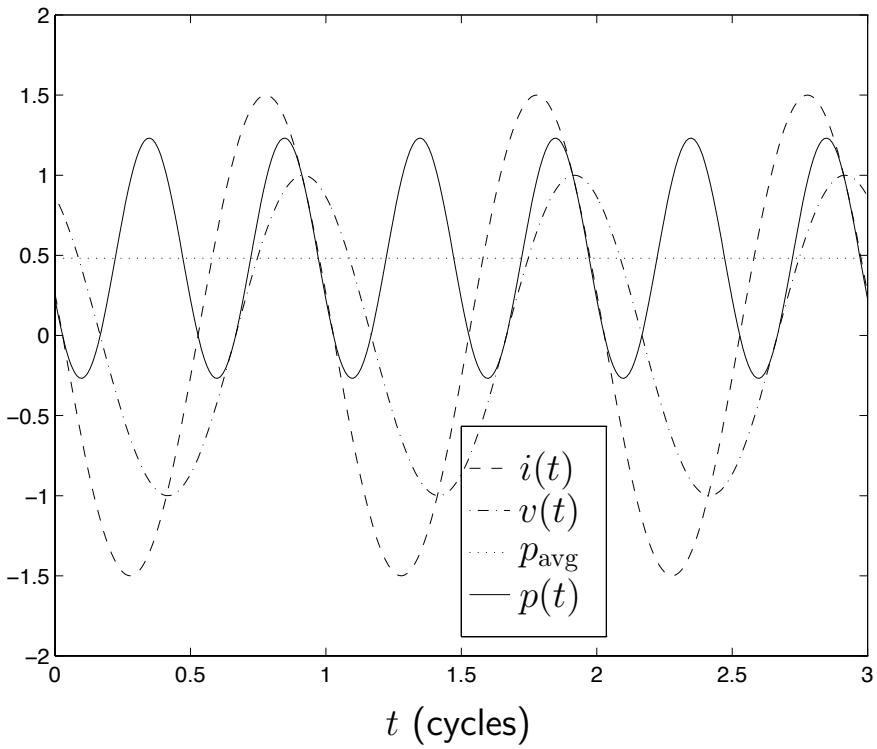
$$\cos\alpha\cos\beta = \frac{1}{2}\cos(\alpha + \beta) + \frac{1}{2}\cos(\alpha - \beta)$$

so the instantaneous power $p(t)$ is the sum of:

- a constant term, $\frac{ab}{2}\cos(\phi - \psi)$, and
- a sinusoidal term, $\frac{ab}{2}\cos(2\omega t + \phi + \psi)$ (at frequency 2ω)

Power in SSS – contd.

Example: $(b = 1,\ \psi = 30°,\ a = 1.5,\ \phi = 80°)$



- $p(t)$ is sometimes positive, sometimes negative
- the constant term is the average power (over one cycle)

$$\frac{\omega}{2\pi}\int_0^{2\pi/\omega} p(t)\ dt = p_{\text{avg}} = \frac{ab\cos(\phi-\psi)}{2}$$

- $\cos(\phi - \psi)$ is called *power factor* (pf)
- amplitude of sinusoidal term is $ab/2$ (always $\geq p_{\text{avg}}$)

Power in SSS – contd.

- max power is $p_{\max} = ab\dfrac{\cos(\phi - \psi) + 1}{2} = p_{\text{avg}} + ab/2$
- min power is $p_{\min} = ab\dfrac{\cos(\phi - \psi) - 1}{2} = p_{\text{avg}} - ab/2$

Extreme cases:

- v and i **in phase**, $i.e.$, $\phi = \psi$, $e.g.$, a resistor:
  - $p(t) \geq 0$ for all t
  - $p_{\max} = ab = 2p_{\text{avg}}$, $p_{\min} = 0$
  - power factor is 1
- v and i **opposite phases**, $i.e.$, $\phi = \psi + 180°$, $e.g.$, sinusoidal source connected to a resistive load:
  - $p(t) \leq 0$ for all t
  - $p_{\min} = -ab = 2p_{\text{avg}}$, $p_{\max} = 0$
  - power factor is -1
- v and i **in quadrature**, $i.e.$, $\phi = \psi \pm 90°$, $e.g.$, capacitor or inductor:
  - $p_{\text{avg}} = 0$
  - $p_{\min} = -ab/2$, $p_{\max} = ab/2$
  - power factor is 0

Average power and phasors

again consider an element with:

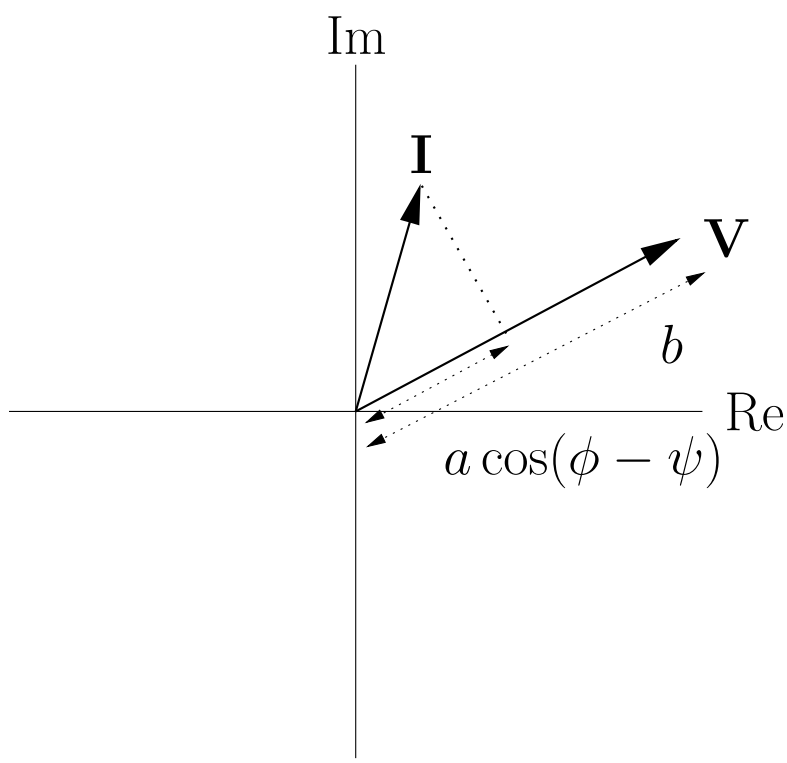
$$i(t) = a\cos(\omega t + \phi), \text{ and } v(t) = b\cos(\omega t + \psi)$$

the average power in terms of phasors:

$$\begin{aligned} p_{\text{avg}} &= \frac{ab}{2}\cos(\phi - \psi) \\ &= \frac{ab}{2}(\cos(\phi)\cos(\psi) + \sin(\phi)\sin(\psi)) \\ &= \frac{1}{2}\operatorname{Re}(\overline{\mathbf{V}}\mathbf{I}) = \frac{1}{2}\operatorname{Re}(\overline{\mathbf{I}}\mathbf{V}) \end{aligned}$$

where $\overline{\mathbf{V}}$ is the *complex conjugate* of $\mathbf{V}$

geometric interpretation: $\operatorname{Re}(\overline{\mathbf{V}}\mathbf{I})$ is *inner* or *dot product* of $\mathbf{V}$ and $\mathbf{I}$



Average power and impedance

suppose the element is an impedance, $i.e.$,

$$\mathbf{V} = Z\mathbf{I}$$

then the average power dissipated is:

$$p_{\text{avg}} = \text{Re}(\bar{\mathbf{I}}\mathbf{V})/2 = \text{Re}(\bar{\mathbf{I}}\mathbf{I}Z)/2 = |\mathbf{I}|^2 \,\text{Re}(Z)/2$$

thus for a given current, the average power dissipated depends only on the real part or *resistive component* of the impedance

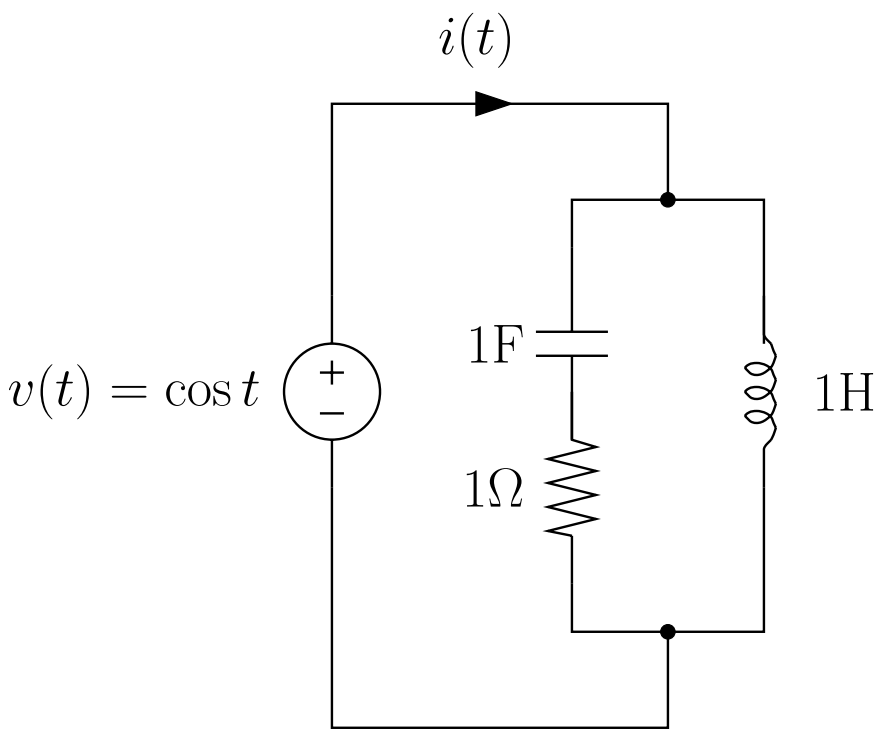
we can also express average power as:

$$p_{\text{avg}} = |\mathbf{V}|^2 \,\text{Re}(Y)/2$$

special case: *purely reactive* elements ($i.e.$, imaginary impedance) dissipate no power on average

- equal energy flows in and out in each cycle (every (π/ω) sec)
- $\mathbf{V}$ and $\mathbf{I}$ are othogonal

Example



- what is avg pwr supplied by source?
- what is max pwr supplied by source?
- what is avg power dissipated in resistor?
- what is max power dissipated in resistor?

Conservation of average power

consider general circuit with capacitors, inductors, linear static elements , and sinusoidal sources in SSS

we know that instantaneous power is conserved (since KCL and KVL always hold)

let $\mathbf{V}$, $\mathbf{I}$, $\mathbf{E}$ be branch voltage, branch current, and node voltage vectors respectively (in phasor representation)

avg pwr dissipated in branch k is $p_k^{\text{avg}} = \text{Re}(\overline{\mathbf{I}}_k \mathbf{V}_k)/2$

intuition suggests

$$p_1^{\text{avg}} + \cdots + p_b^{\text{avg}} = 0$$

$i.e.$, total avg pwr supplied equals total avg pwr absorbed

Conservation of average power – contd.

to verify this note that

$$p_1^{\text{avg}} + \cdots + p_b^{\text{avg}} = \frac{1}{2}\,\text{Re}(\overline{\mathbf{I}}^T\mathbf{V})$$

now KVL and KCL are

$$\mathbf{V} = A^T\mathbf{E}, \quad A\mathbf{I} = 0$$

so

$$\overline{\mathbf{I}}^T\mathbf{V} = \overline{\mathbf{I}}^T A^T\mathbf{E} = (A\overline{\mathbf{I}})^T\mathbf{E} = 0$$

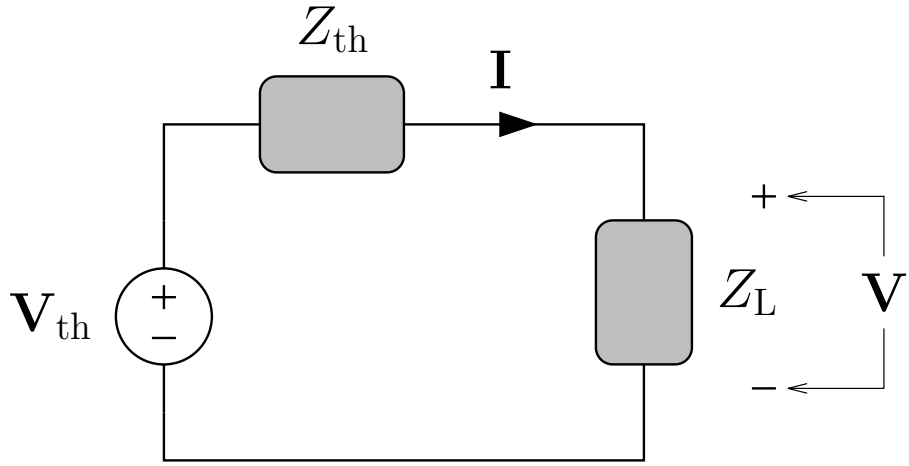
(since $A\overline{\mathbf{I}} = \overline{A\mathbf{I}} = 0$)

therefore

$$\text{Re}(\overline{\mathbf{I}}^T\mathbf{V}) = 0,$$

which establishes conservation of average power

Maximum average power transfer



$$\mathbf{V} = \frac{Z_{\rm L}}{Z_{\rm L} + Z_{\rm th}}\mathbf{V}_{\rm th}, \quad \mathbf{I} = \frac{\mathbf{V}_{\rm th}}{Z_{\rm L} + Z_{\rm th}}$$

so average power dissipated in load impedance $Z_{\rm L}$ is

$$\begin{aligned} p_{\rm avg} &= \frac{1}{2}\,{\rm Re}(\bar{\mathbf{I}}\mathbf{V}) \\ &= \frac{1}{2}\,{\rm Re}(|\mathbf{V}_{\rm th}|^2 \frac{Z_{\rm L}}{|Z_{\rm L} + Z_{\rm th}|^2}) \\ &= \frac{|\mathbf{V}_{\rm th}|^2}{2|Z_{\rm L} + Z_{\rm th}|^2}\,{\rm Re}(Z_{\rm L}) \\ &= \frac{1}{2}|\mathbf{V}_{\rm th}|^2 \frac{R_{\rm L}}{(R_{\rm L} + R_{\rm th})^2 + (X_{\rm L} + X_{\rm th})^2} \end{aligned}$$

where $Z_{\rm L} = R_{\rm L} + jX_{\rm L}$, $Z_{\rm th} = R_{\rm th} + jX_{\rm th}$

- $R_{\rm th}$, $X_{\rm th}$ are fixed
- $R_{\rm L}$, $X_{\rm L}$ are to be chosen to maximize $p_{\rm avg}$

Maximum power transfer – contd.

best choice for X_{L} is $X_{\mathrm{L}} = -X_{\mathrm{th}}$
(since $X_{\mathrm{L}} + X_{\mathrm{th}} \neq 0$ increases the denominator)

with $X_{\mathrm{L}} + X_{\mathrm{th}} = 0$, problem reduces to maximizing half the static pwr, so optimum load resistance is: $R_{\mathrm{L}} = R_{\mathrm{th}}$

and the maximum average power delivered is:

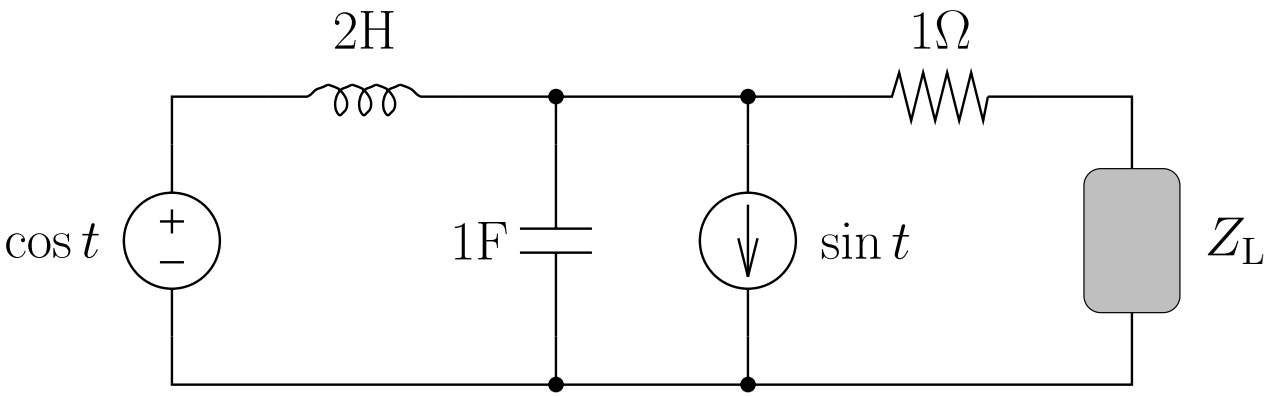
$$p_{\mathrm{avg}}^{\mathrm{max}} = \frac{|\mathbf{V}_{\mathrm{th}}|^2}{8R_{\mathrm{th}}}$$

conclusion: optimal load impedance is:

$$X_{\mathrm{L}} = -X_{\mathrm{th}}, \quad R_{\mathrm{L}} = R_{\mathrm{th}}, \quad i.e., \; Z_{\mathrm{L}} = \overline{Z}_{\mathrm{th}}$$

- when $Z_{\mathrm{L}} = \overline{Z}_{\mathrm{th}}$ we say load and source impedances are *matched* (or *conjugate matched*)
- when matched, load reactance cancels source reactance
- with matched load, source current $\mathbf{I}$ and voltage $\mathbf{V}_{\mathrm{th}}$ are in phase since $Z_{\mathrm{th}} + Z_{\mathrm{L}} = 2R_{\mathrm{th}}$

Example



- find Z_L that maximizes power transfer
- realize Z_L as a circuit with Rs, Ls, Cs

Stored energy

consider inductor with $i(t) = a\cos(\omega t + \phi)$

stored energy is:

$$E(t) = \frac{1}{2}Li(t)^2 = \frac{a^2 L}{4}\left(1 + \cos(2\omega t + 2\phi)\right)$$

- $E_{\text{avg}} = a^2 L/4 = |\mathbf{I}|^2 L/4$
  (*cf.* static case: $E = i^2 L/2$)
- $E_{\text{max}} = |\mathbf{I}|^2 L/2 = 2E_{\text{avg}}$

for capacitor with $v(t) = b\cos(\omega t + \psi)$, stored energy is:

$$E(t) = \frac{1}{2}Cv(t)^2 = \frac{b^2 C}{4}\left(1 + \cos(2\omega t + 2\psi)\right)$$

- $E_{\text{avg}} = b^2 C/4 = |\mathbf{V}|^2 C/4$
  (*cf.* static case: $E = v^2 C/2$)
- $E_{\text{max}} = |\mathbf{V}|^2 C/2 = 2E_{\text{avg}}$

twice each cycle, energy E_{max} is stored and then removed

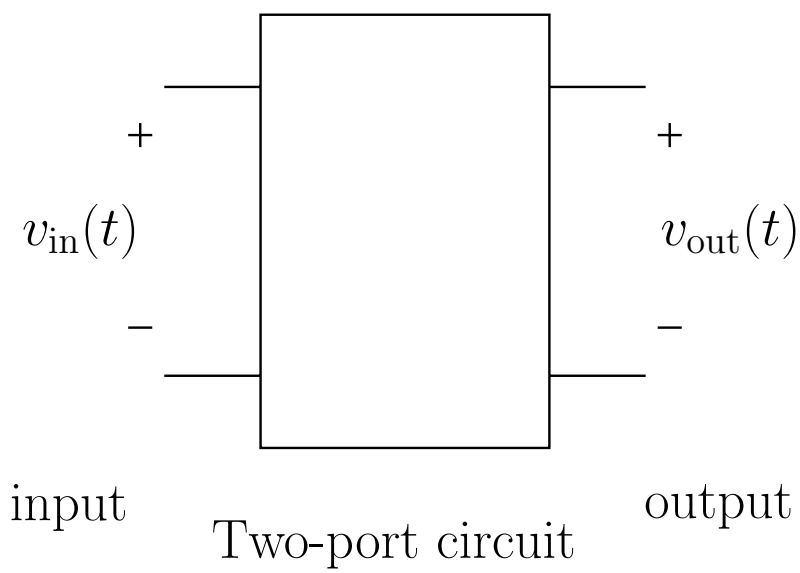
Lecture Notes 11
Introduction to Frequency Response

- frequency response
- Bode plots
- examples:
  - RC circuit
  - RLC circuit

Frequency response

consider a *two-port* circuit, $e.g.$, an amplifier, consisting only of:

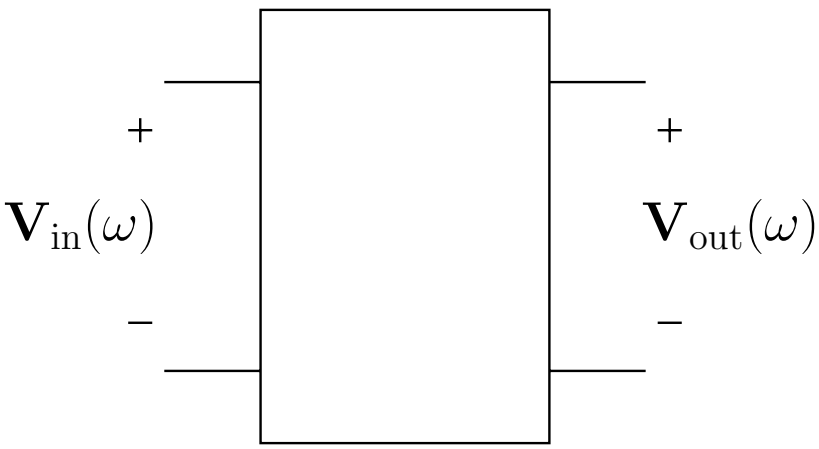
- linear static elements,
- capacitors and inductors, and
- two-terminal input and output ports



if we apply a sinusoidal voltage source to the input (port), then in steady state (assuming the circuit is stable), the output voltage is also sinusoidal with the same frequency

Frequency response – contd.

so in phasor domain:



the *transfer function* of the circuit is defined as:

$$H(\omega) \triangleq \frac{\mathbf{V}_{\text{out}}(\omega)}{\mathbf{V}_{\text{in}}(\omega)}$$

$H(\omega)$ is in general complex and a function of ω

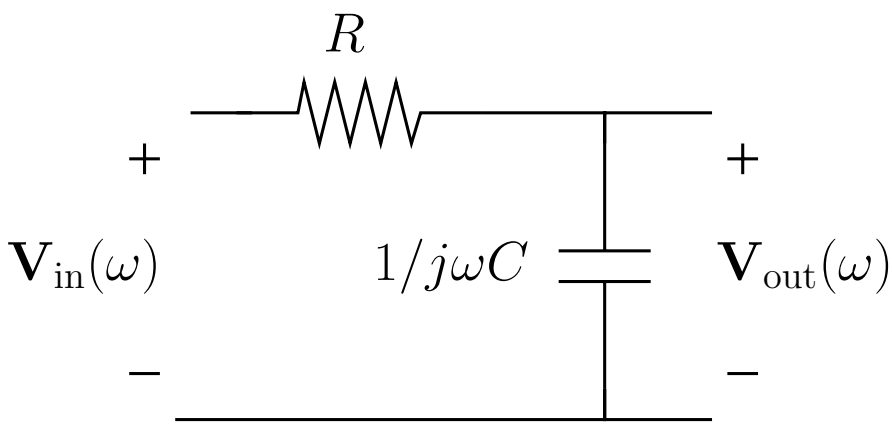
we can express it in terms of its *magnitude* $|H(\omega)|$ and phase $\angle H(\omega)$ as:

$$H(\omega) = |H(\omega)| e^{j\angle H(\omega)}$$

$|H(\omega)|$ and $\angle H(\omega)$ (as functions of ω) define the *frequency response* of the circuit

Frequency response of RC circuit

consider the two-port RC circuit:



the transfer function is:

$$H(\omega) = \frac{1}{1 + j\omega RC}$$

define $\omega_o = 1/RC$ (called the *cutoff frequency* of the circuit)

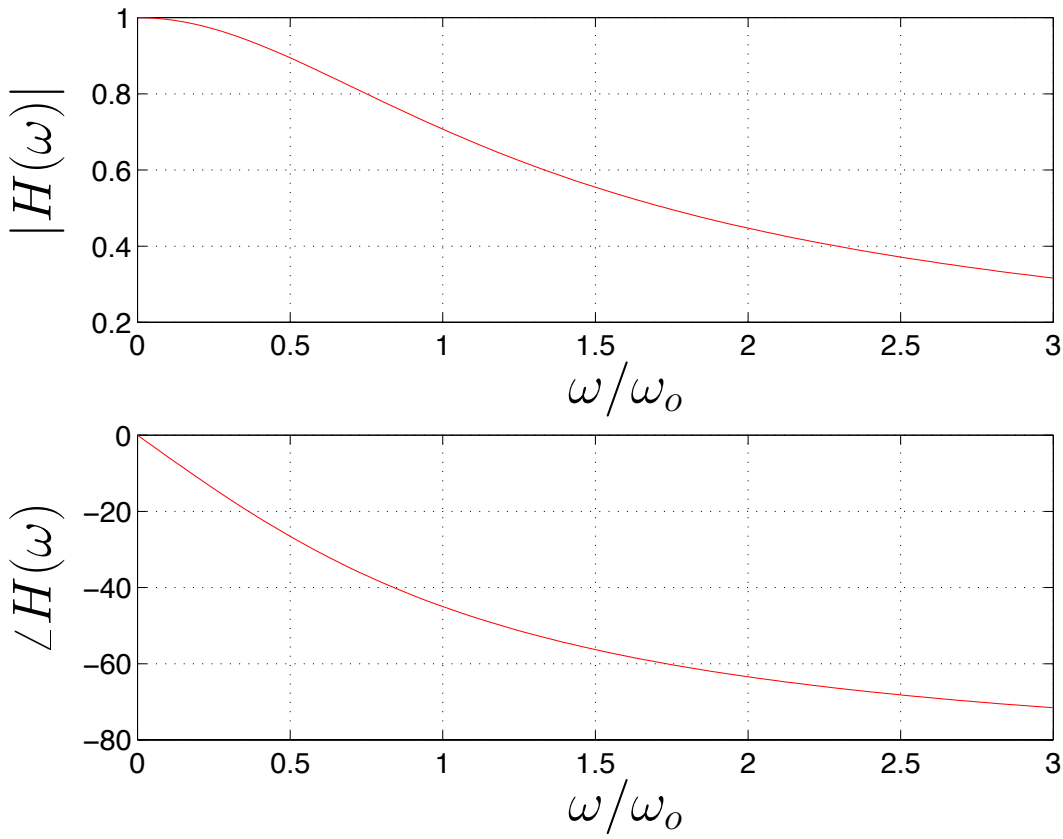
in terms of ω_o, the transfer function is:

$$H(\omega) = \frac{1}{1 + j(\omega/\omega_o)}$$

and the ferquency response is defined by its

$$\begin{aligned} \text{amplitude: } |H(\omega)| &= \frac{1}{\sqrt{1 + (\omega/\omega_o)^2}}, \text{ and} \\ \text{phase: } \angle H(\omega) &= \arctan(-(\omega/\omega_o)) \end{aligned}$$

Freq. response of RC circuit – contd.



so the circuit acts as a *low pass filter* – it *attenuates* the input signal more as frequency increases

the output signal *lags* the input signal more as frequency increases

Why study frequency response?

real world signals, *e.g.*, speech, music, video, radio . . . , can (by the Fourier Transform) be represented as the sum (integral) of sinusoids within some frequency *band*

examples:

speech	20Hz – 5kHz
music	20Hz – 20kHz
phone	300Hz – 3.4kHz
AM radio signal	0 – 5kHz (around carrier frequency)
TV VHF signal	0–6MHz (around carrier frequency)

so we can speak of the *frequency component* of a signal

these signals are often amplified or filtered using two-port circuits that can be modeled using linear static elements, Cs, and Ls

in steady state, frequency response and superposition can be used to analyze such circuits:

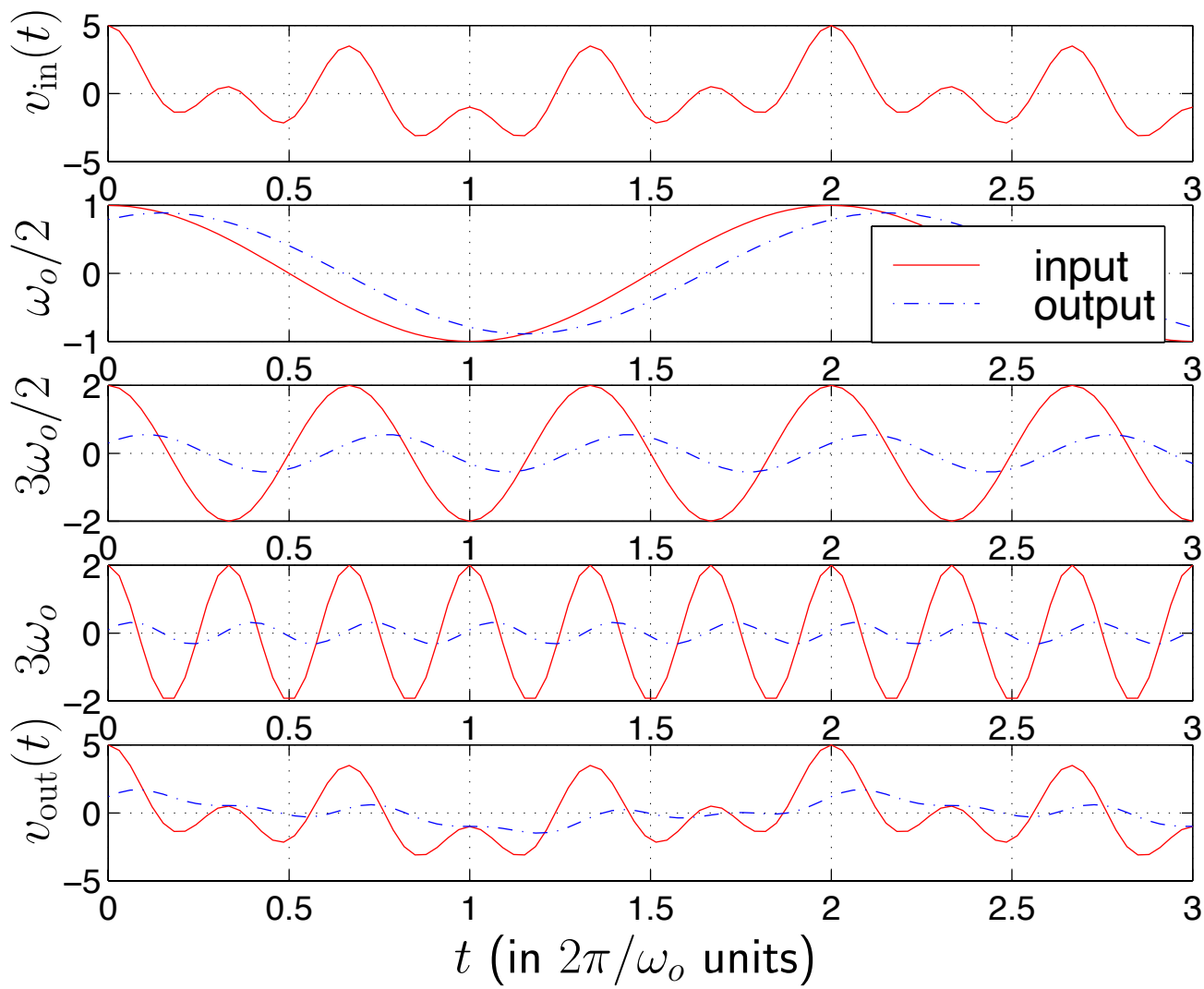
- use frequency response to find the amplitude and phase of each output frequency component
- add the output frequency components (in the same domain) to find the output signal

Example

let the input to an RC circuit be:

$$v_{\text{in}}(t) = \cos\left(\frac{1}{2}\omega_o t\right) + 2\cos\left(\frac{3}{2}\omega_o t\right) + 2\cos\left(3\omega_o t\right)\ \text{V}$$

find $v_{\text{out}}(t)$, assuming the circuit is in steady state



Bode plots

it is customary to use logarithmic instead of linear scale to plot frequency response

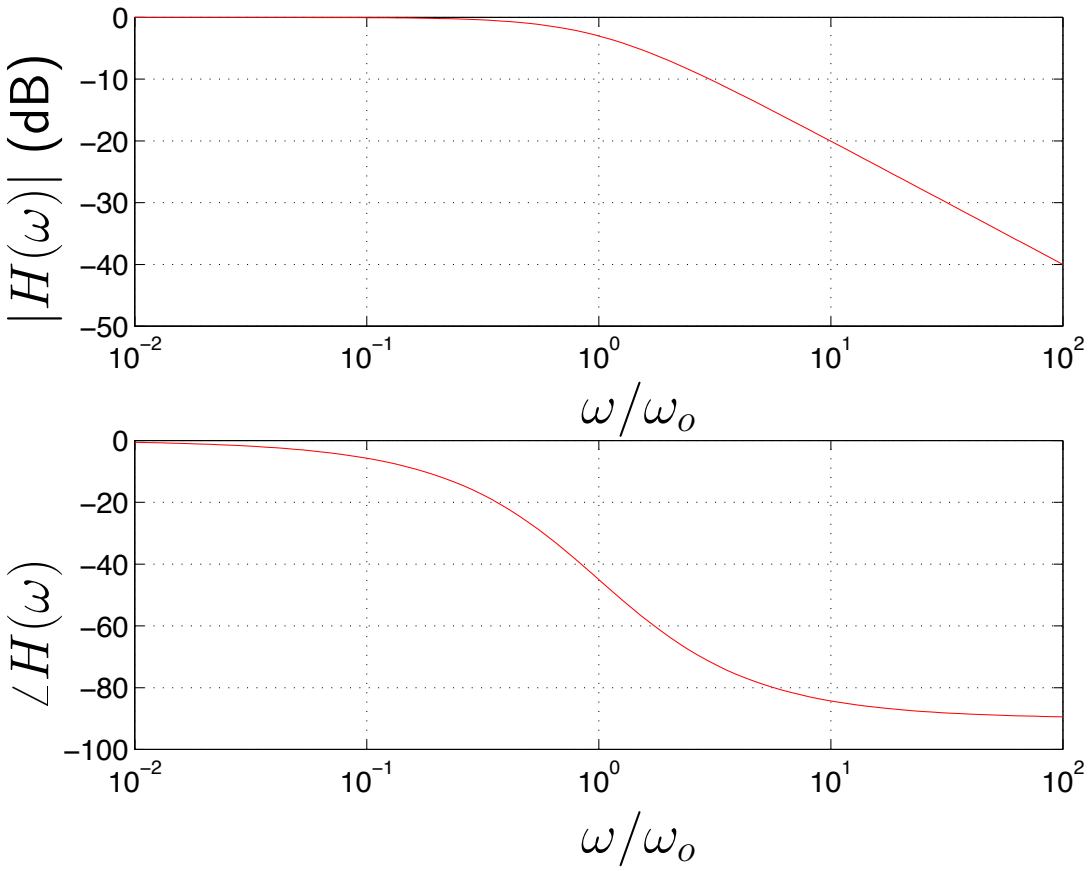
in Bode plot, the magnitude part of the frequency response is a plot of $20 \log_{10} |H(\omega)|$ in decibels (dB) vs. $\log_{10} \omega$

common dB values:

$\lvert H(\omega)\rvert$	$20 \log_{10} \lvert H(\omega)\rvert$
100	40 dB
10	20 dB
3.2	10 dB
2	6 dB
$\sqrt{2}$	3 dB
1	0 dB
0.1	-20 dB
0.01	-40 dB

phase is plotted using a linear scale (in degrees) also vs. $\log_{10} \omega$

Bode plot for RC circuit

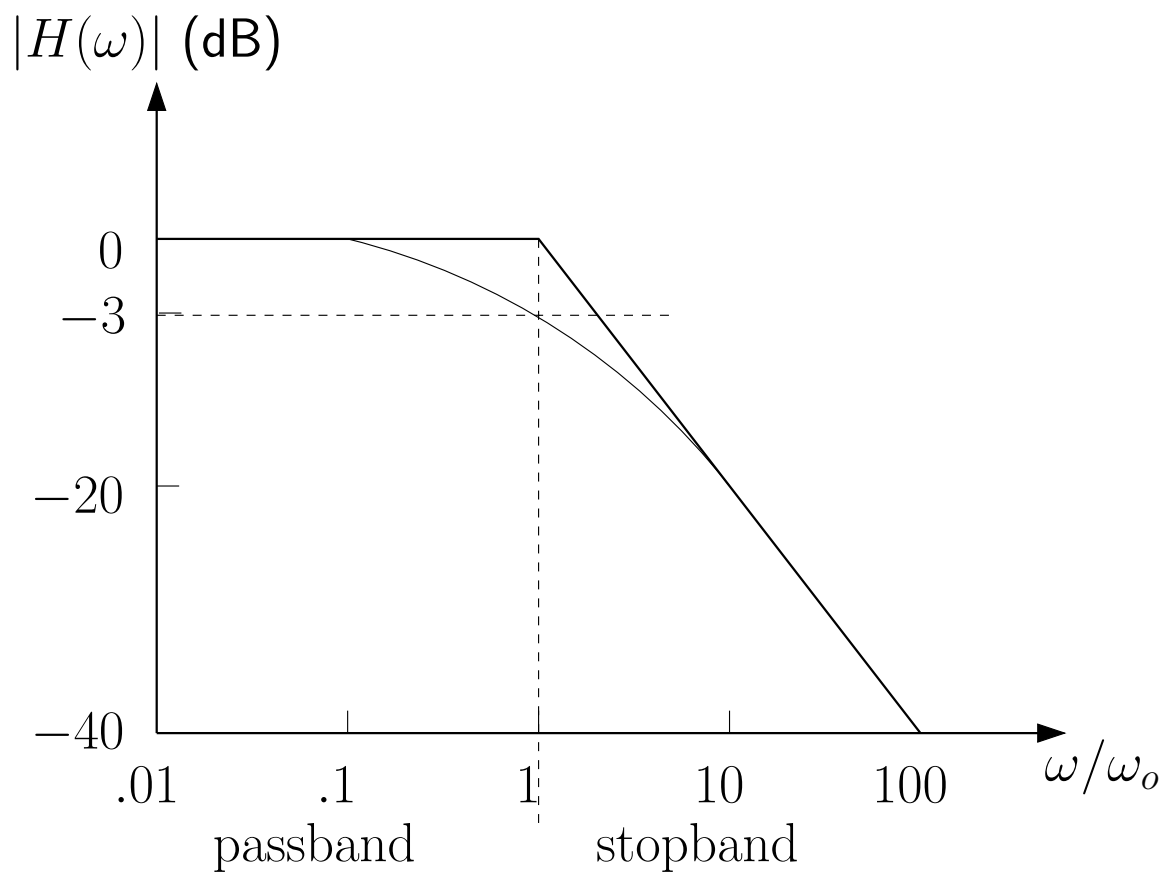


- at the cutoff freuqency ω_o, $|H(\omega)| = 1/\sqrt{2}$, $i.e.$, 3bB below its maximum value (of 1)
- for $\omega >> \omega_o$, $|H(\omega)| \approx (\omega_o/\omega)$,

  so $|H(\omega)|$ in dB vs. $\log_{10}(\omega/\omega_o)$ is roughly a straight line with slope -20dB per decade ($i.e.$, drop of 20dB for 10X increase in ω/ω_o)

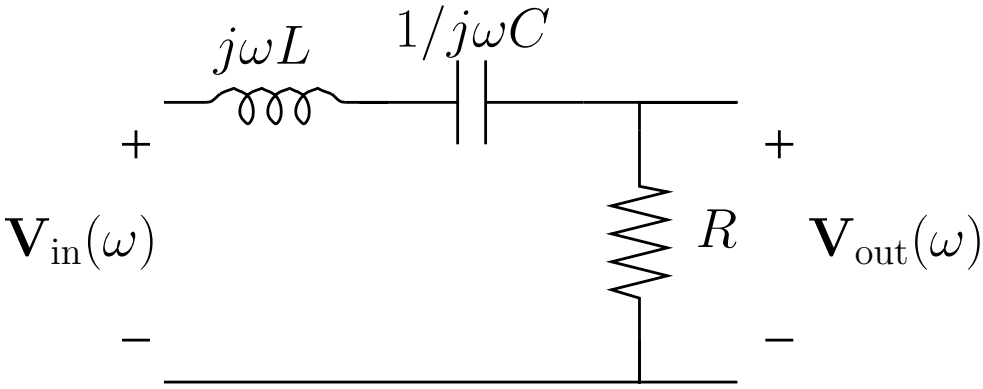
Bode plot for RC circuit – contd.

- $|H(\omega)|$ often idealized by two segments:
  - constant ($= 1$) from $\omega = 0$ to ω_o (the *passband* of the *low pass filter*), and
  - line dropping at 20 dB per decade for $\omega > \omega_o$ (the *stopband* of the filter)
- the *bandwidth* (frequency range) of the passband is ω_o (also called the 3dB bandwidth)



Frequency response of RLC circuit

consider a series RLC circuit in SSS:



the transfer function is:

$$\begin{aligned} H(\omega) &= \frac{R}{R + jwL + 1/j\omega C} \\ &= \frac{1}{1 + j(wL/R - 1/\omega RC)} \end{aligned}$$

its amplitude

$$|H(\omega)| = \frac{1}{\sqrt{1 + (wL/R - 1/\omega RC)^2}},$$

define the *reasonant frequency* of the circuit as: $\omega_o \triangleq 1/\sqrt{LC}$, and

the *quality factor* of the circuit as: $Q \triangleq \frac{\sqrt{L/C}}{R}$

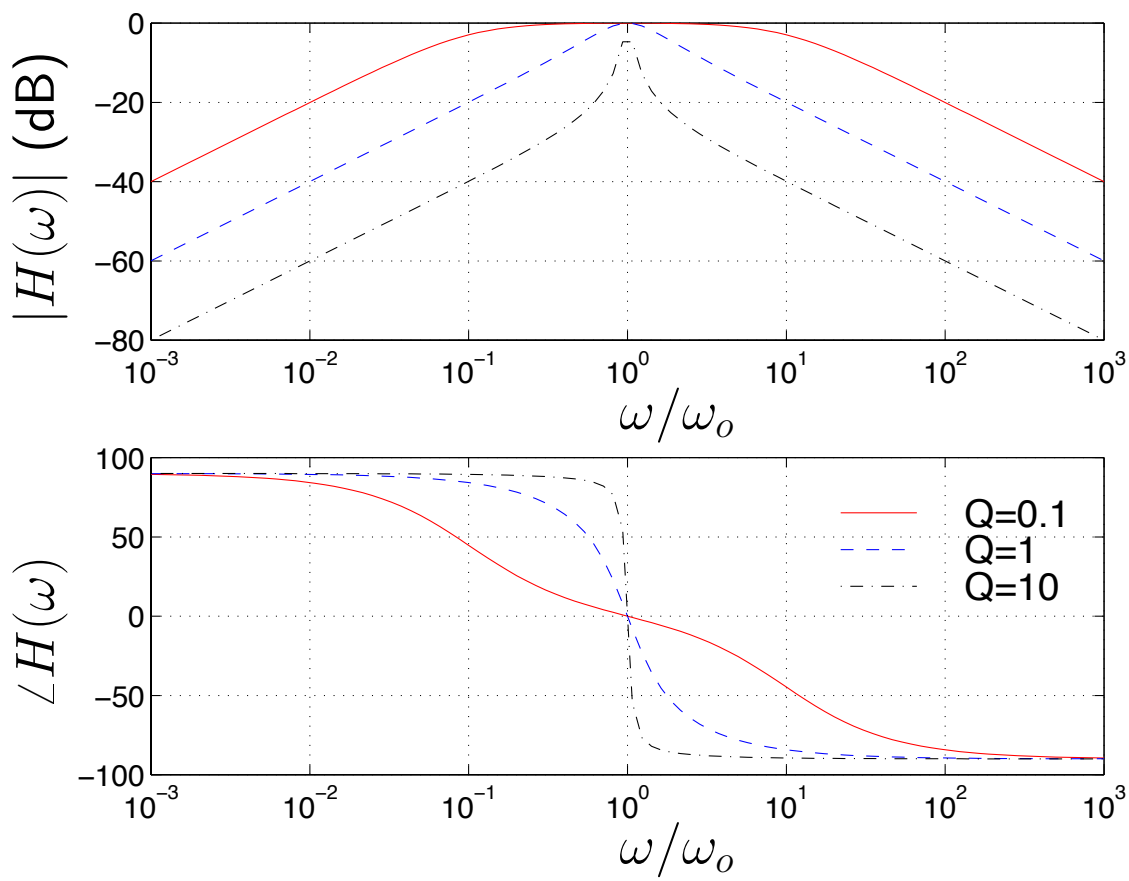
Response of RLC circuit – contd.

now we express the magnitude in terms of ω_o and Q as:

$$|H(\omega)| = \frac{1}{\sqrt{1 + (Q(\omega/\omega_o - \omega_o/\omega))^2}}$$

and the phase as:

$$\angle H(\omega) = \arctan\left(-Q(\omega/\omega_o - \omega_o/\omega)\right)$$



the circuit acts as a *bandpass* filter

Response of RLC circuit – contd.

- magnitude is maximum at $\omega = \omega_o$
- the 3 dB bandwidth of the circuit is the range of frequency where $|H(\omega)| > 1/\sqrt{2}$, $i.e.$, within 3 dB from the maximum ($= 1$ at ω_o)

  to find it, we set $|H(\omega)| = 1/\sqrt{2}$, which gives:

  $$Q(\omega/\omega_o - \omega_o/\omega) = \pm 1$$

  choosing the $+1$, we get the quadratic equation

  $$\omega^2 - \frac{\omega_o}{Q}\omega - \omega_o^2 = 0$$

  and we get the high end frequency of the bandwidth

  $$\omega_h = \omega_o \left(\sqrt{1 + (\frac{1}{2Q})^2} + \frac{1}{2Q} \right)$$

  similarly, choosing the -1, we can find the low end frequency

  $$\omega_l = \omega_o \left(\sqrt{1 + (\frac{1}{2Q})^2} - \frac{1}{2Q} \right)$$

  and the 3dB bandwidth is: $\omega_h - \omega_l = \omega_o/Q$, $i.e.$, the quality factor determines the *passband* of the filter (note: $\omega_o/Q = R/L$ independent of C!!)
- for $\omega >> \omega_h$ and $\omega << \omega_l$, $|H(\omega)|$ drops/rises at 20dB per decade, respectively

Lecture Notes 12

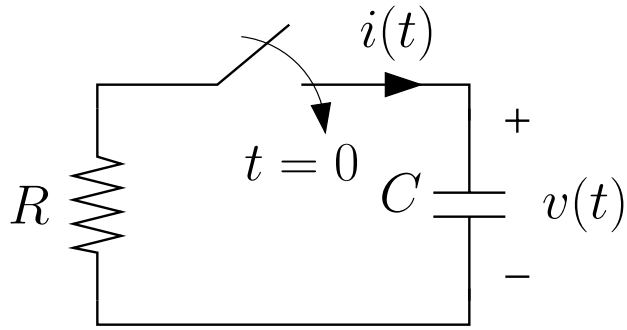
Natural and step response of first order circuits

- natural response of RC and RL circuits
- step response of RC circuit
- application: CMOS inverter delay
  - MOS transistor RC model
  - CMOS inverter delay using the RC model
  - MOS transistor first order dynamic model
- application: power dissipation in digital CMOS circuits
- natural and step response of general first order circuit
  - hand analysis method
  - unbounded response
- charge sharing

Natural response of RC circuit

natural response is the response of a dynamic circuit with no independent sources

consider an RC circuit with initial voltage on the capacitor $v(0^-) = v_o$



the natural response is $v(t)$ and $i(t)$ after the switch closes, $i.e.$, for $t \geq 0$:

- from device relation and KCL:

$$i(t) = C\frac{dv}{dt} = -\frac{1}{R}v(t)$$

  so we get the simple first order differential equation:

$$\frac{dv}{dt} = -\frac{1}{RC}v(t)$$

  with initial condition: $v(0^-) = v_o$

Natural response – contd.

- we can solve the differential equation by separating the variables:

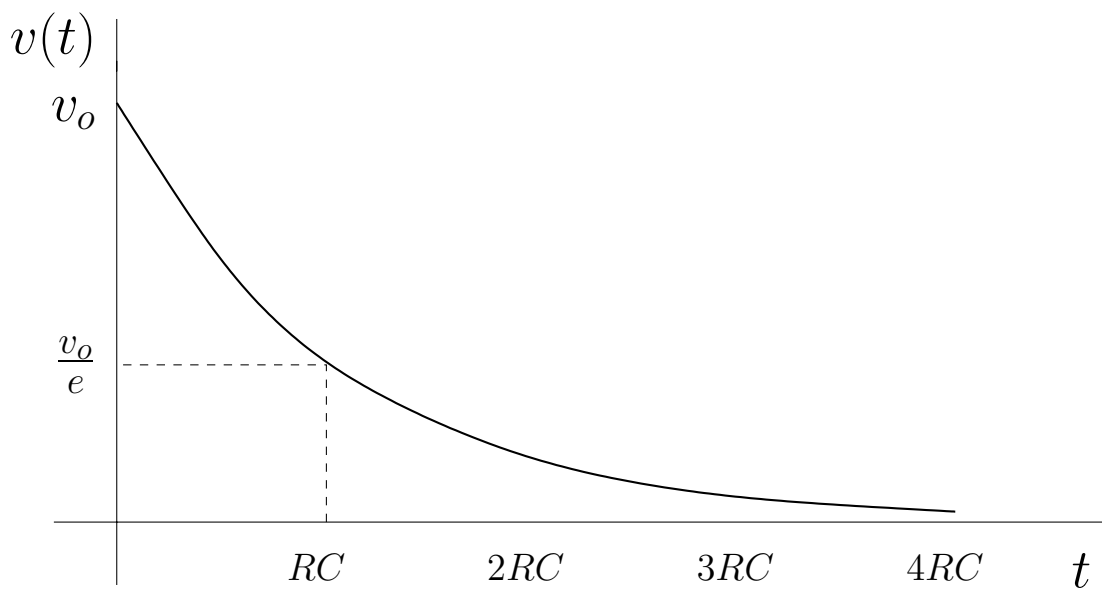
$$RC\frac{dv}{v(t)} = -dt,$$

now integrating from 0 to t:

$$\begin{aligned} RC\int_{v_o}^{v(t)} \frac{dv}{v} &= -t, \text{ we get} \\ RC\ln v\Big|_{v_o}^{v(t)} &= -t \end{aligned}$$

thus:

$$v(t) = v_o e^{-\frac{t}{RC}}$$



RC is called the circuit *time constant*, and has the units of $\frac{\mathrm{V}}{\mathrm{A}} \cdot \frac{\text{coul}}{\mathrm{V}} = \text{sec}$

Natural response – contd.

- the current, for $t \geq 0$, is given by:

$$i(t) = -\frac{v_o}{R} e^{-\frac{t}{RC}}$$

- so:
  - at $t = 0$, the voltage across R is v_o and $\frac{v_o}{R}$ flows *out of* the capacitor
  - if this current continued to flow, the capacitor would be discharged in RC seconds
  - but as current flows, the capacitor voltage decreases and therefore the current flow decreases as well . . .

Power and energy analysis

since KCL and KVL hold for all t, power conservation also holds for all t

so the *instantaneous* power dissipated in R:

$$p_R(t) = i^2(t)R = \frac{v_o^2}{R}e^{-2t/RC}$$

must equal the power supplied by the capacitor

the energy supplied by the capacitor from 0 to t is:

$$w(t) = \frac{1}{2}C(v_o^2 - v^2(t))$$

let's verify that it is the same as the energy dissipated in R from 0 to t

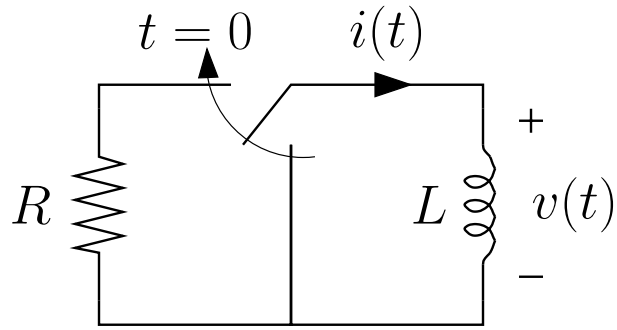
$$\begin{aligned} w(t) &= \int_0^t -i(\tau)v(\tau)d\tau \\ &= \int_0^t -C\frac{dv}{d\tau}v(\tau)d\tau \\ &= -\int_{v_o}^{v(t)} Cvdv \\ &= \frac{1}{2}C(v_o^2 - v^2(t)) \end{aligned}$$

as $t \rightarrow \infty$, $v(t) \rightarrow 0$ and $w(\infty) = \frac{1}{2}Cv_o^2$

$i.e.$, all the stored energy in the capacitor ends up as heat dissipated in the resistor . . .

Natural response of RL circuit

consider an RL circuit with no independent sources, and with initial current $i(0^-) = i_o$



using KCL and the inductor relation we get a differential equation (simular to the RC case) with solution, for $t \geq 0$:

$$i(t) = i_o e^{-t/(\frac{L}{R})}$$

and

$$v(t) = -i_o R e^{-t/(\frac{L}{R})}$$

the time constant for the circuit is (L/R) sec

the instantaneous power dissipated in the resistor:

$$p_R(t) = v^2(t)/R = i_o^2 R e^{-2t/(\frac{L}{R})}$$

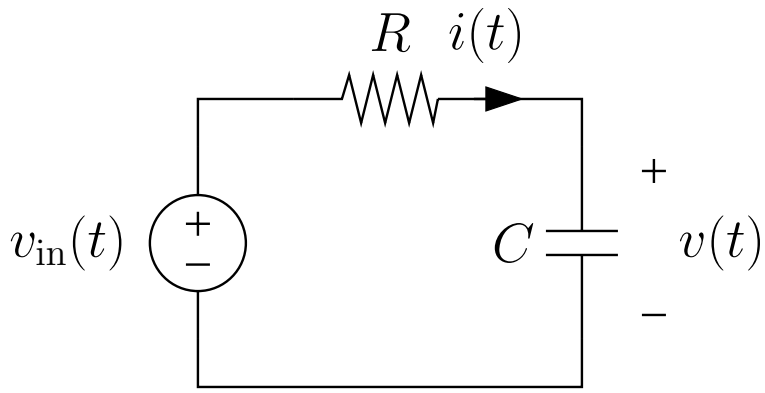
and the energy dissipated in the resistor from 0 to t is:

$$w(t) = \frac{1}{2} L (i_o^2 - i^2(t))$$

this is also the energy supplied by the inductor

Step response of RC circuit

here the RC circuit is *driven* by a step function voltage source and the capacitor is initially (at $t = 0^-$) uncharged:

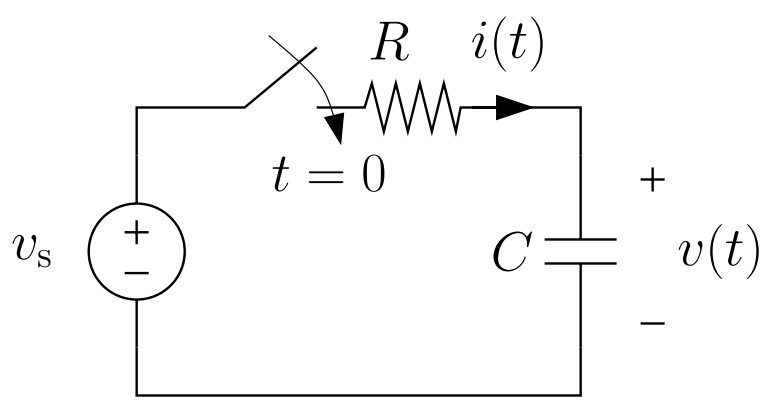


where

$$v_{\rm in}(t) = \begin{cases} 0 & t < 0 \\ v_{\rm s} & t \geq 0, \end{cases}$$

and $v(0^-) = 0$

an equivalent circuit is:



with $v(0^-) = 0$

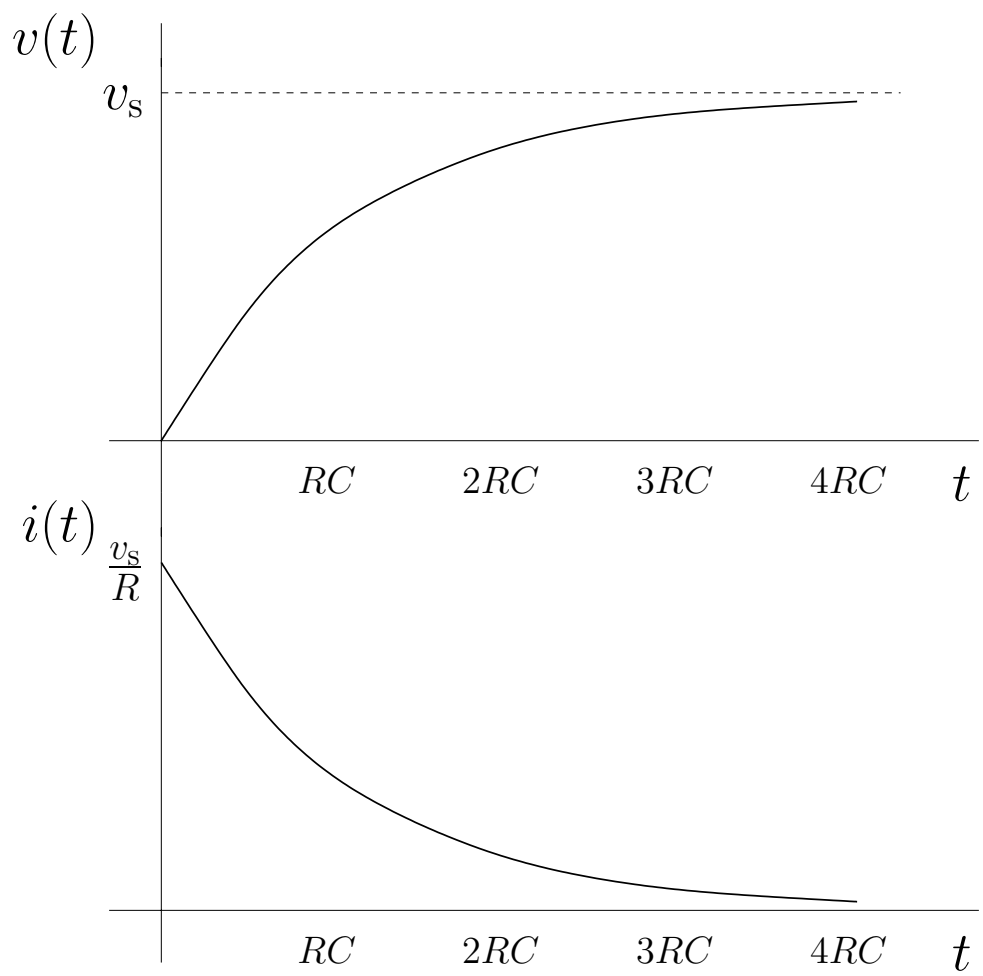
Step response of RC circuit – contd.

now for $t \geq 0$:

$$C\frac{dv}{dt} = i(t) = \frac{v_{\mathrm{s}} - v(t)}{R}$$

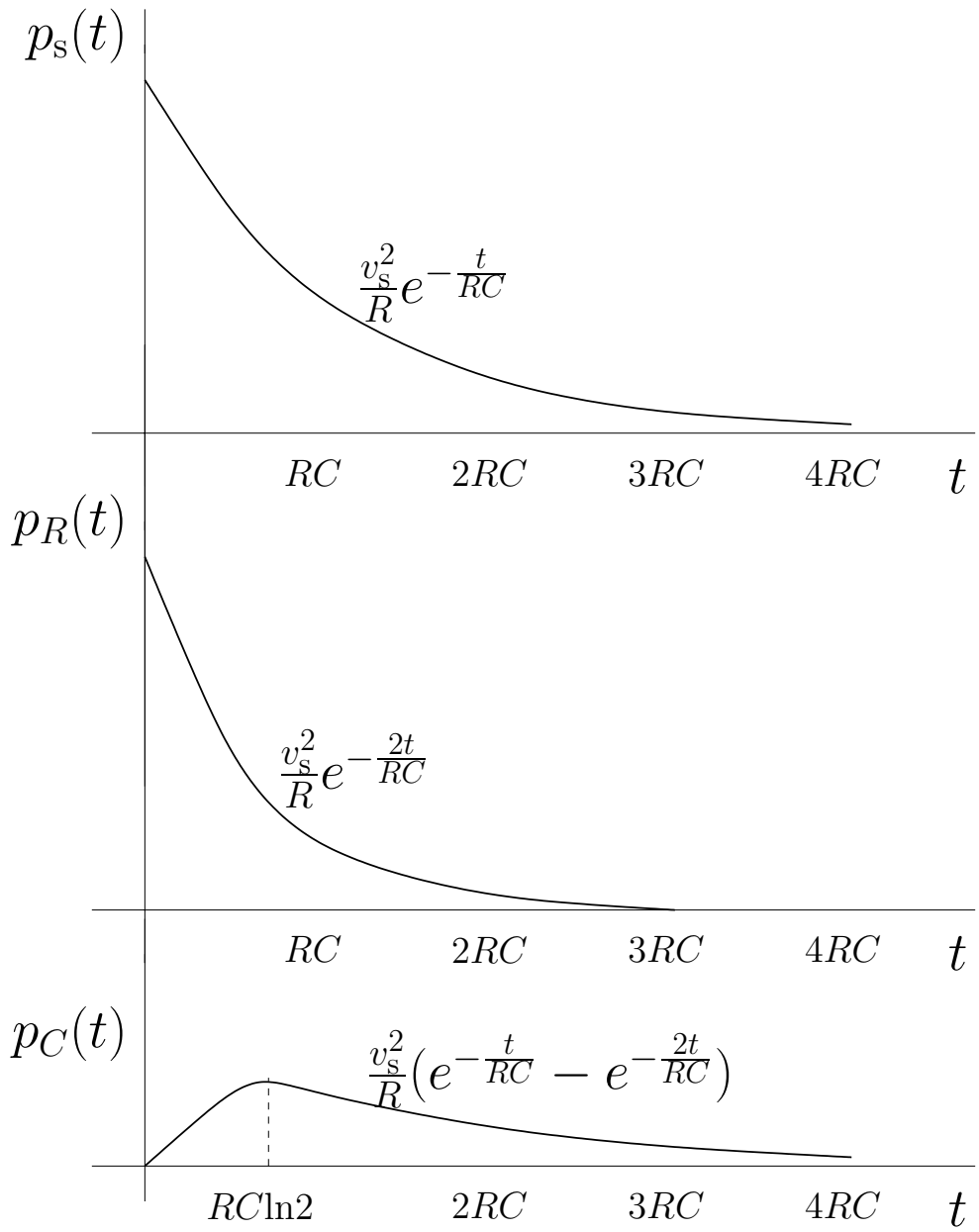
another linear differential equation with solution, for $t \geq 0$:

$$v(t) = v_{\mathrm{s}}(1 - e^{-\frac{t}{RC}}), \text{ and } \quad i(t) = \frac{v_{\mathrm{s}}}{R}e^{-\frac{t}{RC}}$$



Power and energy

let's plot the power supplied by the source $p_{\mathrm{s}}(t)$, dissipated in the resistor $p_R(t)$, and absorbed by the capacitor $p_C(t)$



Power and energy – contd.

note that:

- we only need to verify two out of the three plots – the third follows by power conservation
- the power absorbed in the capacitor first increases as the voltage on the capacitor rises, then decreases as the current falls – maximum achieved at $t = RC\ln 2$

now let's look at the energy in the circuit:

the energy supplied by the source from 0 to t is

$$\begin{aligned} w_{\mathrm{s}}(t) &= \int_0^t v_{\mathrm{s}} C \frac{dv}{d\tau} d\tau \\ &= C v_{\mathrm{s}} v(t), \end{aligned}$$

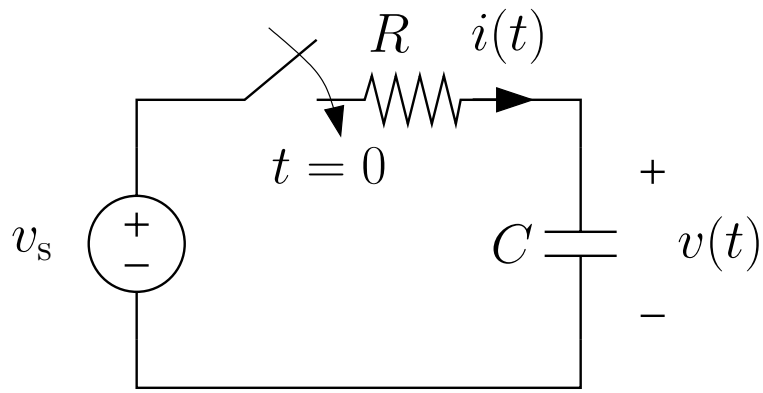
so as $t \rightarrow \infty$, $v(t) \rightarrow v_{\mathrm{s}}$, and:

- $w_{\mathrm{s}}(t) \rightarrow C v_{\mathrm{s}}^2$
- the energy stored in $C \rightarrow \frac{1}{2} C v_{\mathrm{s}}^2$
- the energy dissipated in R also $\rightarrow \frac{1}{2} C v_{\mathrm{s}}^2$

so as $t \rightarrow \infty$: the energy dissipated in R equals the energy stored in C and is *independent of* R !! (the rate of energy dissipation depends on R though)

Combined RC circuit response

consider the step response circuit with $v(0^-) = v_o$ (not necessarily 0)



we get the same step response differential equation but with non-zero initial condition
the solution is:

$$v(t) = v_o e^{-\frac{t}{RC}} + v_\mathrm{s}(1 - e^{-\frac{t}{RC}}),$$

and

$$i(t) = \frac{v_\mathrm{s} - v_o}{R} e^{-\frac{t}{RC}}$$

since the differential equation is linear this result can also be obtained by superposition of the natural and step responses
note: similar analysis can be carried out for an RL circuit (with step function voltage source) to get:

$$i(t) = i_o e^{-\frac{t}{(L/R)}} + \frac{v_\mathrm{s}}{R}(1 - e^{-\frac{t}{(L/R)}})$$

Application: CMOS inverter delay

in Lecture notes 3, we analyzed the CMOS inverter (static) $v_{\rm in}$ – $v_{\rm out}$ response using two MOS transistor models:

- the *switch model*, which provides a *digital* model for the inverter, and is used to verify its function
- the *first order static model*, which provides an *analog* model of the inverter and is used to find a more accurate response

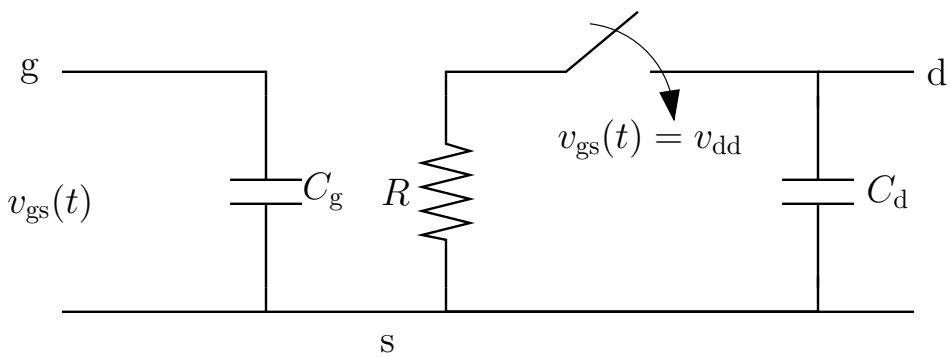
to analyze the switching delay of an inverter, $i.e.$, time to transition from '1' to '0' or from '0' to '1', we need a dynamic model:

- first we present a simple dynamic model for the MOS transistor called the *MOS transistor* RC model
- we use the model and the natural/step reponse of an RC circuit to find the delay
- we then discuss a more complex MOS transistor dynamic model called the *first order dynamic* model

MOS transistor RC model

the model assumes that $v_{\mathrm{gs}}(t)$ can take on only one of two values: $0\mathrm{V}$ (say logic '0') or v_{dd} (logic '1')

the two cases can be combined to get the circuit:

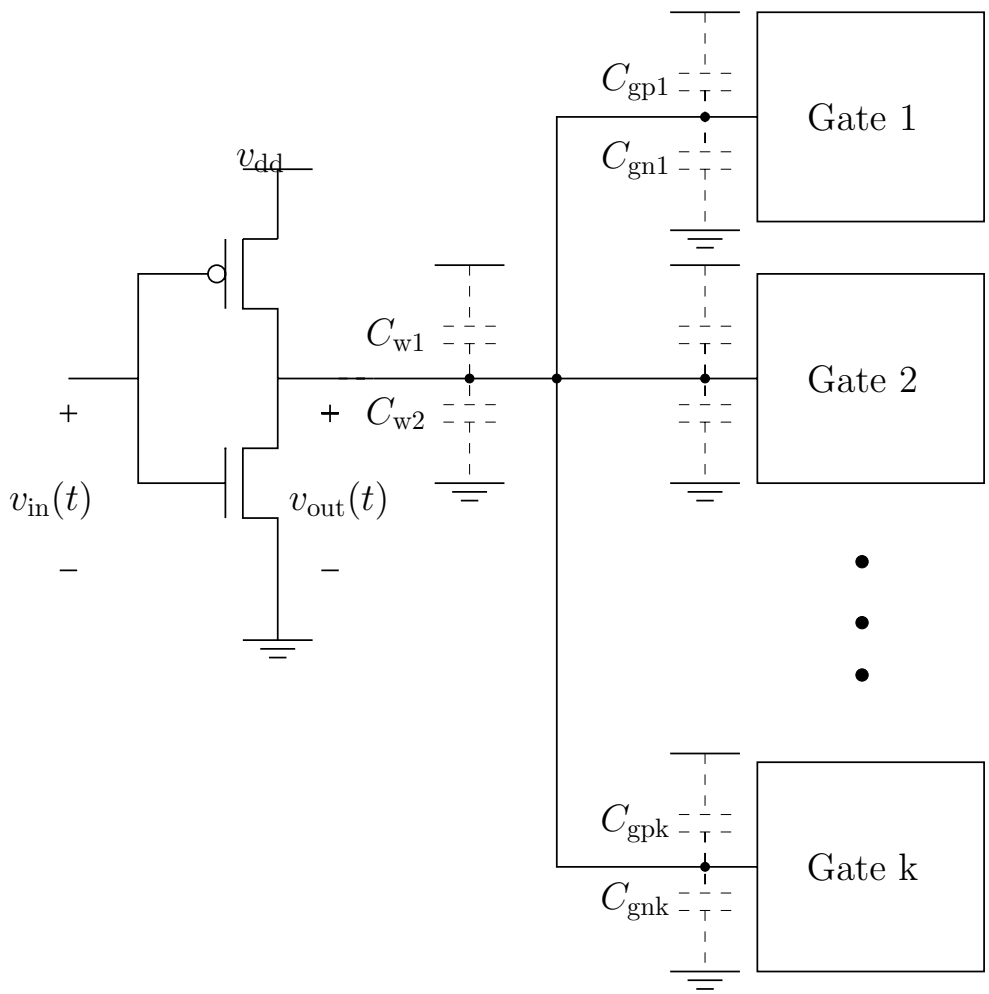


- the reference directions for $v_{\mathrm{gs}}(t)$, $v_{\mathrm{ds}}(t)$, and $i_{\mathrm{d}}(t)$ depend on whether the transistor is an 'n' or a 'p' type (g is '$+$', s is '$-$', and d is '$+$' for nMOS ...)
- in steady state, with $R = 0$, the model reduces to the switch model
- the values of the *gate capacitance* C_{g}, the *drain capacitance* C_{d}, and the 'output' resistance R depend on the fabrication process parameters and on the transistor physical dimensions (EE 112)
  - capacitances range from $1\mathrm{fF}$ to fraction of pF
  - resistance ranges from 10s of Ωs to 10s of $\mathrm{k}\Omega$s

CMOS inverter delay problem

a digital CMOS circuit consists of CMOS logic gates (inverters, NAND gates, NOR gates . . .) connected via metal wires

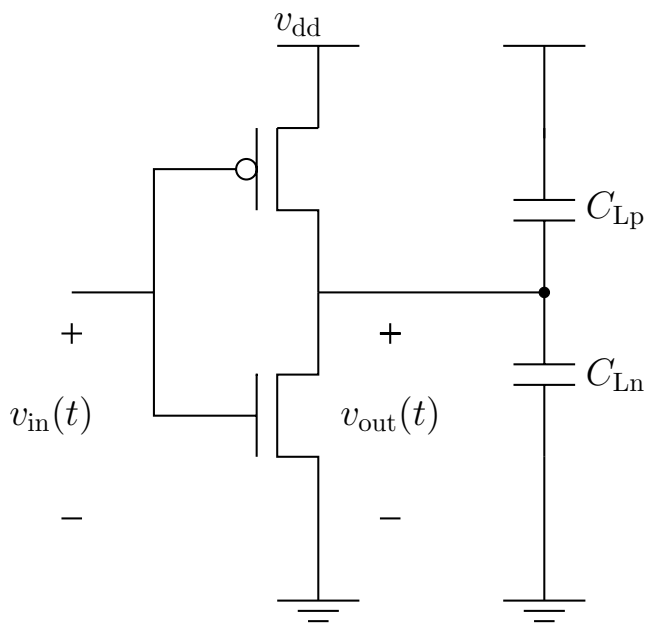
we consider an inverter in a digital CMOS circuit whose output is connected to (or *drives*) k other gates:



the capacitances shown represent the wiring and gate capacitances connected to the output of the inverter

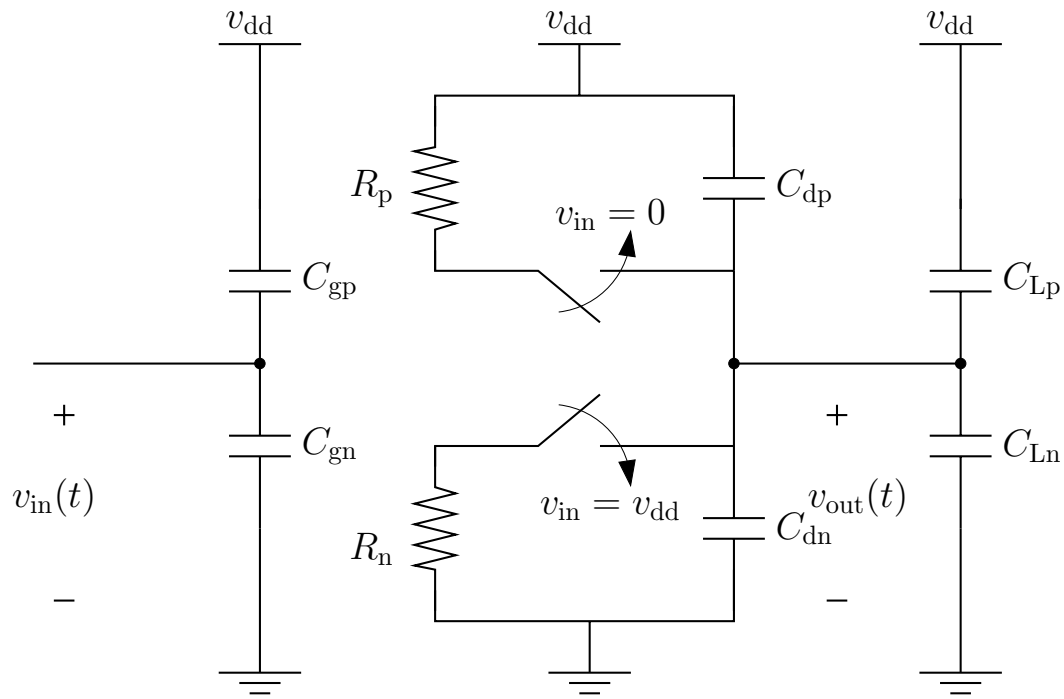
CMOS inverter delay problem – contd.

we can lump these capacitances into two *load* capacitances: C_{Ln} and C_{Lp} (C_{Ln} is the sum of all capacitances to ground . . .) to get the equivalent circuit:



to analyze the delay of the inverter we plug in the MOS transistor RC model for both transistors to get the circuit:

CMOS inverter delay problem – contd.



we will analyze this circuit by considering the two possible switching events:

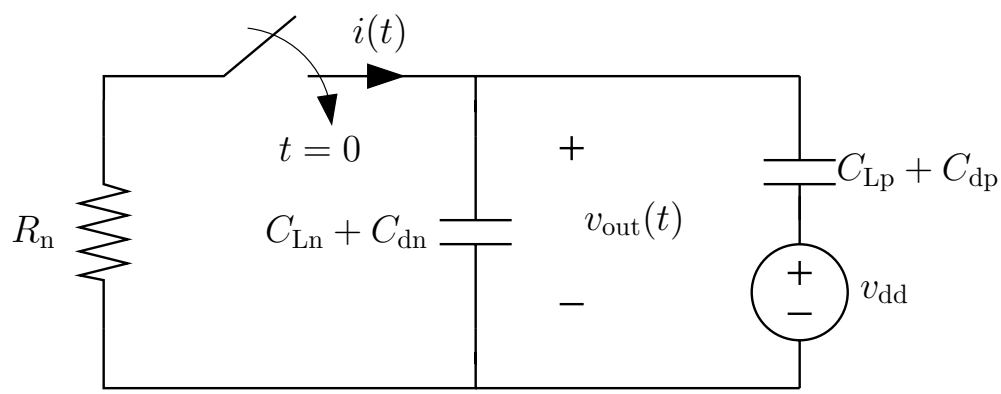
- **high-to-low** (or 'pull-down'): this is the case when the inverter output switches from '1' to '0', *i.e.*, the input switches from '0' to '1'
- **low-to-high** (or 'pull-up'): this is the opposite case

High-to-low (pull-down) delay

here the input to the inverter switches at $t = 0$ from low (logic '0') to high (logic '1'), *i.e.*, $v_{\rm in}(0^-) = 0$ and $v_{\rm in}(0^+) = v_{\rm dd}$

we assume that $v_{\rm out}(0^-) = v_{\rm H}$, where $v_{\rm H} \leq v_{\rm dd}$ ($\approx v_{\rm dd}$ if no switching has occurred for a very long time)

the equivalent circuit, for $t \geq 0$:

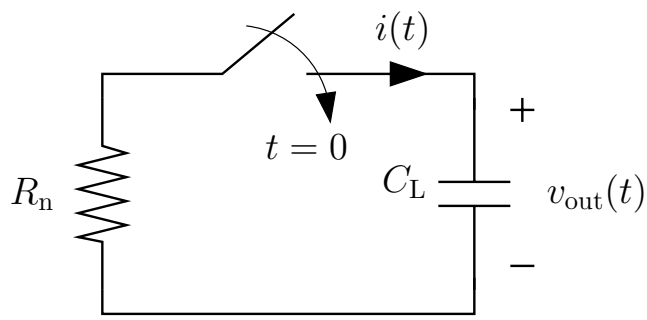


the circuit can be simplified further by inspecting its KCL differential equation:

$$\begin{aligned} i(t) &= (C_{\rm Ln} + C_{\rm dn})\frac{dv_{\rm out}}{dt} + (C_{\rm Lp} + C_{\rm dp})\frac{d(v_{\rm out} - v_{\rm dd})}{dt} \\ &= (C_{\rm Ln} + C_{\rm dn} + C_{\rm Lp} + C_{\rm dp})\frac{dv_{\rm out}}{dt} \end{aligned}$$

High-to-low delay – contd.

to get:



where

$$C_{\mathrm{L}} = C_{\mathrm{Ln}} + C_{\mathrm{dn}} + C_{\mathrm{Lp}} + C_{\mathrm{dp}}$$

is the load capacitance

so the problem reduces to finding the natural response of an RC circuit with $v_{\mathrm{out}}(0^-) = v_{\mathrm{H}}$

thus:

$$v_{\mathrm{out}}(t) = v_{\mathrm{H}} e^{-t/R_{\mathrm{n}}C_{\mathrm{L}}}$$

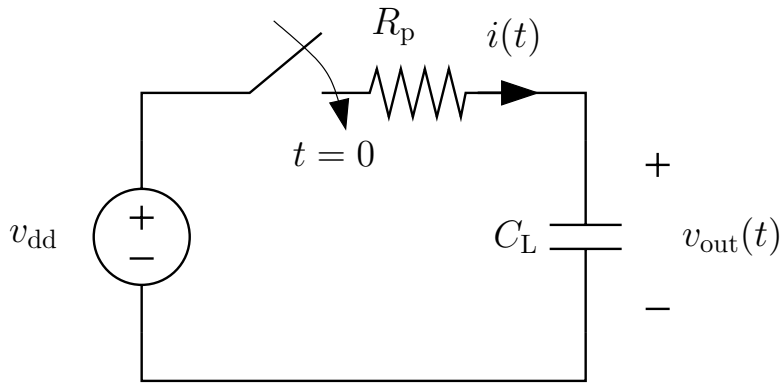
high-to-low delay (t_{HL}) is typically defined as the time to drop to $\frac{v_{\mathrm{dd}}}{2}$

substituting $v_{\mathrm{out}}(t) = \frac{v_{\mathrm{dd}}}{2}$ in the equation we get:

$$t_{\mathrm{HL}} = R_{\mathrm{n}}C_{\mathrm{L}} \ln\left(\frac{2v_{\mathrm{H}}}{v_{\mathrm{dd}}}\right) \text{ sec}$$

Low-to-high (pull-up) delay

here we get the equivalent circuit:



with $v_\mathrm{out}(0^-) = v_\mathrm{L}$ (≈ 0) and $v_\mathrm{s} = v_\mathrm{dd}$, and the problem reduces to finding the natural/step response of an RC circuit:

$$v_\mathrm{out}(t) = v_\mathrm{L} e^{-t/R_\mathrm{p}C_\mathrm{L}} + v_\mathrm{dd}(1 - e^{-t/R_\mathrm{p}C_\mathrm{L}})$$

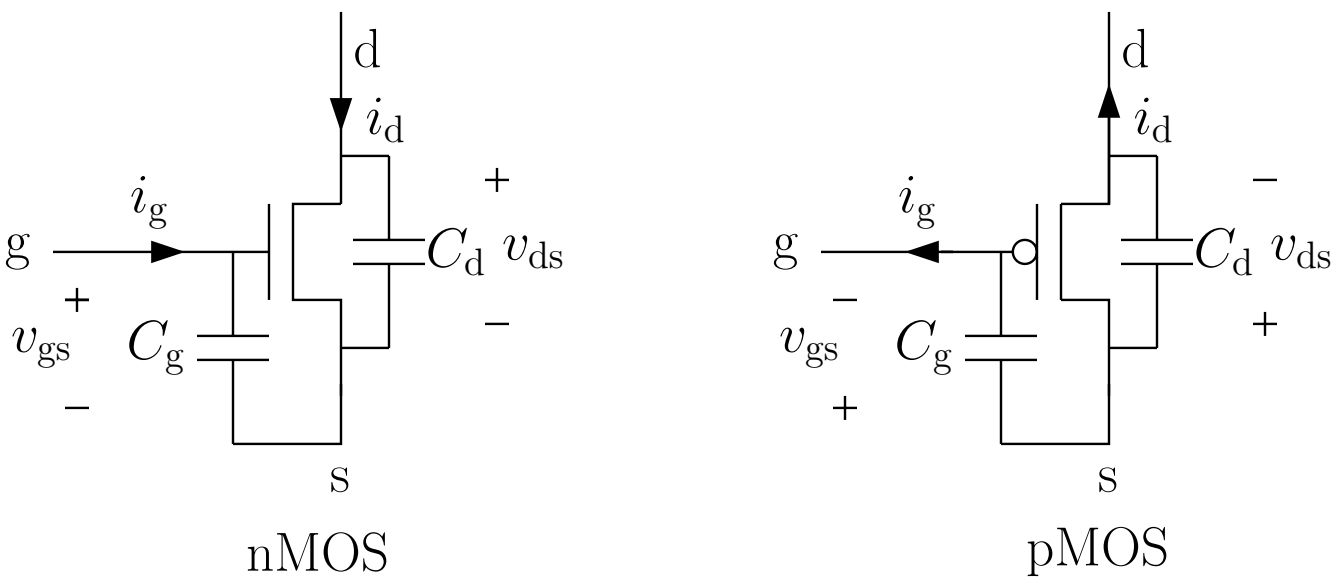
low-to-high delay (t_LH) is defined as the time to reach $\frac{v_\mathrm{dd}}{2}$

substituting $v_\mathrm{out}(t) = \frac{v_\mathrm{dd}}{2}$ in the equation we get:

$$t_\mathrm{LH} = R_\mathrm{p}C_\mathrm{L}\ln\frac{2(v_\mathrm{dd} - v_\mathrm{L})}{v_\mathrm{dd}} \text{ sec}$$

First order dynamic MOS model

a more accurate dynamic model adds C_{g} and C_{d} to the first order static model we discussed earlier
if we use the transistor symbols to mean the first order static model we get:



the model equations are:

$$
\begin{aligned}
i_{\mathrm{g}} &= C_{\mathrm{g}} \frac{dv_{\mathrm{gs}}}{dt} \\
i_{\mathrm{d}} &= i_{\mathrm{d}}^{\mathrm{static}} + C_{\mathrm{d}} \frac{dv_{\mathrm{ds}}}{dt}
\end{aligned}
$$

where

$$
i_{\mathrm{d}}^{\mathrm{static}} = \begin{cases} 0, & v_{\mathrm{gs}} \leq v_{\mathrm{t}} \\ \frac{k}{2} v_{\mathrm{ds}} (2v_{\mathrm{gs}} - 2v_{\mathrm{t}} - v_{\mathrm{ds}}), & 0 \leq v_{\mathrm{ds}} \leq v_{\mathrm{gs}} - v_{\mathrm{t}} \\ \frac{k}{2} (v_{\mathrm{gs}} - v_{\mathrm{t}})^2, & 0 < v_{\mathrm{gs}} - v_{\mathrm{t}} < v_{\mathrm{ds}} \end{cases}
$$

First order dynamic MOS model – contd.

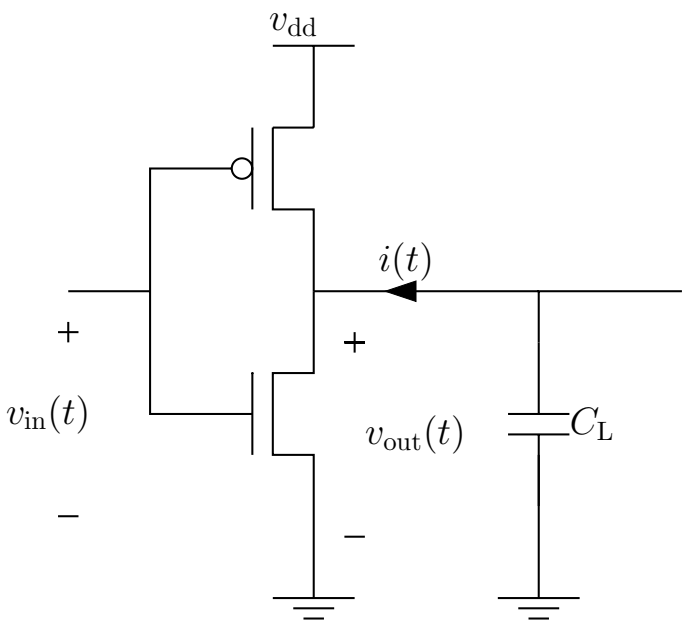
using this model:

- we can find a more accurate *waveform* for the inverter switching
- we can find the delay directly in terms of k and v_{t} ...
- can derive the RC model (see HW problem)

Application: Power dissipation in digital CMOS circuits

we can derive a very general formula for estimating power dissipation in digital circuits . . .

first we consider the energy dissipated when a CMOS inverter switches



to simplify the analysis we assume that $v_{\mathrm{L}} = 0$ and $v_{\mathrm{H}} = v_{\mathrm{dd}}$

Power dissipation in digital CMOS circuits – contd.

assume that at $t = 0$, the input transitions from $0 \rightarrow 1$, $i.e.$, from $0\mathrm{V}$ to v_{dd}

the energy dissipated in the nMOS transistor from $t = 0$ to ∞ ($i.e.$, as the output switches from $1 \rightarrow 0$):

$$\begin{aligned} w_{1 \rightarrow 0} &= \int_0^\infty i(t) v_{\mathrm{out}}(t) dt \\ &= -\int_0^\infty C_{\mathrm{L}} \frac{dv_{\mathrm{out}}}{dt} v_{\mathrm{out}}(t) dt \\ &= -C_{\mathrm{L}} \int_{v_{\mathrm{dd}}}^0 v dv \\ &= \frac{1}{2} C_{\mathrm{L}} v_{\mathrm{dd}}^2 \ \mathrm{J} \end{aligned}$$

note that the only assumptions we made about the transistor model is that $v_{\mathrm{out}}(t) \rightarrow 0$ as $t \rightarrow \infty$

similarly when the output transitions from $0 \rightarrow 1$

$$w_{0 \rightarrow 1} = \frac{1}{2} C_{\mathrm{L}} v_{\mathrm{dd}}^2 \ \mathrm{J}$$

Power dissipation in digital CMOS circuits – contd.

now let's use this result to estimate the power consumption in a digital CMOS circuit consisting of n logic gates:

- we assume that gate i has capacitance load C_{L_i} and switches (from $0 \rightarrow 1$ or $1 \rightarrow 0$) at rate of $2f_i$ per sec (so f_i is the switching frequency)
- assuming that f_i is low enough so that v_{out} reaches steady state ($i.e.$, v_{dd} or 0) before transitions, we get that the

  (average) power dissipation of gate i $= C_{\mathrm{L}_i} v_{\mathrm{dd}}^2 f_i$ W

- therefore for the circuit:

  total (average) power dissipation $= \sum_{i=1}^{n} C_{\mathrm{L}_i} v_{\mathrm{dd}}^2 f_i$ W

important consequence: since the average power consumption increases as the square of the supply voltage (and only linearly in the load C_{L} and the frequency f) the most effective way to reduce power is to lower the supply voltage of the circuit (this reduces the circuit speed, however . . .)

Example

consider a CMOS circuit operating at $v_{\mathrm{dd}} = 5\mathrm{V}$, and having 10^4 gates:

- 1000 gates have (average) load $C_{\mathrm{L}_1} = 0.1\mathrm{pF}$ and switching frequency $f_1 = 100$MHz
- 4000 gates have (average) load $C_{\mathrm{L}_2} = 0.5\mathrm{pF}$ and switching frequency $f_2 = 50$MHz
- 5000 gates have (average) load $C_{\mathrm{L}_3} = 1\mathrm{pF}$ and switching frequency $f_3 = 10$MHz

find the total average power consumption of the circuit

Step and natural response of a general first order circuit

a first order circuit consists only of:

- linear static elements, $e.g.$, resistors, dependent sources, op-amps
- independent sources
- one (equivalent) capacitor or inductor

we consider the case when the sources in the circuit consist only of constant and step function sources

equivalently, we assume that the circuit has constant sources and one or more *switches* that change state (open, close, change position) at certain time instances

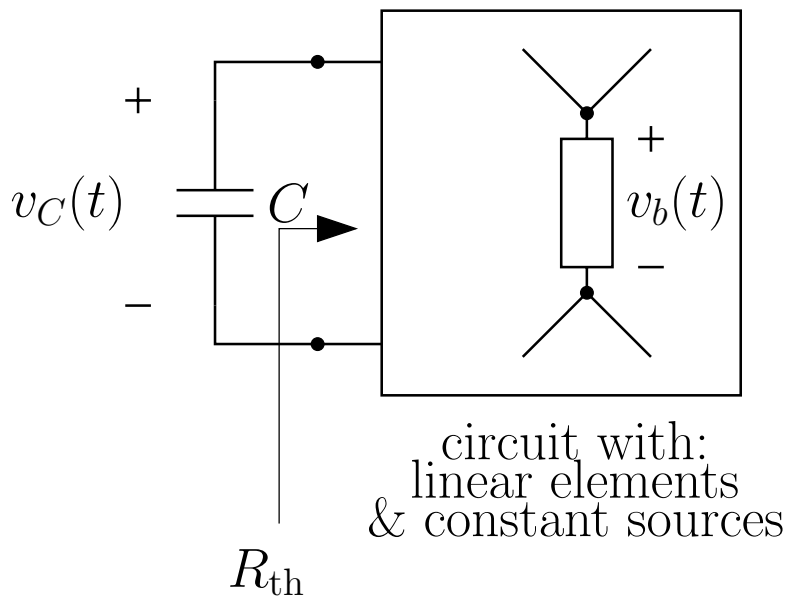
to simplify the analysis, we consider the case of only one switch changing state at $t = t_o$

the natural/step response of the circuit is its response after the switch changes state, $i.e.$, for $t \geq t_o$

we first describe a method for hand analysis of natural/step response of a first order circuit, work out an example, and then show why it works

Method for finding natural/step response

to find a branch voltage $v_b(t)$ for $t \geq t_o$, *i.e.*, after the switch changes state, consider the circuit:

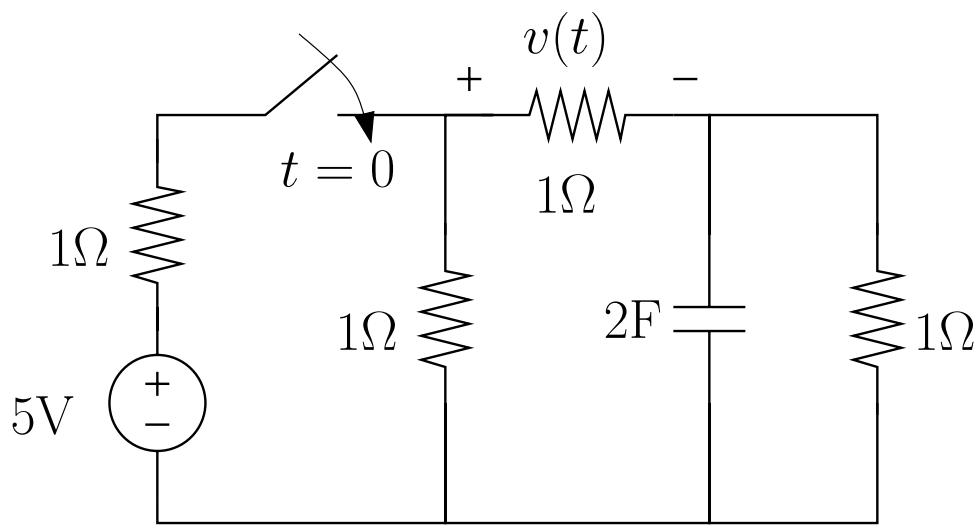


1. find the Thevenin resistance R_{th} (assume here that $R_{\text{th}} > 0$)
2. replace the capacitor by a voltage source $v_C(t_o^-)$ (the voltage on the capacitor before the switch changed state) and find $v_b(t_0^+)$
3. replace the capacitor by an open circuit and find $v_b(\infty)$ (the steady state voltage)
4. the branch voltage, for $t \geq t_o$:

$$v_b(t) = v_b(\infty) + (v_b(t_0^+) - v_b(\infty))e^{-\frac{(t-t_o)}{R_{\text{th}}C}}$$

branch current can be similarly found by replacing every v_b by i_b in the previous steps

Example

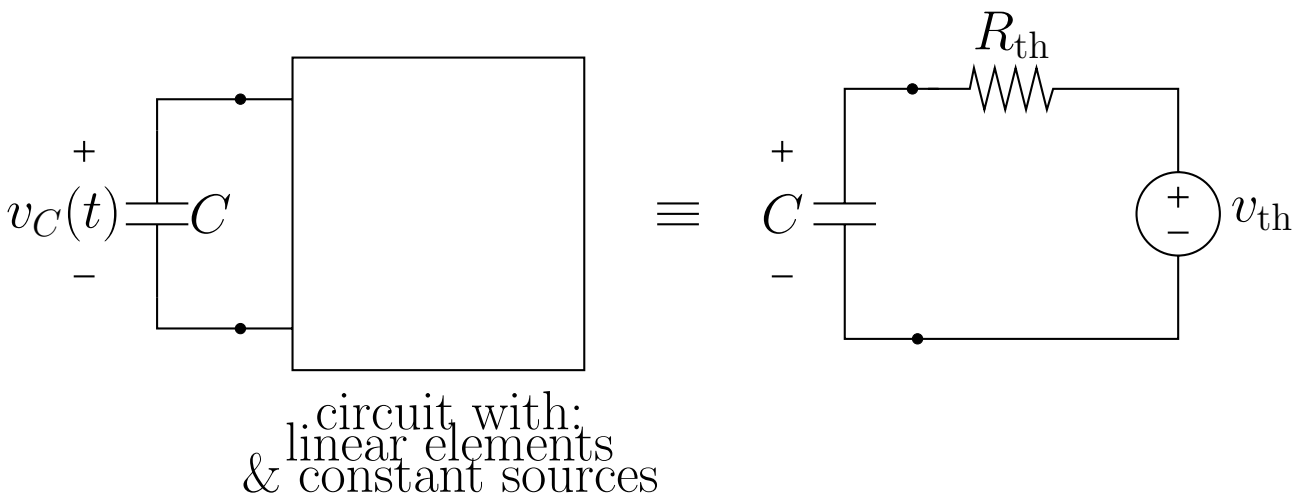


find $v(t)$, for $t > 0$, assuming that the circuit is in steady state at $t = 0^-$

Proof that the method works

let's show (using the giant matrix equation) why the method we described works

by Thevenin equivalence (for $t \geq t_o$):



thus, by the combined natural/step response of an RC circuit:

$$v_C(t) = v_{\text{th}} + (v_C(t_0^-) - v_{\text{th}})e^{-\frac{(t-t_o)}{R_{\text{th}}C}}$$

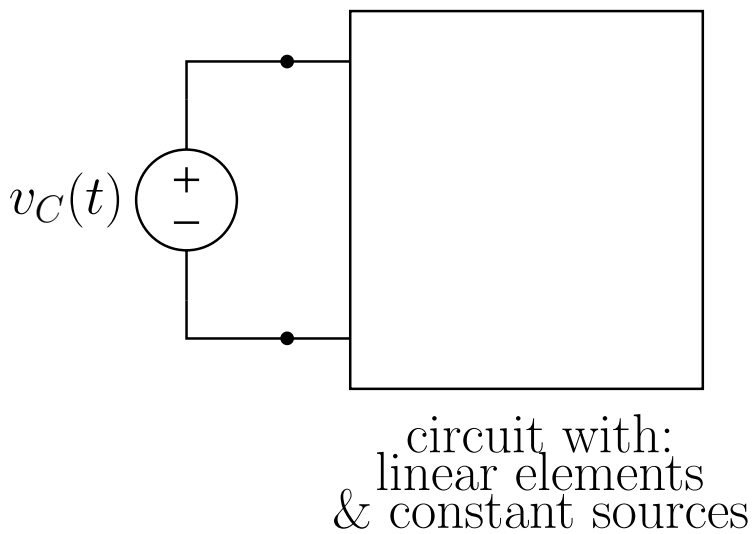
or

$$v_C(t) = v_{\text{th}} + (v_C(t_0^+) - v_{\text{th}})e^{-\frac{(t-t_o)}{R_{\text{th}}C}}$$

since (for $R_{\text{th}} > 0$) $v_C(t_0^+) = v_C(t_0^-)$ (the voltage cannot change instantaneously on the capacitor)

Proof – contd.

now replace the capacitor by the time varying voltage source $v_C(t)$:



clearly the values of the branch voltages and currents inside the circuit are the same as in the original circuit

now (by the giant matrix formula) any branch voltage or current is linear in the sources, thus we can write:

$$v_b(t) = v_b^{\mathrm{dc}} + c_b e^{-\frac{(t-t_o)}{R_{\mathrm{th}}C}},$$

where v_b^{dc} is the contribution of the constant sources and c_b is a constant coefficient

Proof – contd.

to find v_b^{dc} and c_b, we need two equations:

- first we set $t = \infty$ and get $v_b^{\mathrm{dc}} = v_b(\infty)$ (which corresponds to the capacitor being treated as an open circuit)
- now we set $t = t_o^+$ and get $c_{\mathrm{b}} = v_b(t_o^+) - v_b(\infty)$ (this corresponds to the case where the capacitor is replaced by a voltage source $v_C(t_o^+) = v_C(t_o^-)$)
- substituting in the $v_b(t)$ equation completes the proof that the method works ...

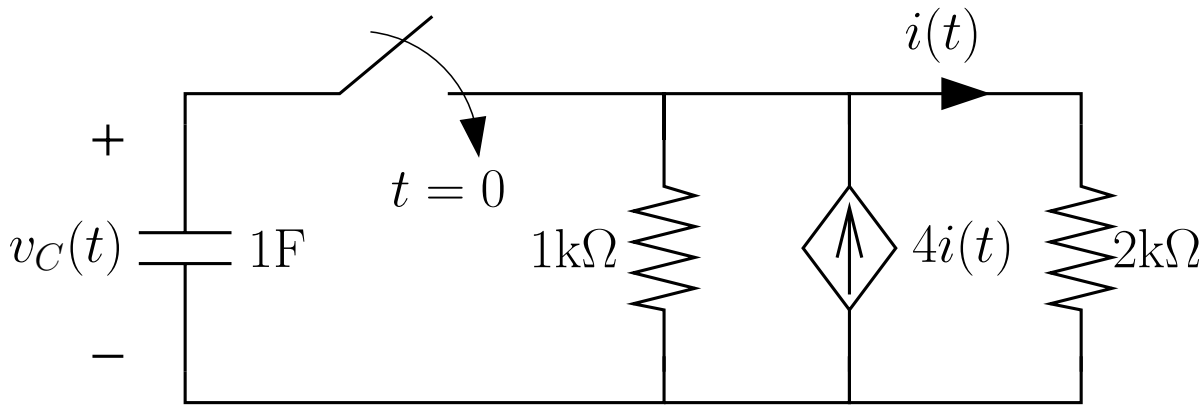
Unbounded response

the method we described for hand analysis of first order circuits assumes that $R_{\text{th}} > 0$

if $R_{\text{th}} < 0$, the circuit response becomes unbounded

in this case we say that the circuit is *unstable* (more on this in EE 102)

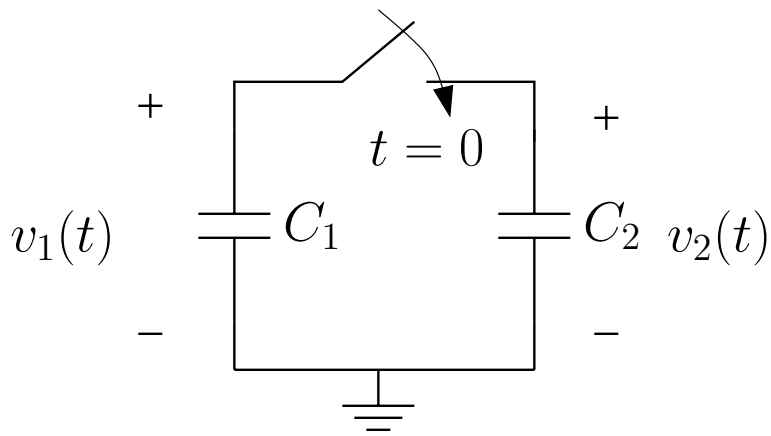
for example, consider the circuit:



assuming $v_C(0) = 10\text{V}$, find $v_C(t)$, for $t > 0$

Charge sharing

consider a circuit with two capacitors:



assume that C_2 is initially (before the switch closes) uncharged but that C_1 has a non-zero initial voltage $v_1(0^-)$

what is the voltage on the capacitors after the switch closes ?

clearly when the switch closes $v_1(t) = v_2(t)$ (KVL must be satisfied)

also the charge on C_1 cannot go anywhere, so

$$C_1 v_1(0^-) = (C_1 + C_2) v_1(t),$$

which gives the *charge sharing* solution:

$$v_1(t) = v_2(t) = \frac{C_1}{C_1 + C_2} v_1(0^-)$$

Charge sharing – contd.

let's find out if this makes sense ...

the energy stored on C_1 before the switch closes is:

$$w(0^-) = \frac{1}{2}C_1 v_1^2(0^-)$$

after the switch closes (if we believe our result) the energy stored on the two capacitors is:

$$w(t) = \frac{1}{2}(C_1 + C_2)(\frac{C_1}{C_1 + C_2})^2 v_1^2(0^-) = \frac{1}{2}\frac{C_1^2}{C_1 + C_2}v_1^2(0^-)$$

smaller than $w(0^-)$!!

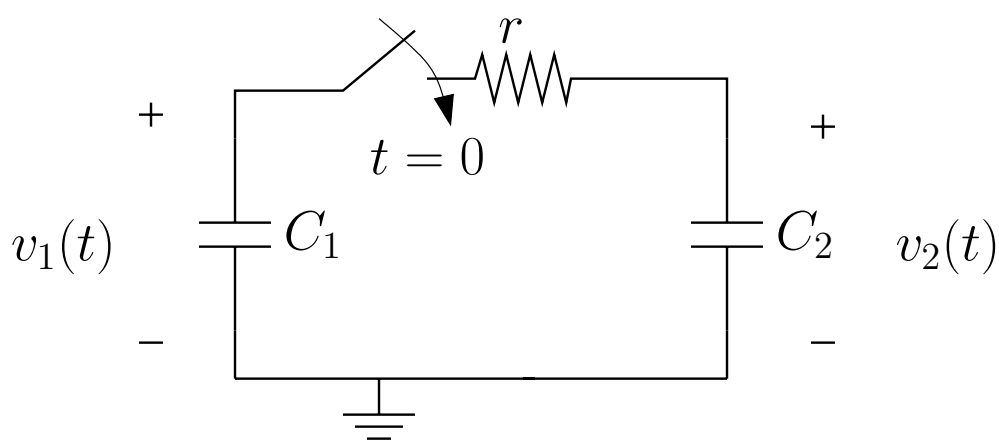
where did the difference in energy go ? capacitors are lossless (they cannot dissipate energy)

well, either our result is wrong or the energy must have been dissipated somehow

Charge sharing – contd.

in order to answer this question we need to make this problem more physically meaningful

so we insert a small resistance (since in reality there must be some non-zero resistance in the path)



after the switch closes, by KCL

$$-C_1 \frac{dv_1}{dt} = C_2 \frac{dv_2}{dt}$$

thus

$$-C_1 \int_{v_1(0^-)}^{v_1(t)} dv_1 = C_2 \int_0^{v_2(t)} dv_2$$

or

$$v_2(t) = \frac{C_1}{C_2}(v_1(0^-) - v_1(t))$$

Charge sharing – contd.

now, by KVL, and substitution:

$$rC_1\frac{dv_1}{dt} = v_2 - v_1 = \frac{C_1}{C_2}v_1(0^-) - \frac{C_1+C_2}{C_2}v_1(t)$$

solving by separating the variables, we get

$$v_1(t) = \frac{C_1}{C_1+C_2}v_1(0^-) + \frac{C_2}{C_1+C_2}v_1(0^-)e^{-t/\frac{rC_1C_2}{C_1+C_2}}$$

so as $t \to \infty$ (or as $r \to 0$)

$$v_1(t) \to \frac{C_1}{C_1+C_2}v_1(0^-)$$

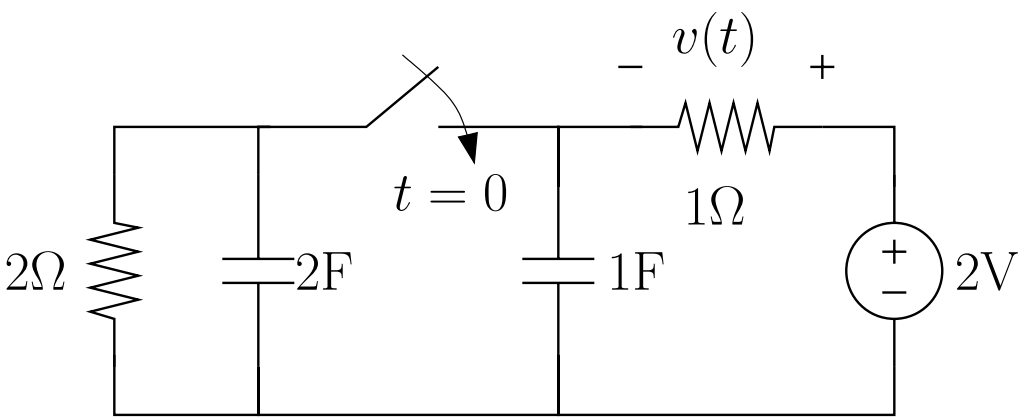
now, by energy conservation, the energy dissipated in r from $t = 0$ to ∞ equals the difference between the energy stored before and after the switch closes, and is independent of r

so the answer to our earlier question is that the energy is dissipated in the resistor (and is the same independent of how small r is)

charge sharing has several important applications, $e.g.$, DRAM operation (HW problem), sample and hold circuit ...

Example

consider the following circuit with two capacitors



find $v(t)$ for $t > 0$, assuming that the circuit is in steady state at $t = 0^-$

Lecture Notes 13
Summary

- device models
- circuit analysis techniques
- circuit theory
- power and energy
- applications

EE 101

EE 101 deals with basic circuit *analysis* techniques

analysis done using *only*:

- device models
- Khirkoff's current and voltage laws (KCL, KVL)

device models:

- same device can have many different models
  - for different modes of operation, $e.g.$, analog vs. digital, static (dc) vs. dynamic (ac)
  - very simple models for hand analysis
  - more complex and accurate models for computer simulation
- it is not necessary to understand in detail the origin of a model, but it is necessary to understand the limits of its applicability

Example: MOS transistor

we discussed five different models:

- switch model
  - only useful for analyzing the function of an MOS digital circuit
- first order static model
  - provides more accurate $v_{\rm in} - v_{\rm out}$ relation for MOS digital circuits, $e.g.$, an inverter
  - useful for large signal (dc) analysis of analog MOS circuits
- small signal model
  - good for analysis around a dc bias point
- RC model
  - good for hand analysis of delay in MOS digital circuits
- first order dynamic model
  - good for large signal analysis of dynamic MOS circuits

Circuits we discussed

we focused on three types of circuits:

- static (dc) circuits with both linear and nonlinear elements
- circuits in sinusoidal steady state
- natural/step response of first order dynamic circuits

hand analysis techniques for static and SSS circuits:

- series/parallel reductions, voltage/current divider, source transformation
- node voltage method
- superposition
- Thevenin and Norton equivalence
- load line – graphical method for static circuits with nonlinear elements
- small signal circuit analysis

Circuits we discussed – contd.

hand analysis technique for natural/step response:

- switch changing state at $t = 0$, branch voltage (or current) for $t \geq 0$:

$$v_{\mathrm{b}}(t) = v_{\mathrm{b}}(\infty) + (v_{\mathrm{b}}(0^+) - v_{\mathrm{b}}(\infty))e^{-t/\tau}$$

  - $\tau = R_{\mathrm{th}}C$ for capacitor and L/R_{th} for inductor
  - $R_{\mathrm{th}} > 0$: Thevenin resistance at storage element terminals

other hand analysis techniques:

- charge sharing
- write the differential equation for the circuit (using branch relations, KVL, KVL) and solve it

Circuit theory

circuit variables: branch voltage vector, $v(t)$, branch current vector $i(t)$, and node voltage vector $e(t)$

KCL: $Ai(t) = 0$ and KVL: $v(t) = A^T e(t)$ hold for all t

consequence: in *any* circuit, instantaneous power is conserved, for all t

for circuit with only linear static elements and sources:

- branch relations:

$$Mi + Nv = s$$

- circuit equations in one giant matrix equation:

$$\begin{bmatrix} A & 0 & 0 \\ 0 & I & -A^T \\ M & N & 0 \end{bmatrix} \begin{bmatrix} i \\ v \\ e \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ s \end{bmatrix}$$

  solution:

$$\begin{bmatrix} i \\ v \\ e \end{bmatrix} = \begin{bmatrix} A & 0 & 0 \\ 0 & I & -A^T \\ M & N & 0 \end{bmatrix}^{-1} \begin{bmatrix} 0 \\ 0 \\ s \end{bmatrix}$$

Circuit theory – contd.

- consequences:
  - any circuit variable can be expressed as linear function of the *independent* sources
  - we used the formulation to derive node voltage, superposition, and Thevenin and Norton

for circuit with only linear static elements, Cs and Ls, and sinusoidal sources with the same frequency, circuit equations (in terms of phasors):

$$\begin{bmatrix} \mathbf{I} \\ \mathbf{V} \\ \mathbf{E} \end{bmatrix} = \begin{bmatrix} A & 0 & 0 \\ 0 & I & -A^T \\ M & N & 0 \end{bmatrix}^{-1} \begin{bmatrix} 0 \\ 0 \\ \mathbf{S} \end{bmatrix}$$

same consequences as static circuits . . . ,

and average power is conserved

Power and energy

analyzed power and energy is circuits:

- with associated reference directions: $p(t) > 0$ means power is *absorbed*, $p(t) < 0$ means power is supplied
- power is conserved in any circuit, for all t
- energy stored in capacitor: $\frac{1}{2}Cv(t)^2$,
  in inductor: $\frac{1}{2}Li(t)^2$
- in SSS circuits:
  - instantaneous power:
    $$p(t) = \frac{|I||V|}{2}\cos(2\omega t + \angle I + \angle V) + \frac{|I||V|}{2}\cos(\angle I - \angle V)$$
  - average power:
    $$p_{\text{avg}} = \frac{|I||V|}{2}\cos(\angle I - \angle V) = \frac{1}{2}\operatorname{Re}(\overline{\mathbf{V}}\mathbf{I}) = \frac{1}{2}\operatorname{Re}(\overline{\mathbf{I}}\mathbf{V})$$
    in terms of impedance:
    $$p_{\text{avg}} = \frac{1}{2}|\mathbf{I}|^2\operatorname{Re}(Z) = \frac{1}{2}|\mathbf{V}|^2\operatorname{Re}(Y)$$
  - energy stored in capacitor:
    $$E_{\max} = \frac{1}{2}|\mathbf{V}|^2 C = 2E_{\text{avg}}$$
    and in inductor:
    $$E_{\max} = \frac{1}{2}|\mathbf{I}|^2 L = 2E_{\text{avg}}$$

Applications

discussed many practical applications along the way:

- MOS digital circuits: function, delay, power dissipation
- DRAM operation
- amplifiers: small signal, integrating amplifier, charge amplifier
- electric power and communication systems
- a bit about frequency response and filters

emphasized circuit analysis techniques that are important for modern circuit design . . .