Devices for Integrated Multi-Aperture Imaging

Ph.D. Oral Examination
May 28, 2008

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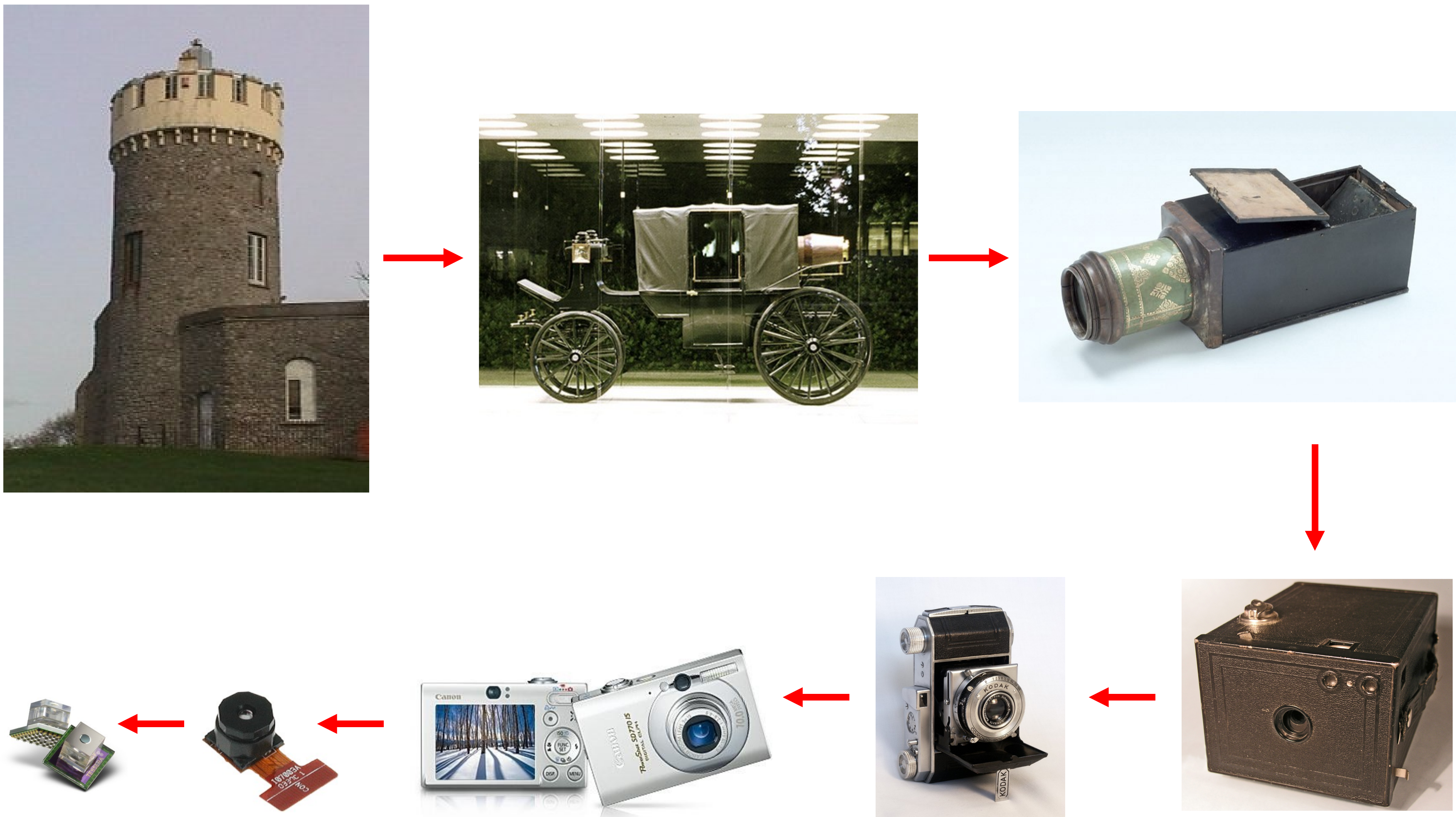
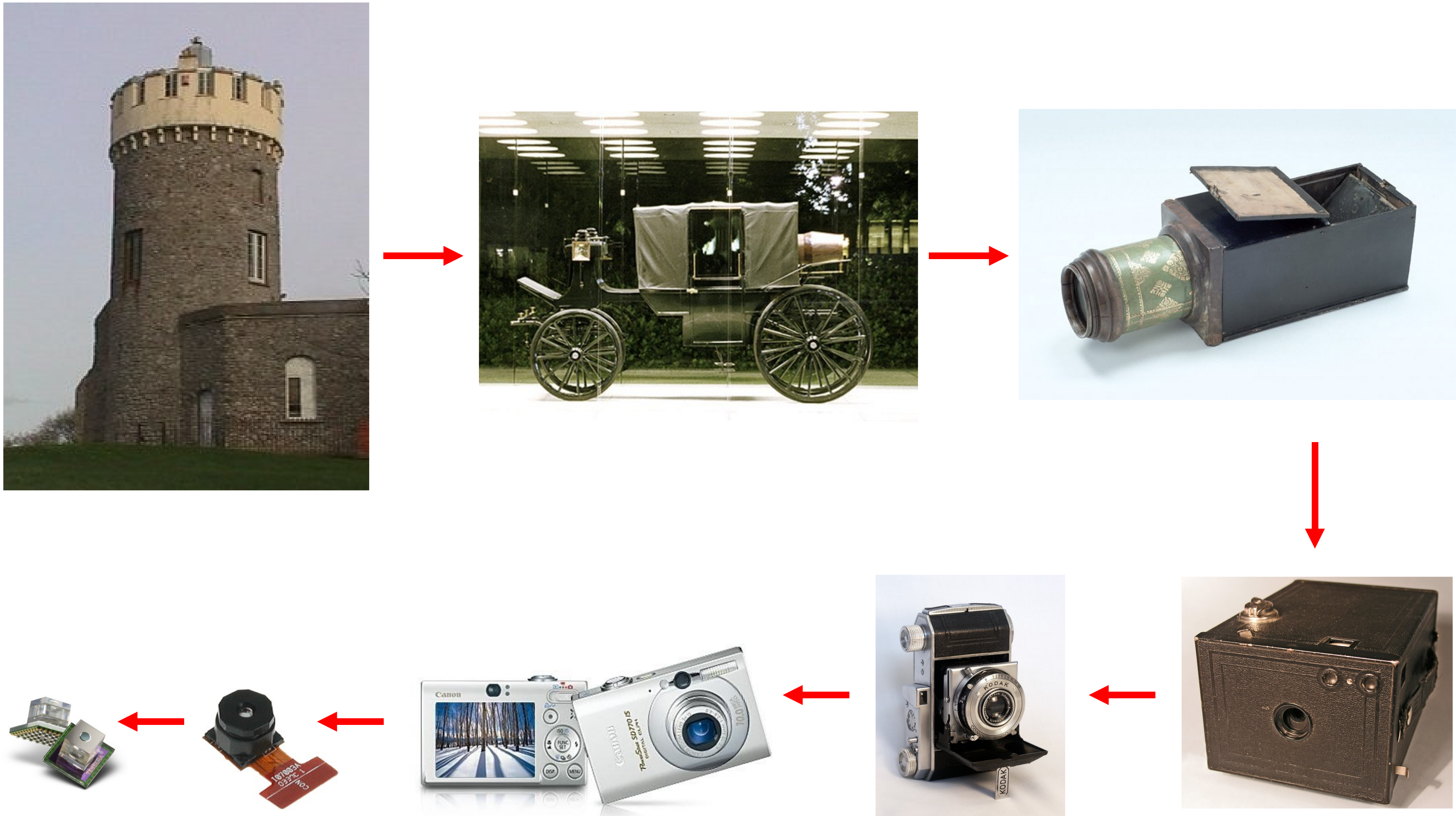
Camera History



Camera History



- Despite progress, each of these cameras form images in the same way

Image Formation in a Camera

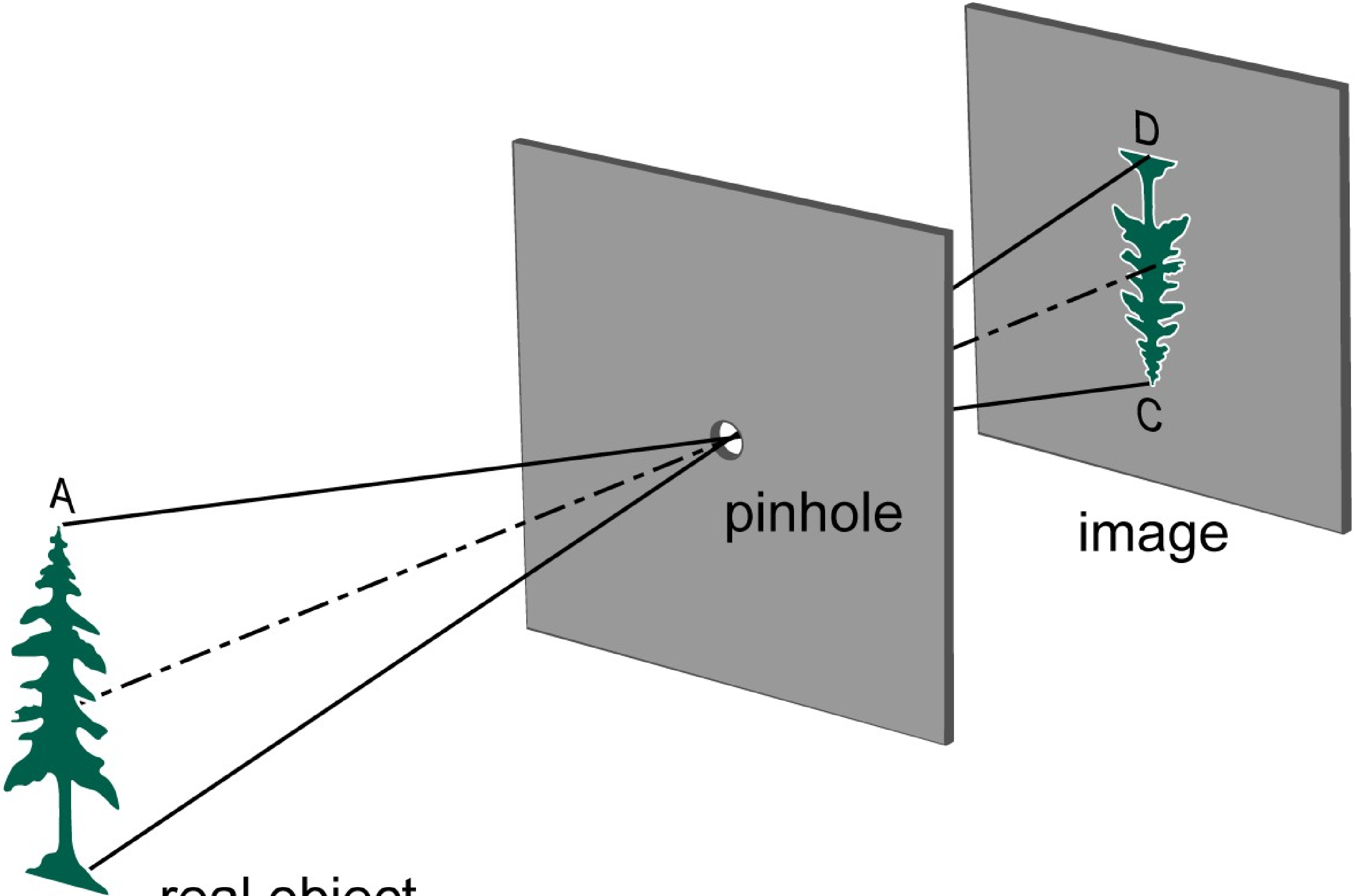


Image Formation in a Camera

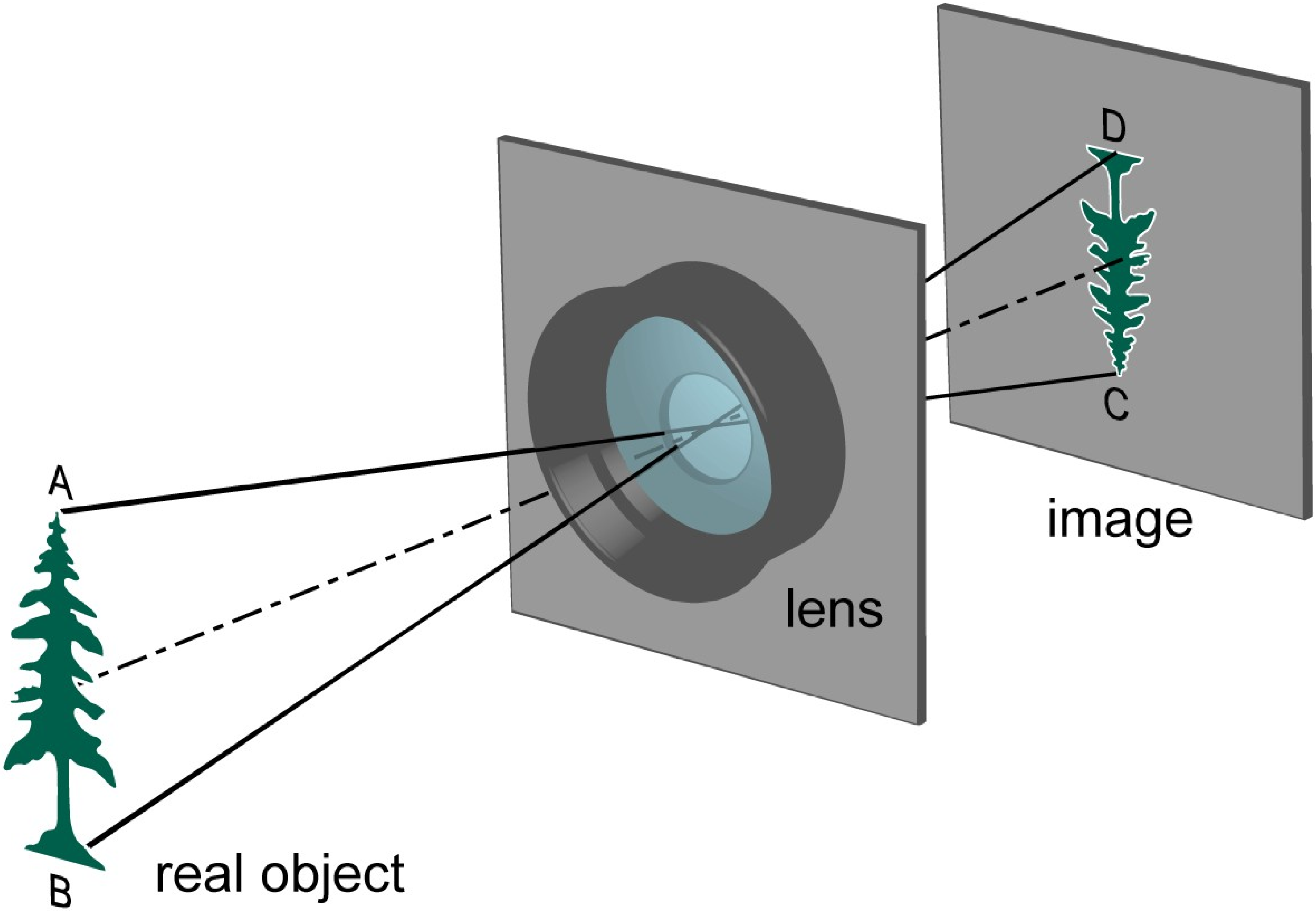
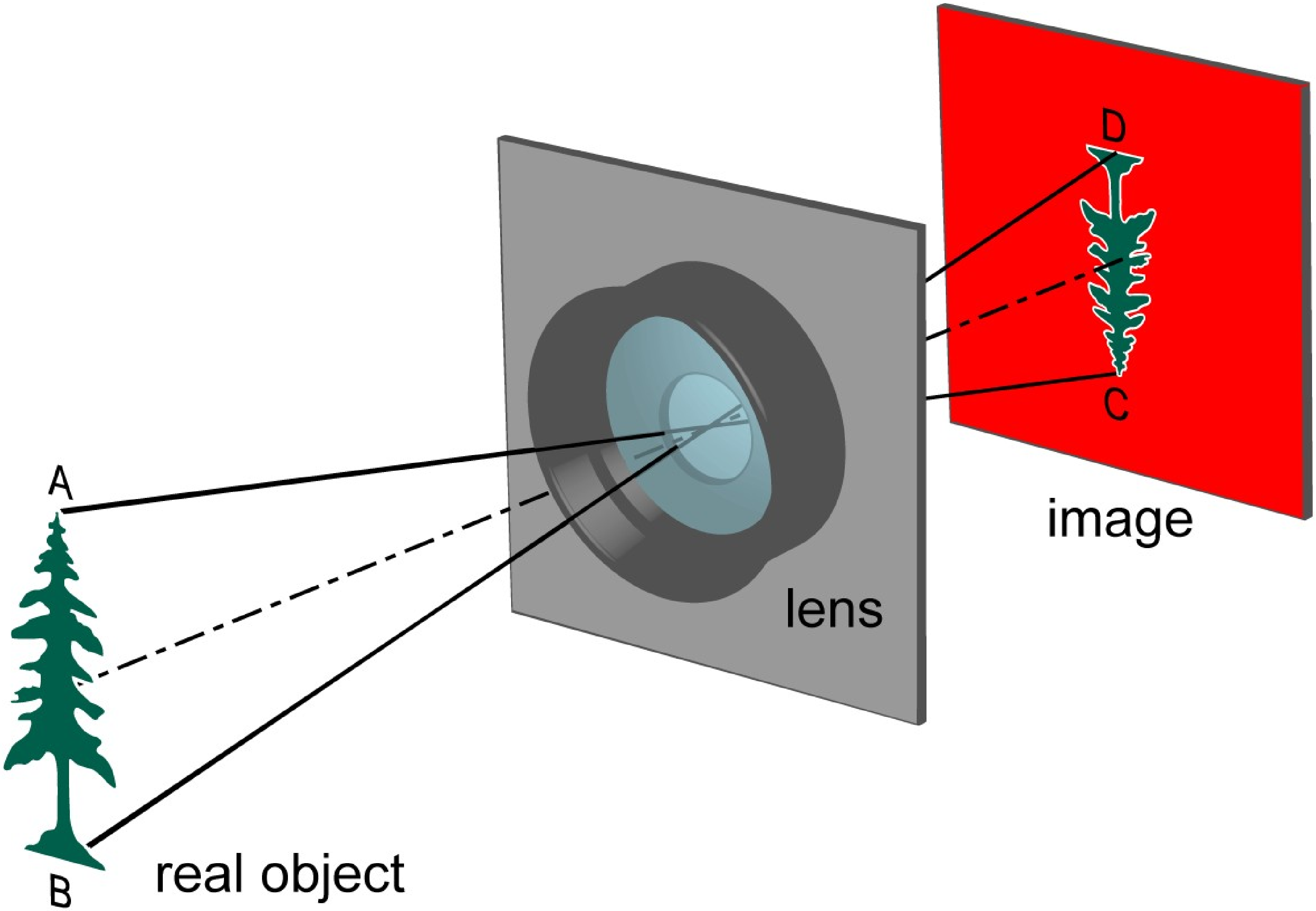
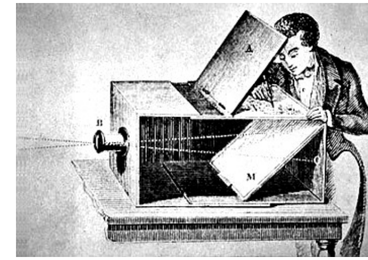


Image Formation in a Camera



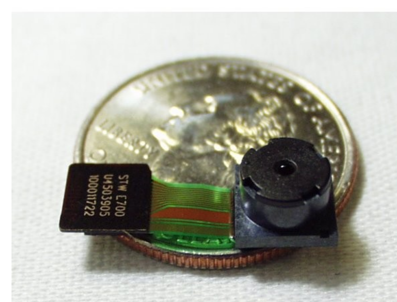
Advances in the Image Recording Process

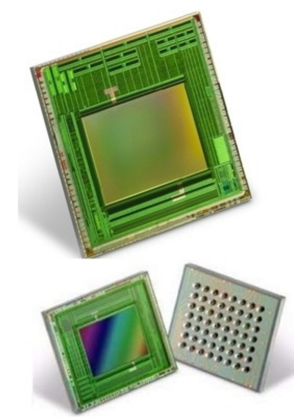
- Images recorded by hand (1015-1900)



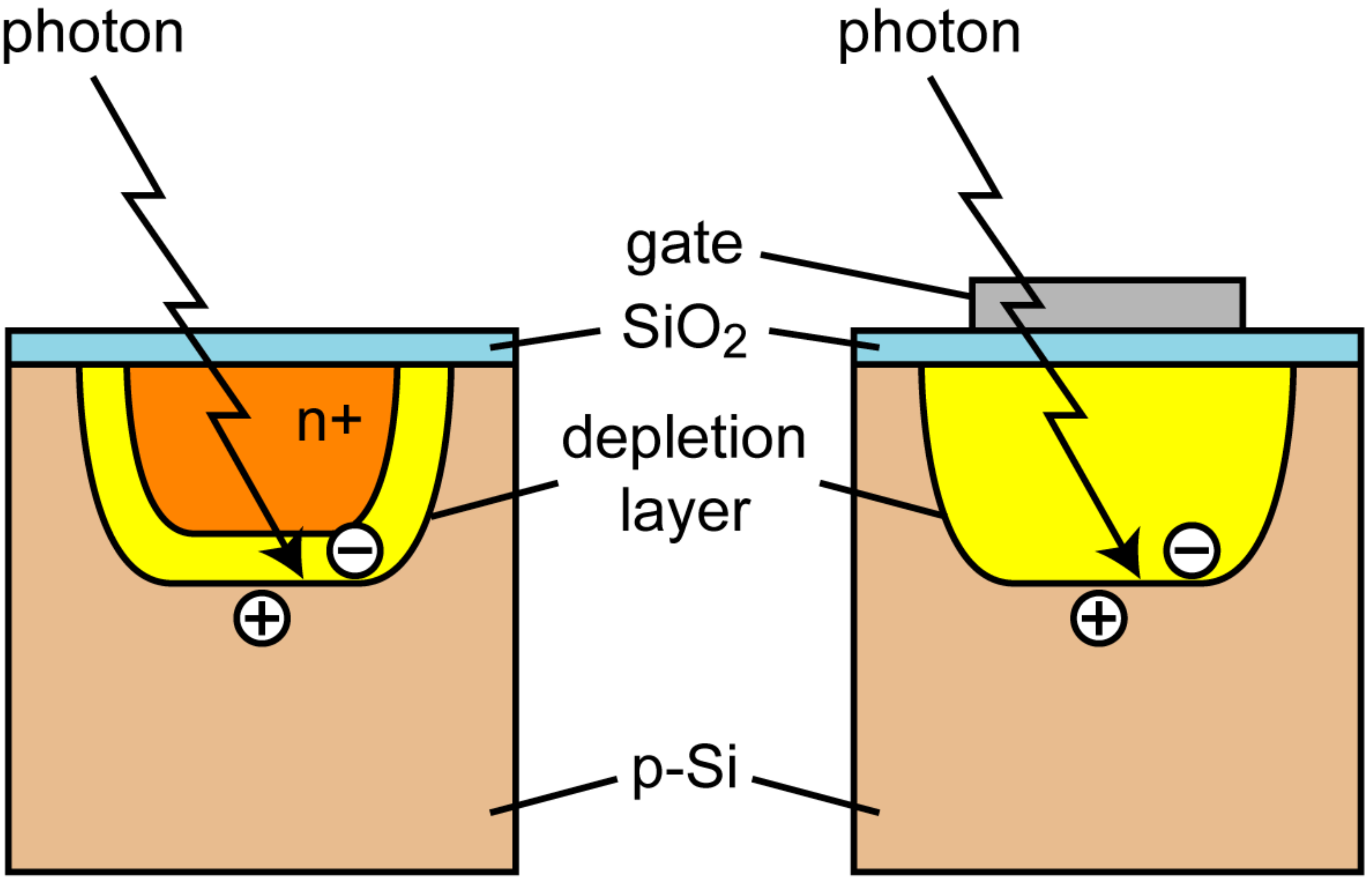
- Images recorded by film (1829-2000)

- Images recorded by semiconductor (1974-present)





Solid-State Photon Conversion



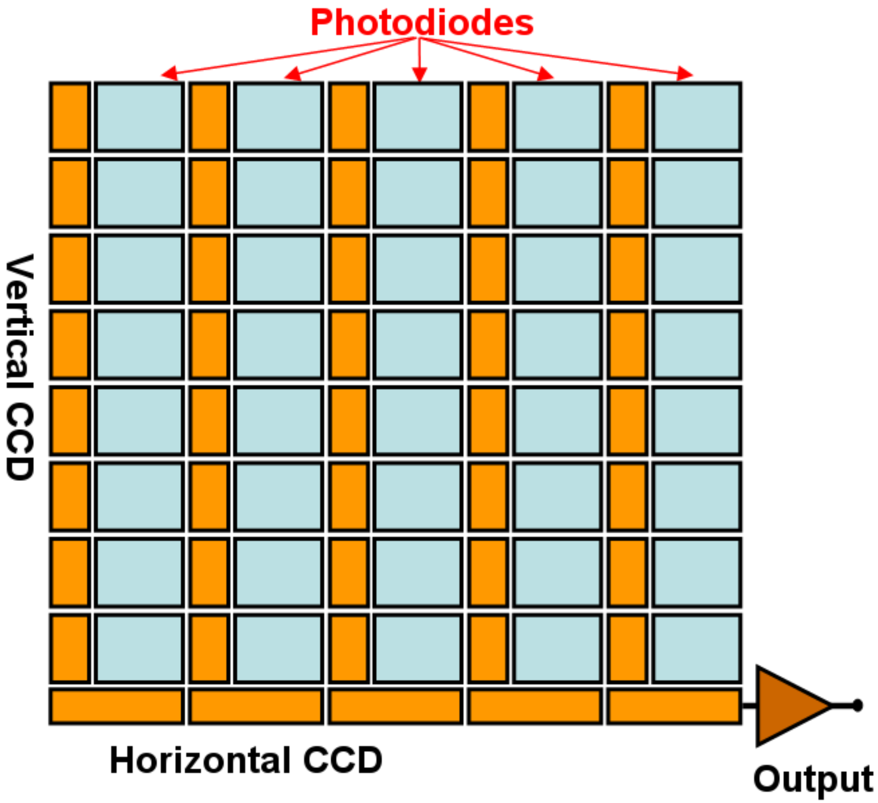
pn junction

Voltage-induced junction

**** A. Theuwissen, Solid-State Imaging with CCDs, p. 111***

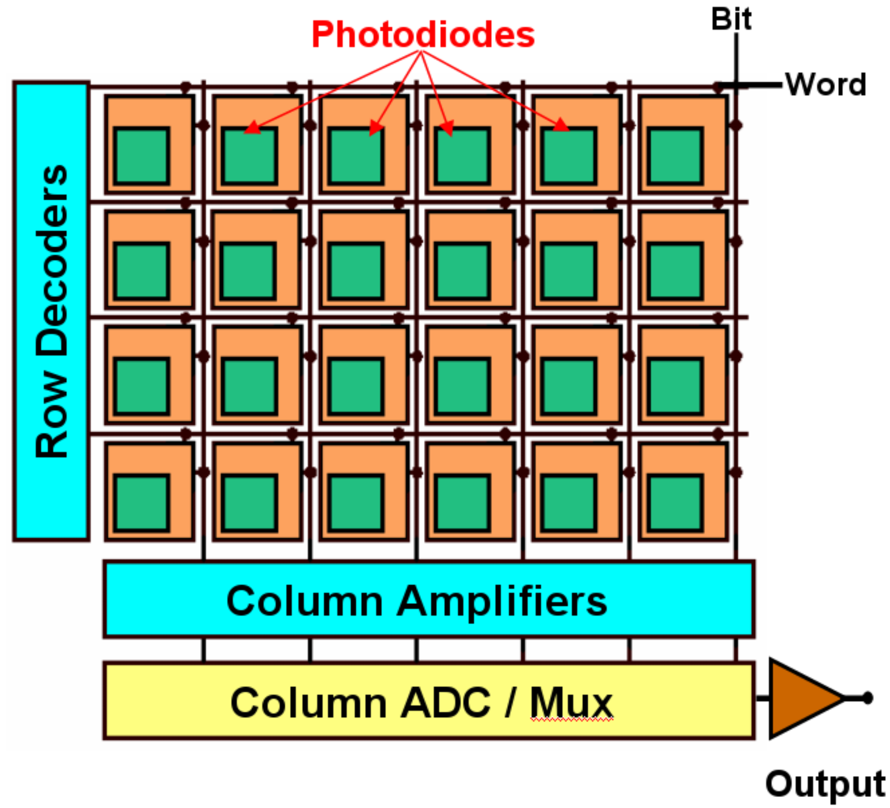
CCD and CMOS Comparison

Interline Transfer CCD



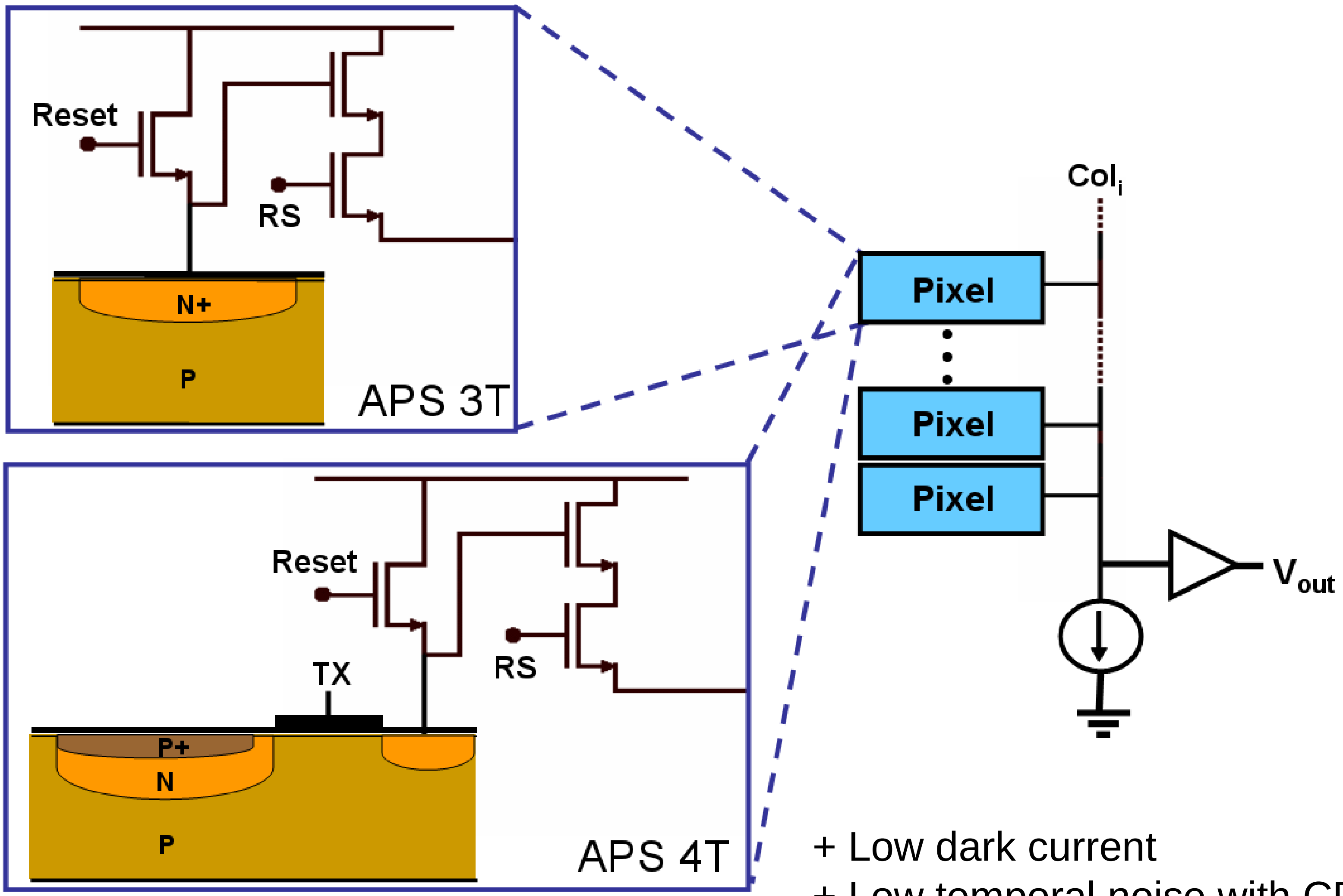
+ Low dark current, low non-uniformity
- Minimal integration of circuits, slow readout, high power

CMOS



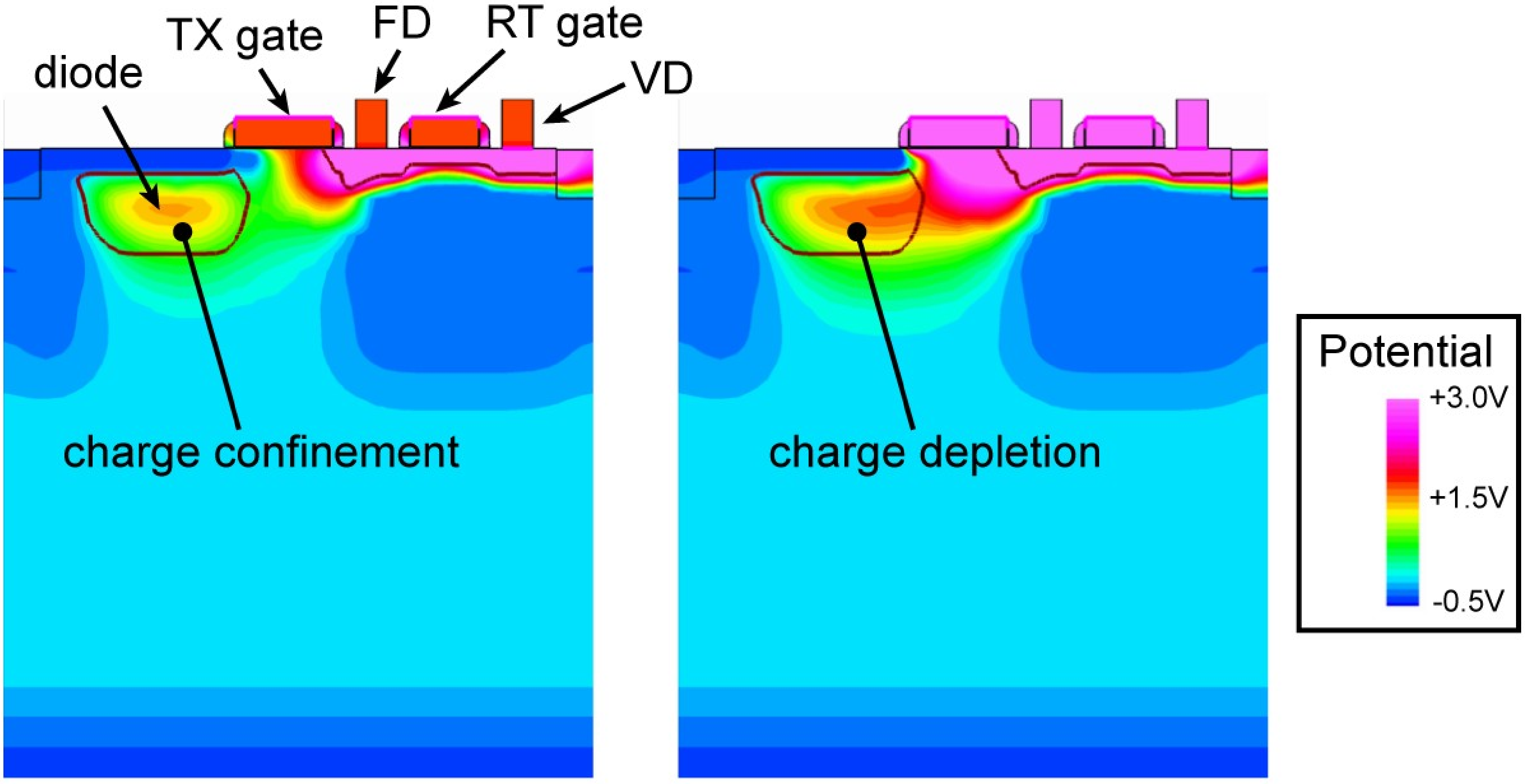
+ Integration, fast readout, low power
- Higher dark signal, non-uniformity

CMOS Active Pixels



+ Low dark current
+ Low temporal noise with CDS
+ Allows for readout multiplexing

4T Buried Diode Operation



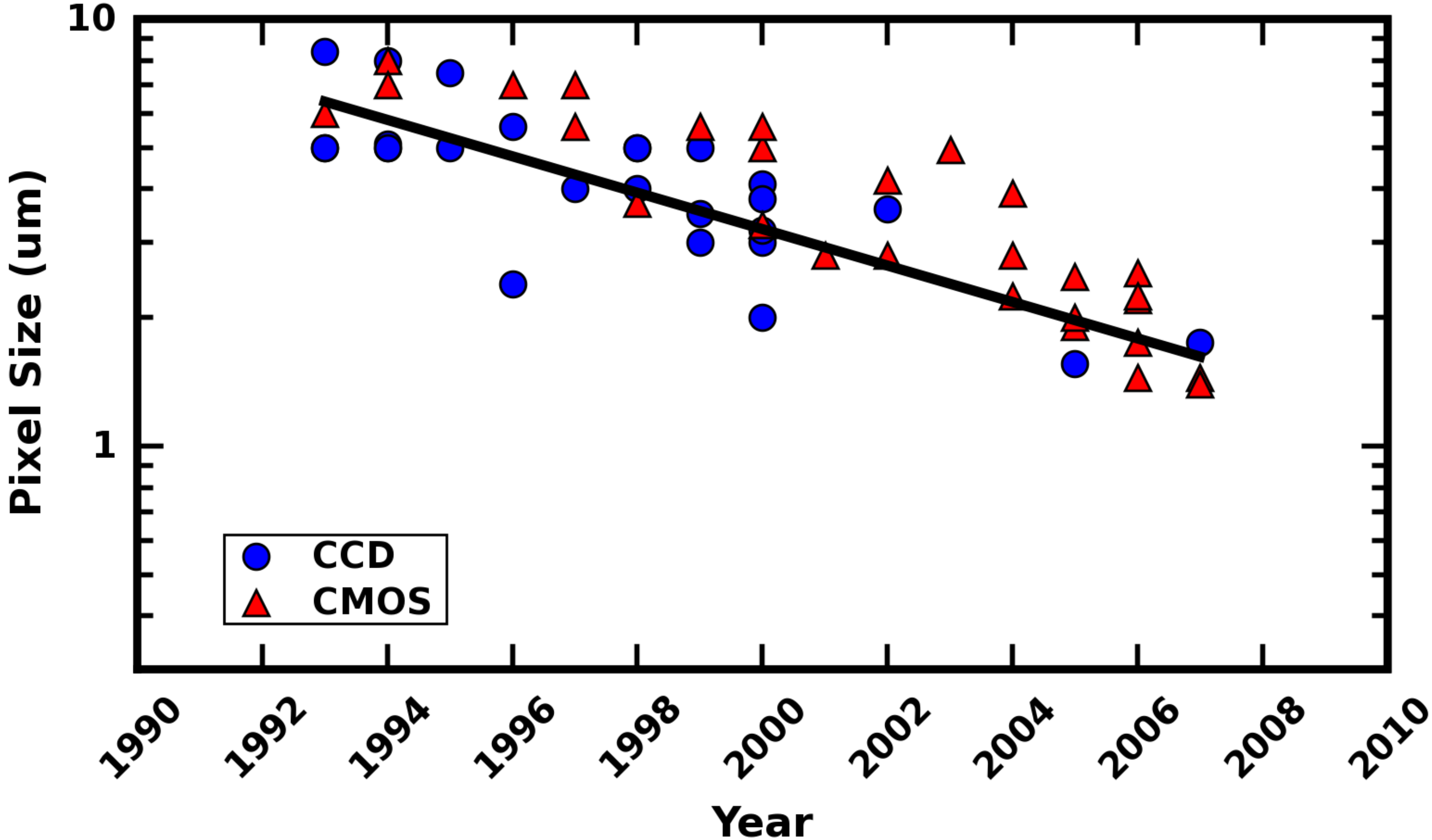
Exposure

Readout

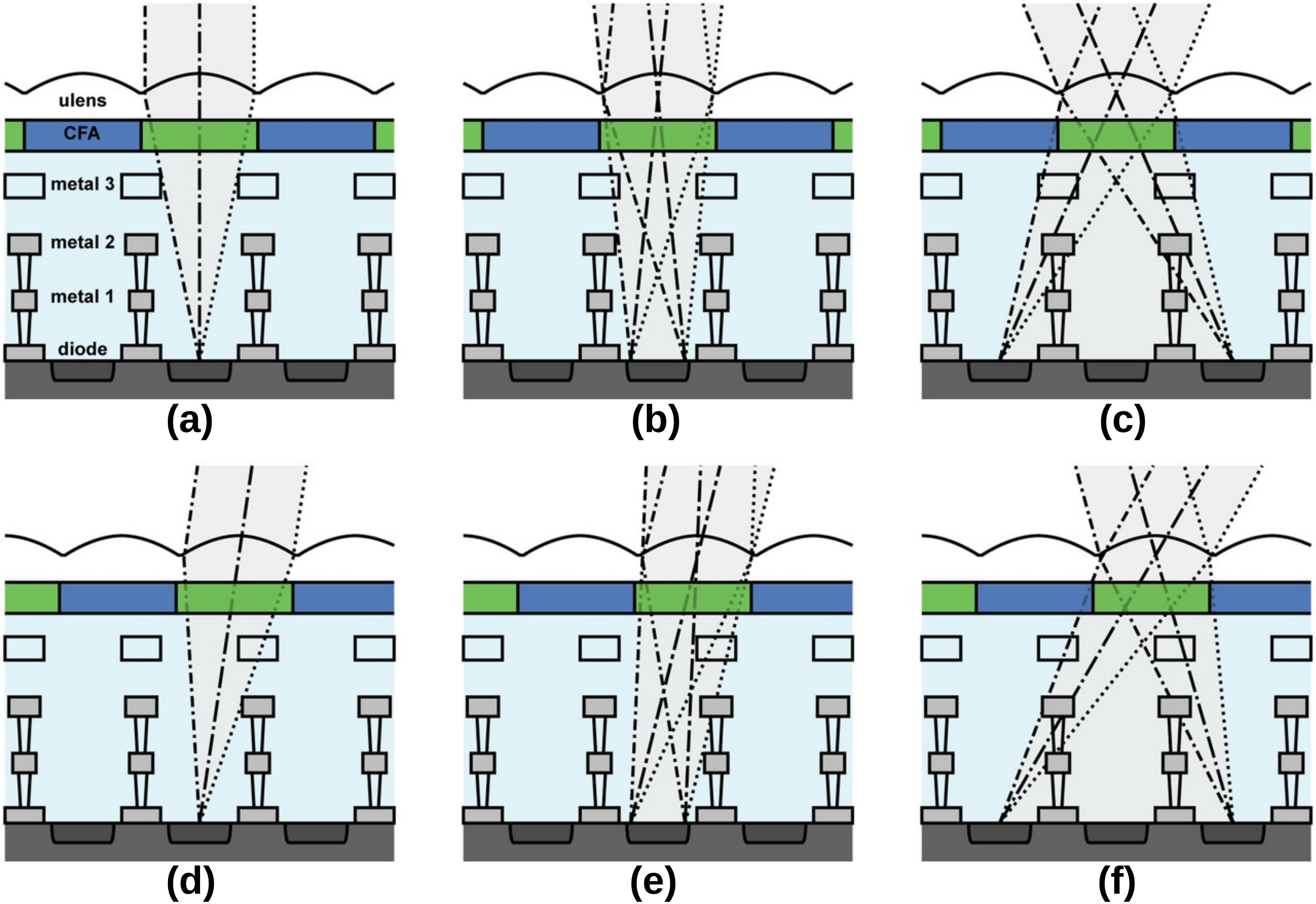
Recent Pixel Scaling

- Increase spatial resolution
- Decrease format size

Pixel Sizes reported at IEDM, ISSCC, IISW

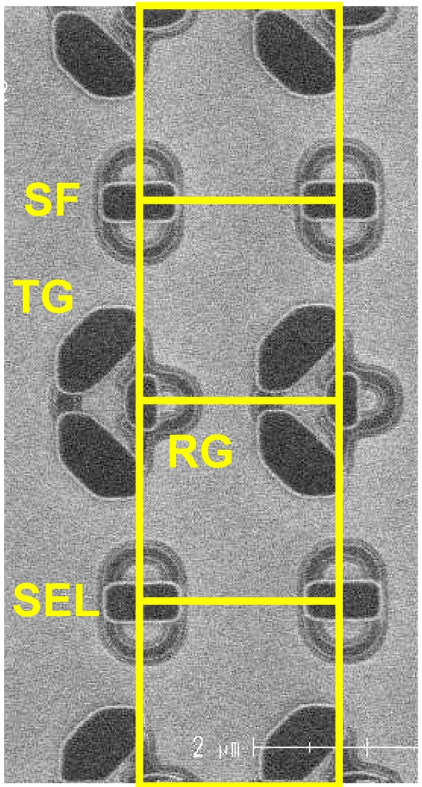


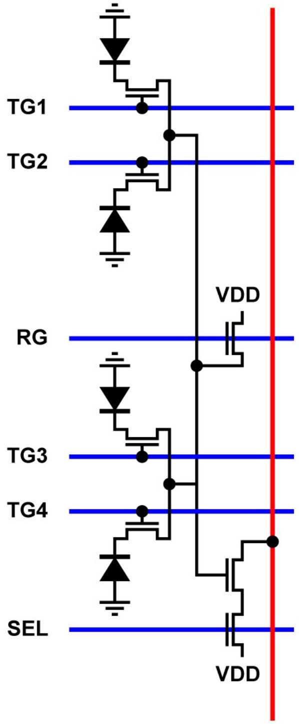
Ray Diagrams for CMOS Pixel



Recent Pixel Scaling Technology

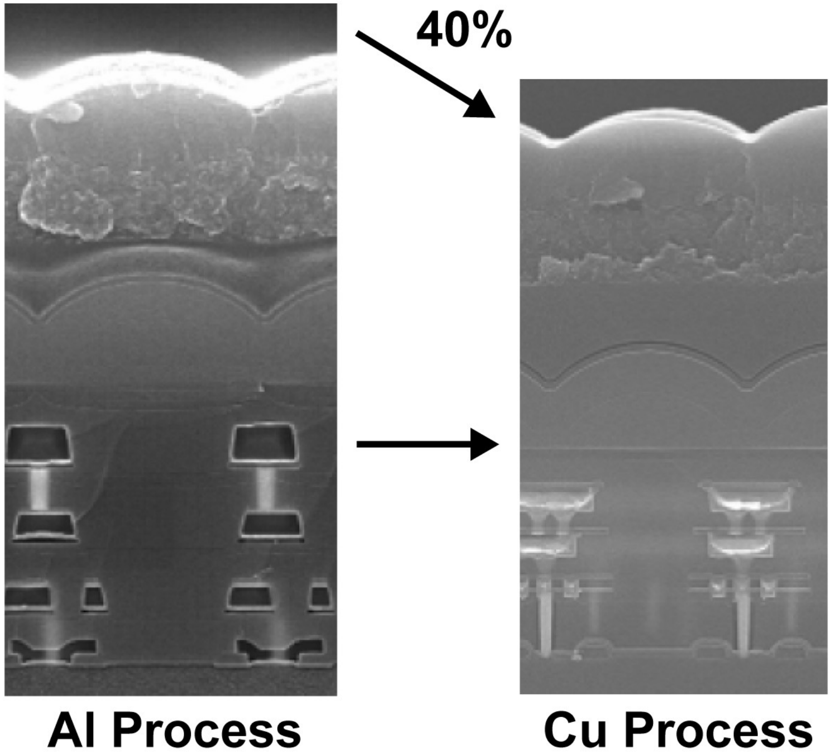
4T sharing





*** J. Kim, J. Shin, C.R. Moon, et. al., IEDM 2006, p123-126**

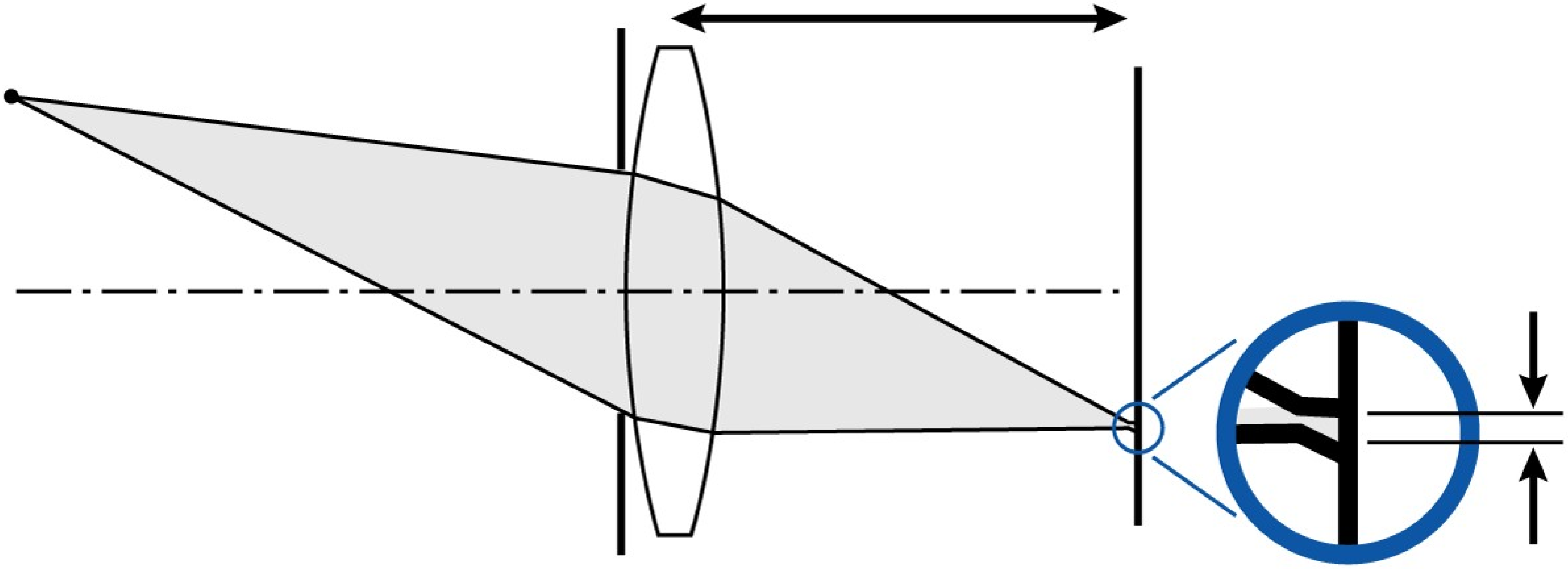
Stack height reduction



*** H. Sumi, IEDM 2006, p119-122**

Spot Size Limitation

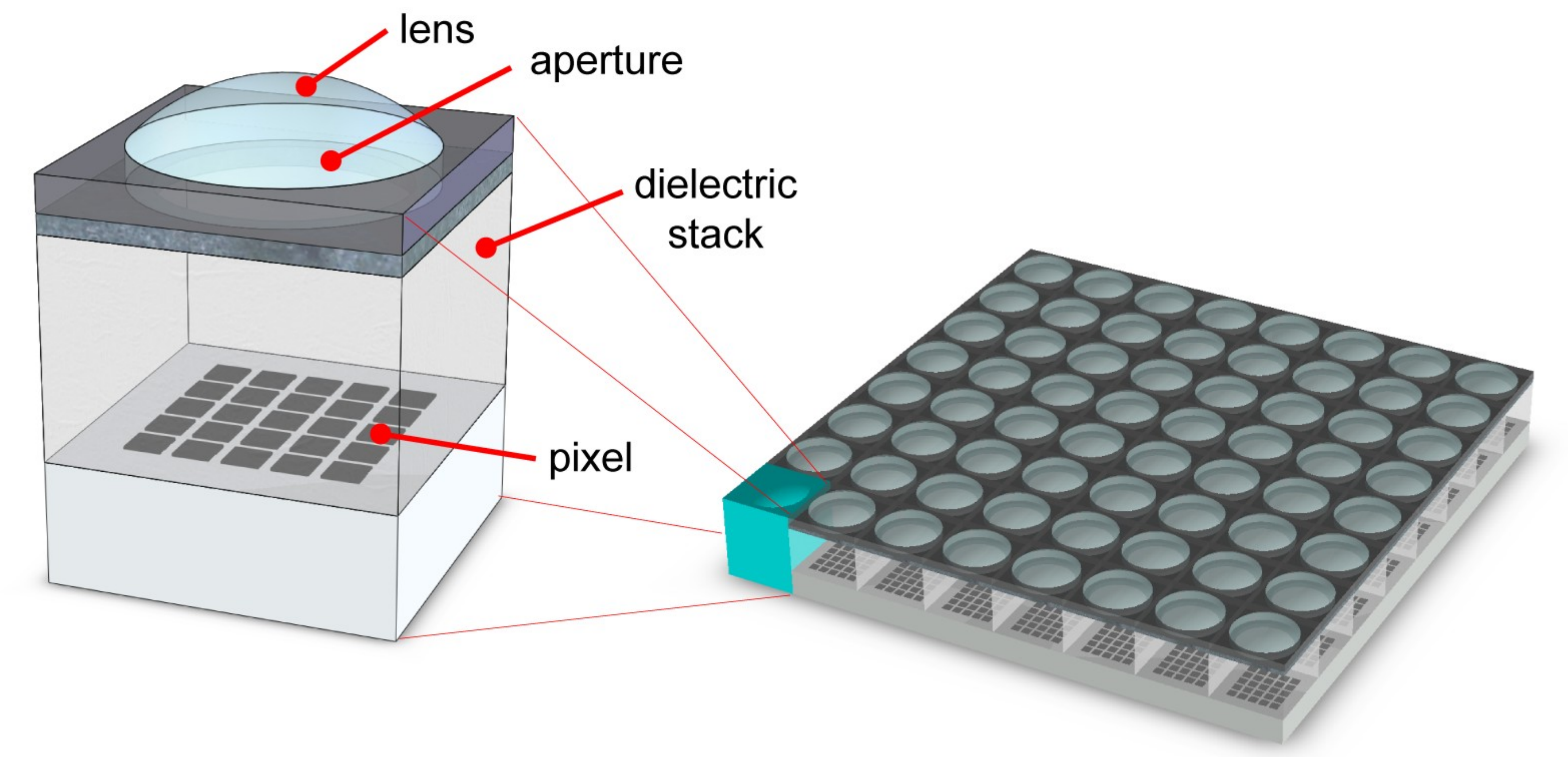
- Point in object space is focused to a small spot in focal plane
- Spot size is limited and dependent on:
  - Relative size of the aperture
  - Aberrations of lens
  - Wavelength of the source



Outline

- Multi-Aperture architecture
- Detailed operation
  - FT-CCD array
  - Multi-Aperture array
  - Column ADC
- Results
- Summary

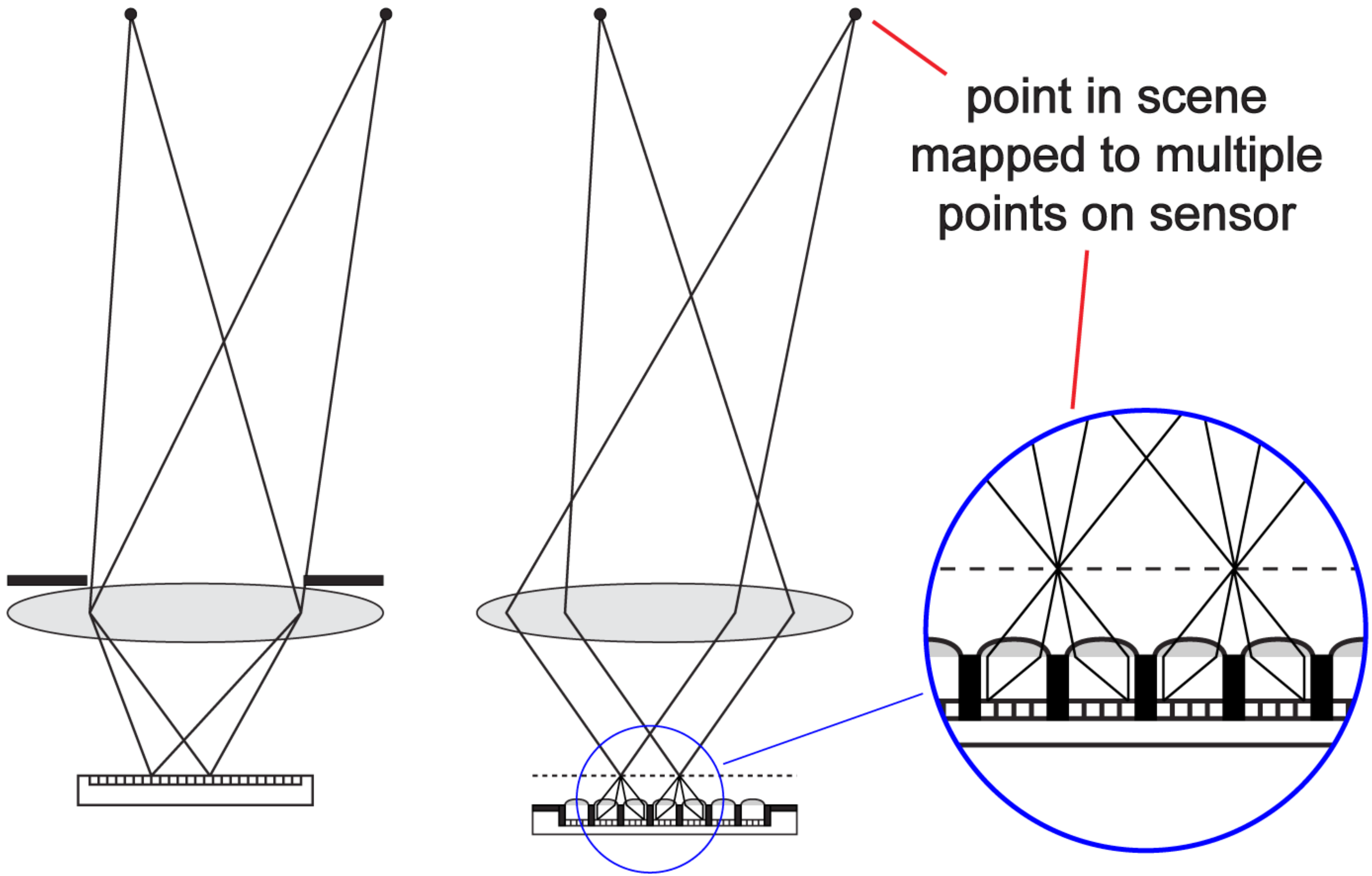
Multi-Aperture Image Sensor



Imager subarray with integrated optics

Imager subarrays integrated to form multi-aperture array

Conventional vs. Multi-Aperture

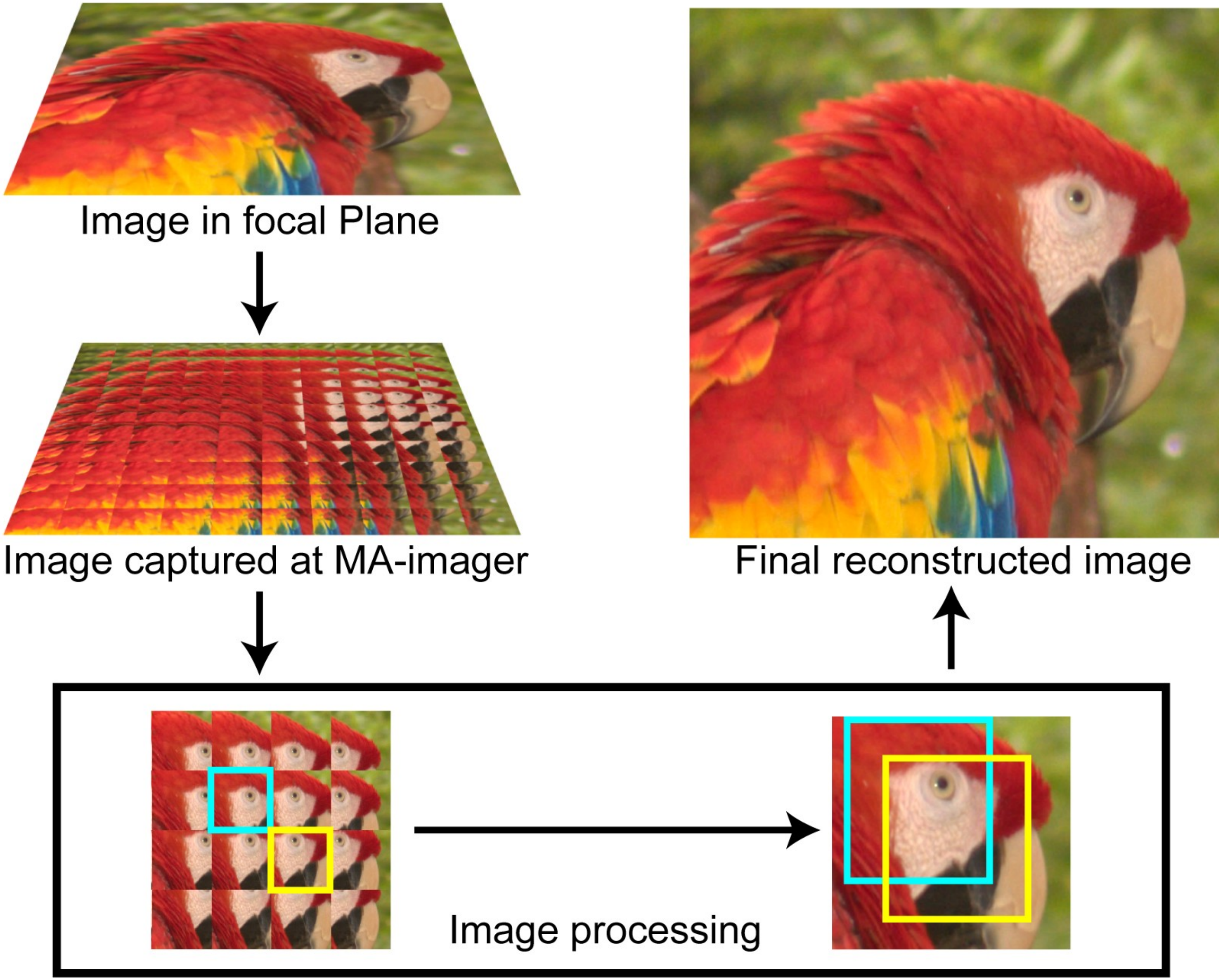


Conventional imaging

Multi-Aperture imaging

* K. Fife, A. El Gamal and H.-S. P. Wong, CICC 2006, p281-284

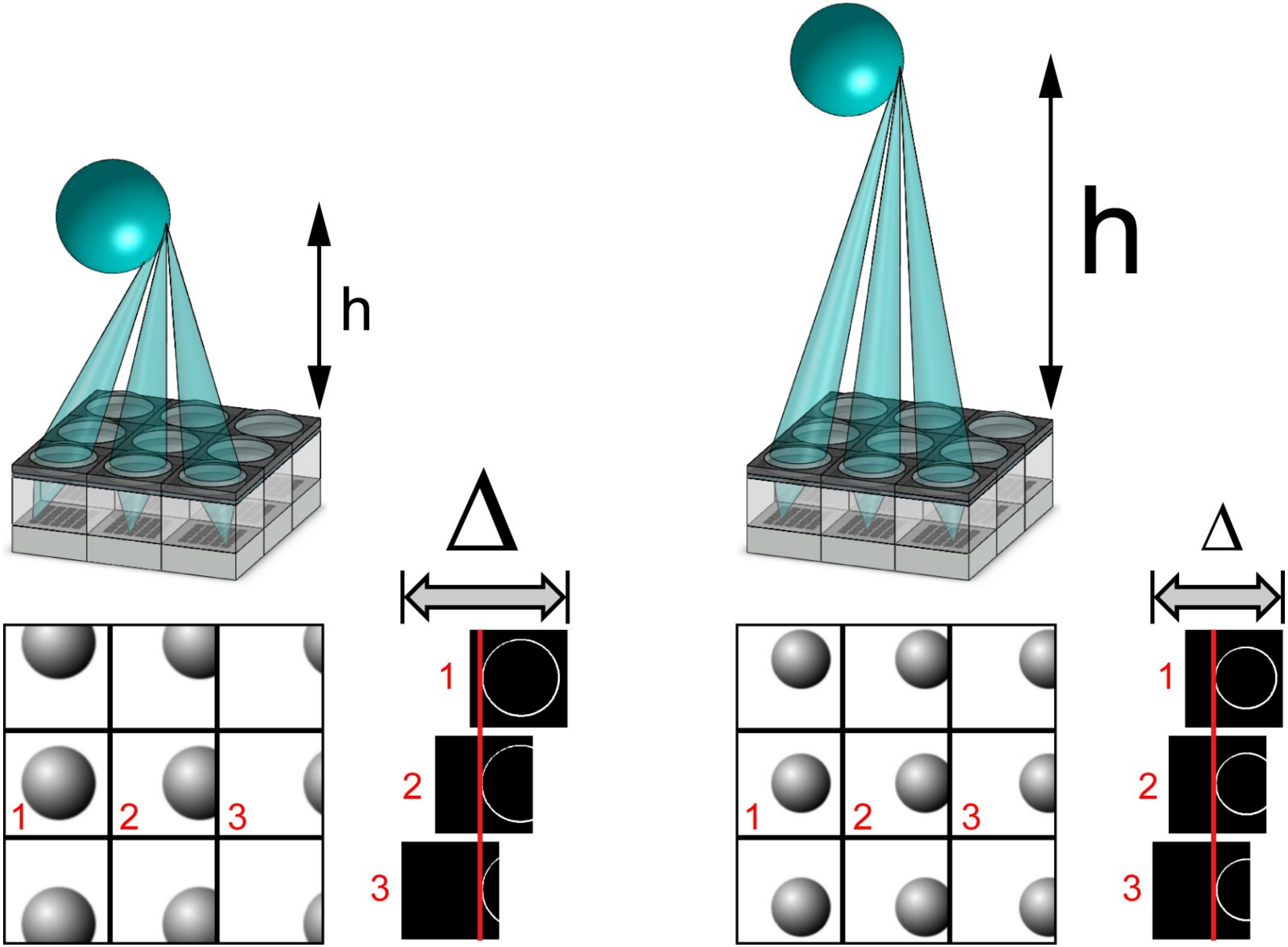
Multi-Aperture Imaging



Benefits of Multi-Aperture Imaging

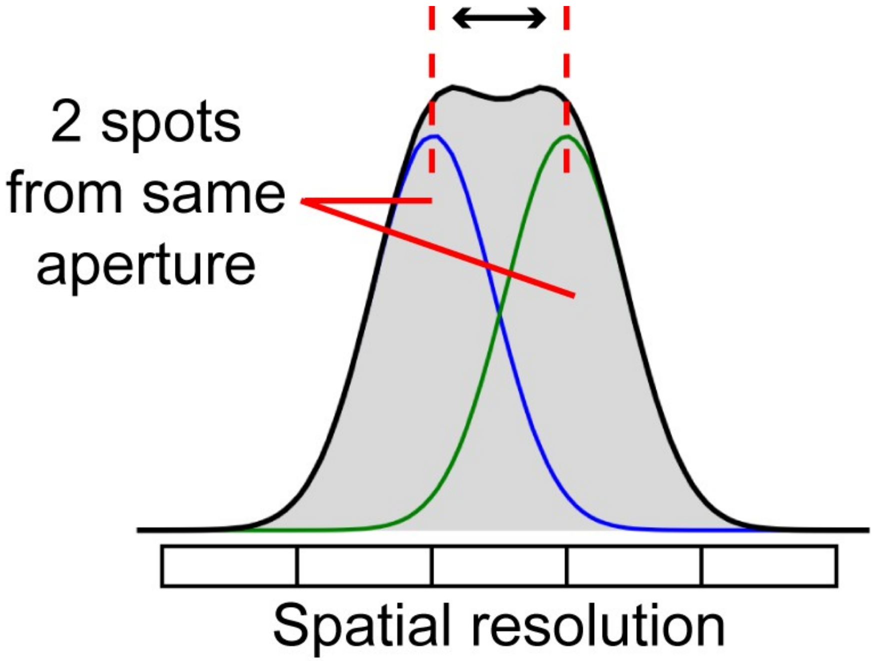
- Capture depth information
- Close proximity imaging
- Achieve better color separation
- Reduce requirements of objective lens
- Increase tolerance to defective pixels

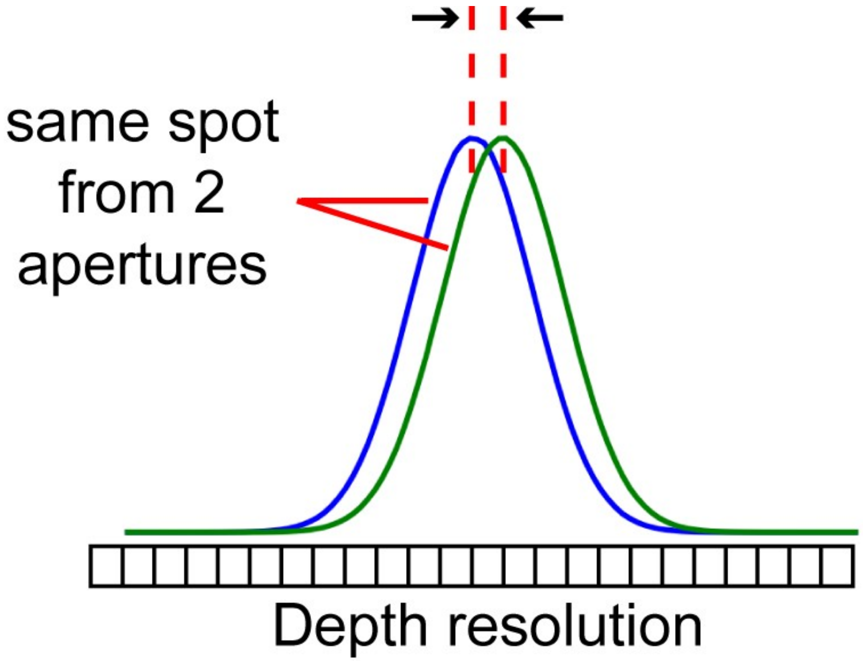
Depth from Multi-Aperture



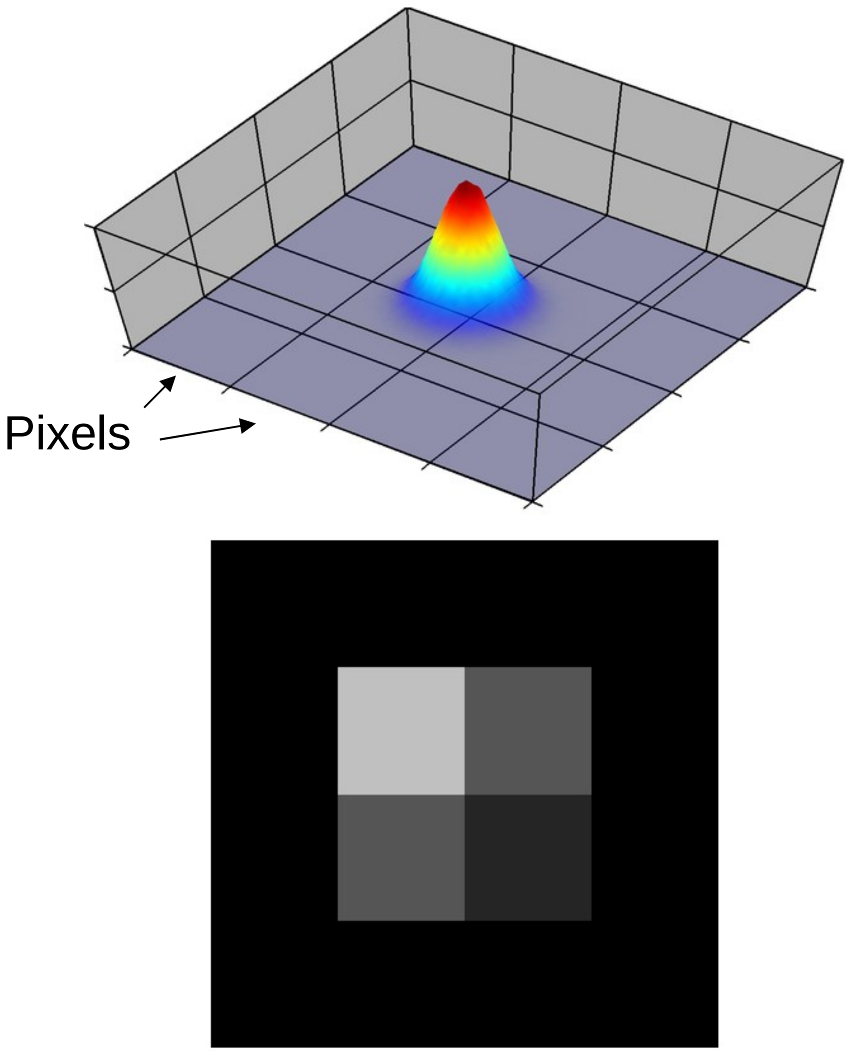
Why Use Small Pixels?

- Depth resolution improves with pixels smaller than the spot size
- Spatial resolution is limited by the spot size
- Depth resolution is limited by accuracy in localization of the spot

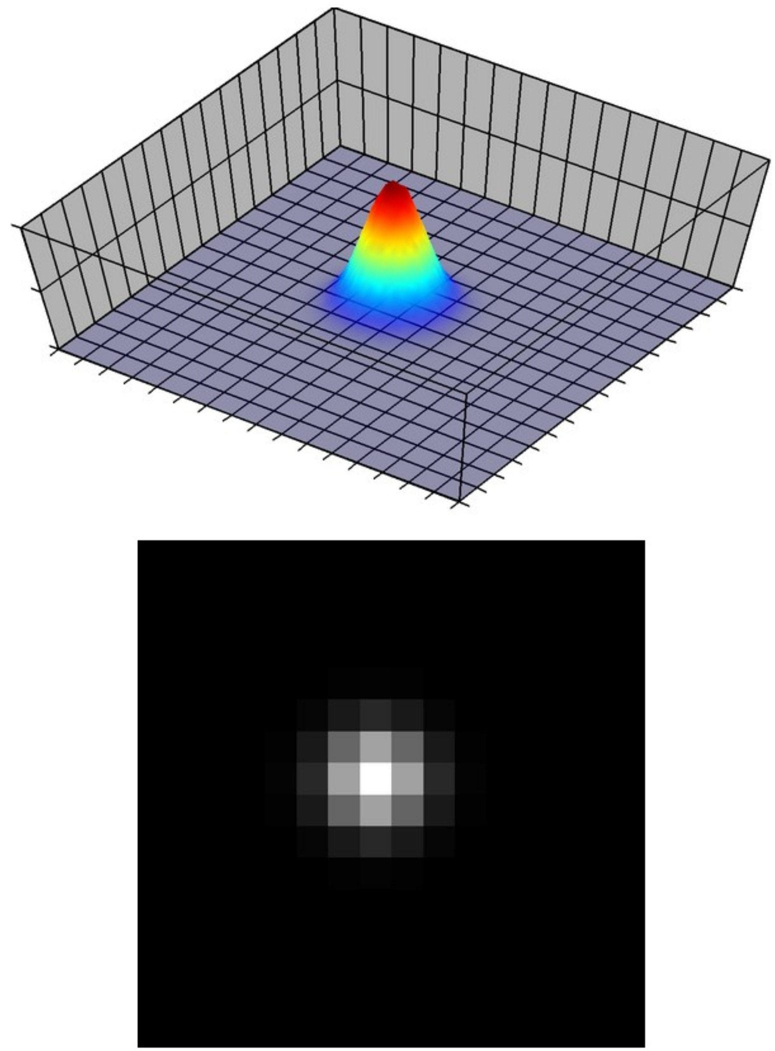




Feature Localization vs. Pixel Size



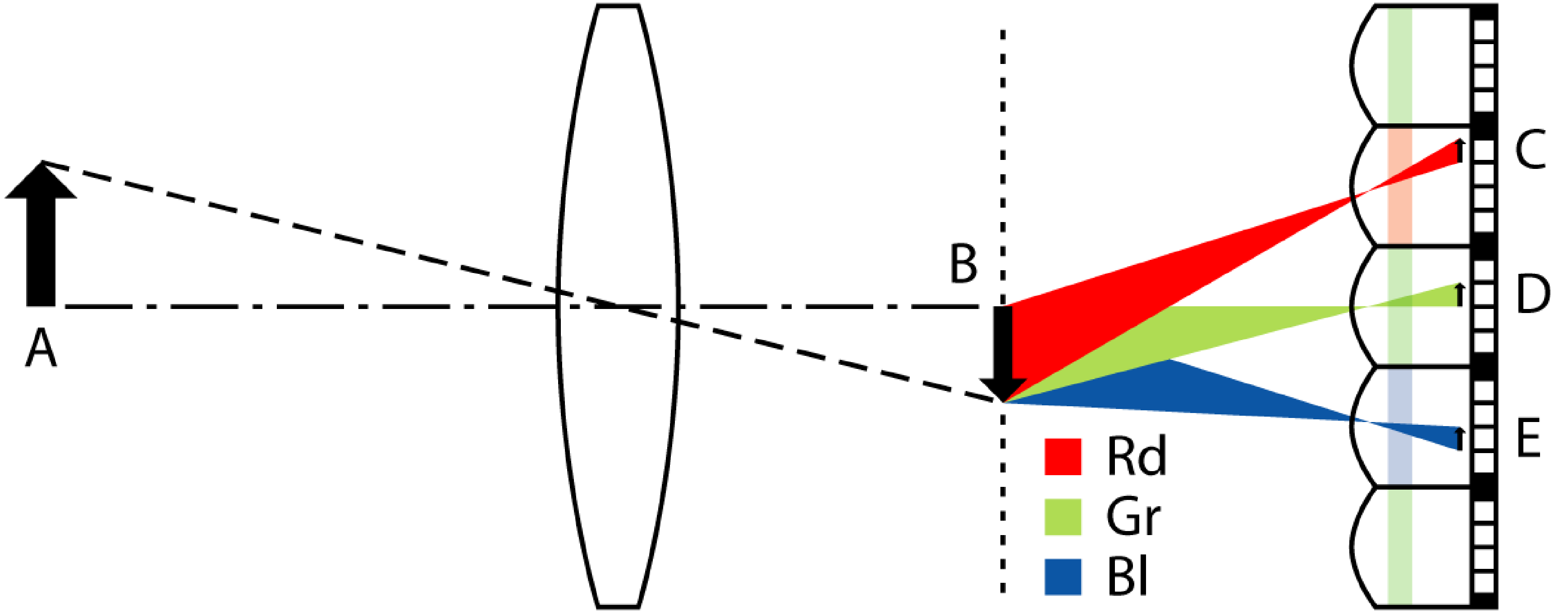
Poor location accuracy



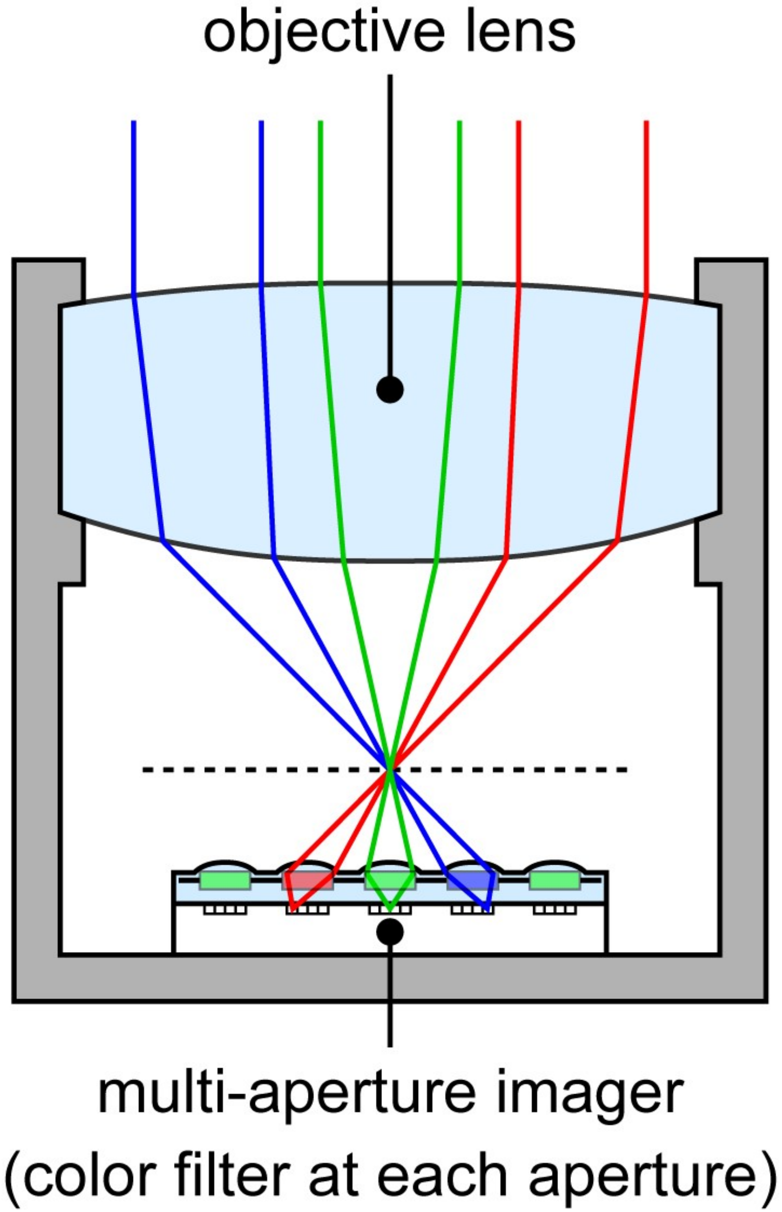
High location accuracy

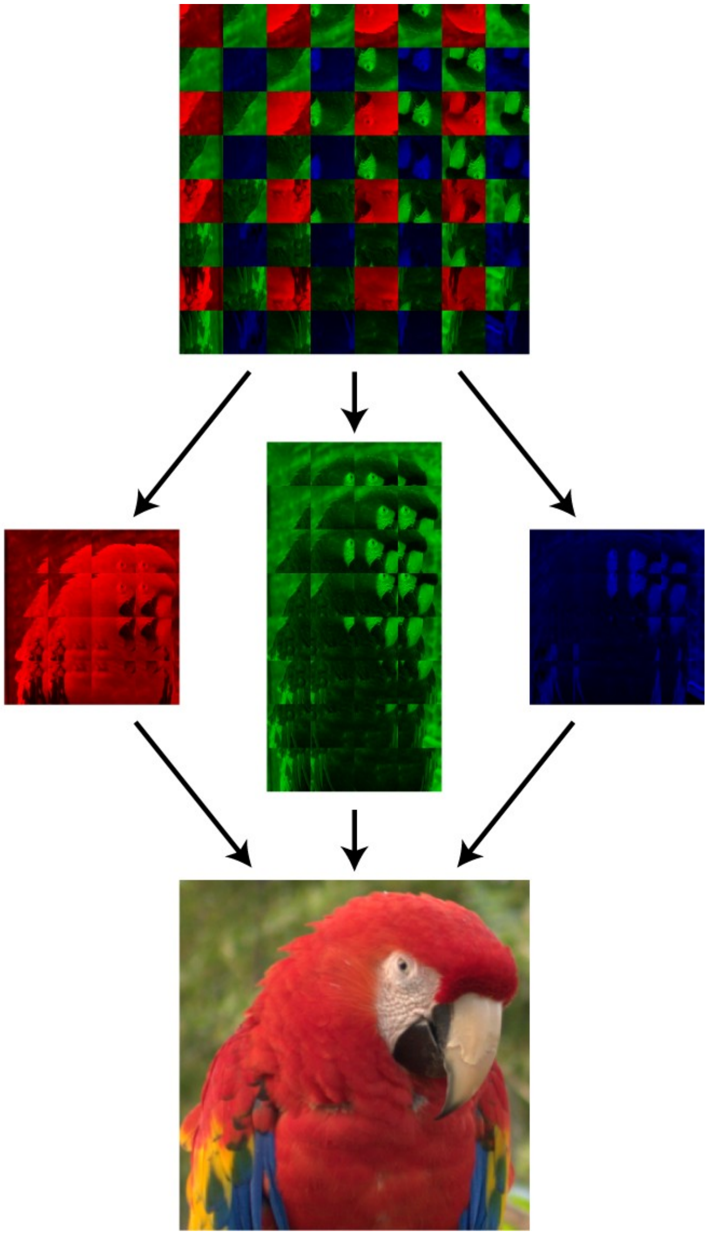
Color Separation with Multi-Aperture

- Color filter placed over each subarray of pixels rather over each individual pixel

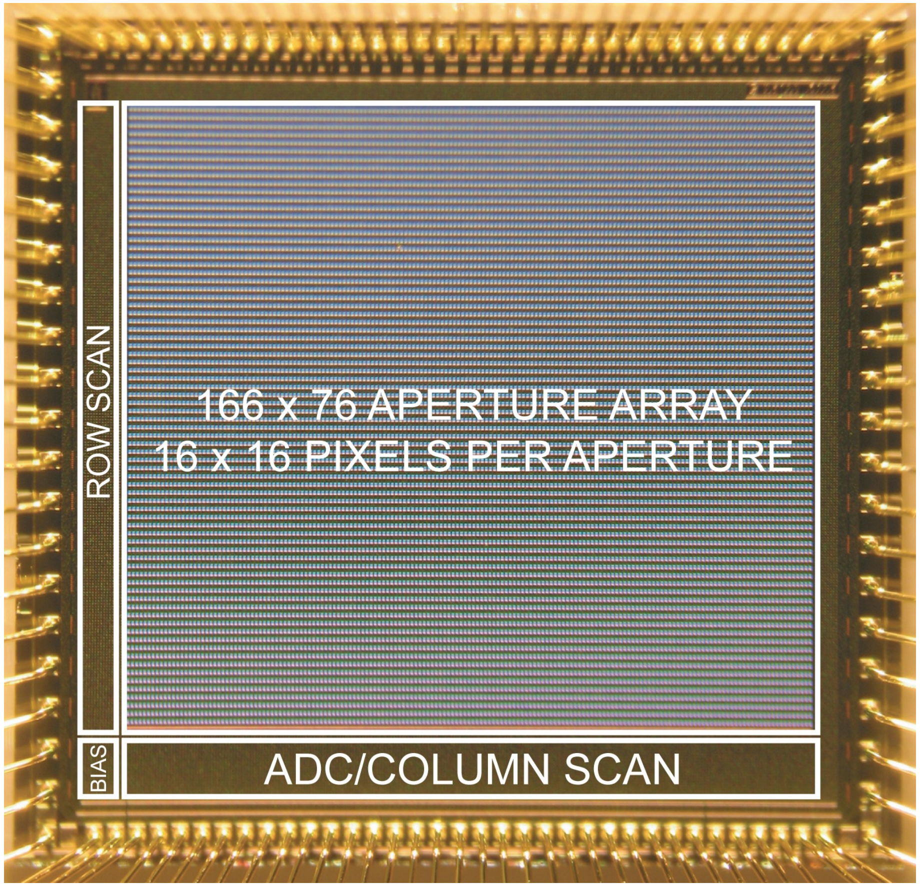


Color Imaging with Multi-Aperture





Fabricated Multi-Aperture Imager

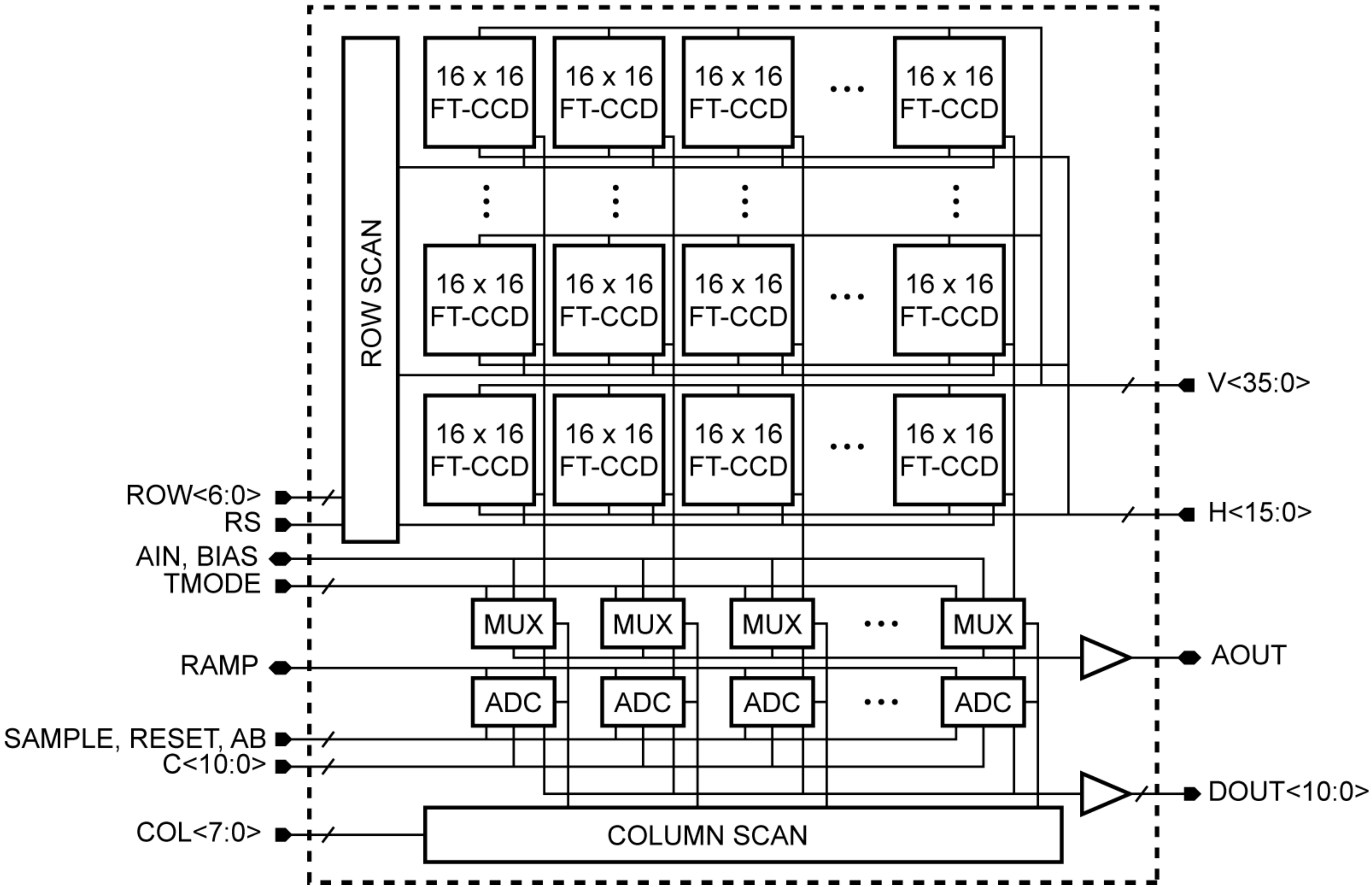


- 0.11μm CMOS (TSMC)
- Chip size: 3.0 x 2.9mm^2
- 166 x 76 aperture array
- 16 x 16 pixel FT-CCD per aperture
- Pixel size: 0.7 μm
- Max frame rate: 15fps
- ADC resolution: 10 bit
- Power: 10.45mW

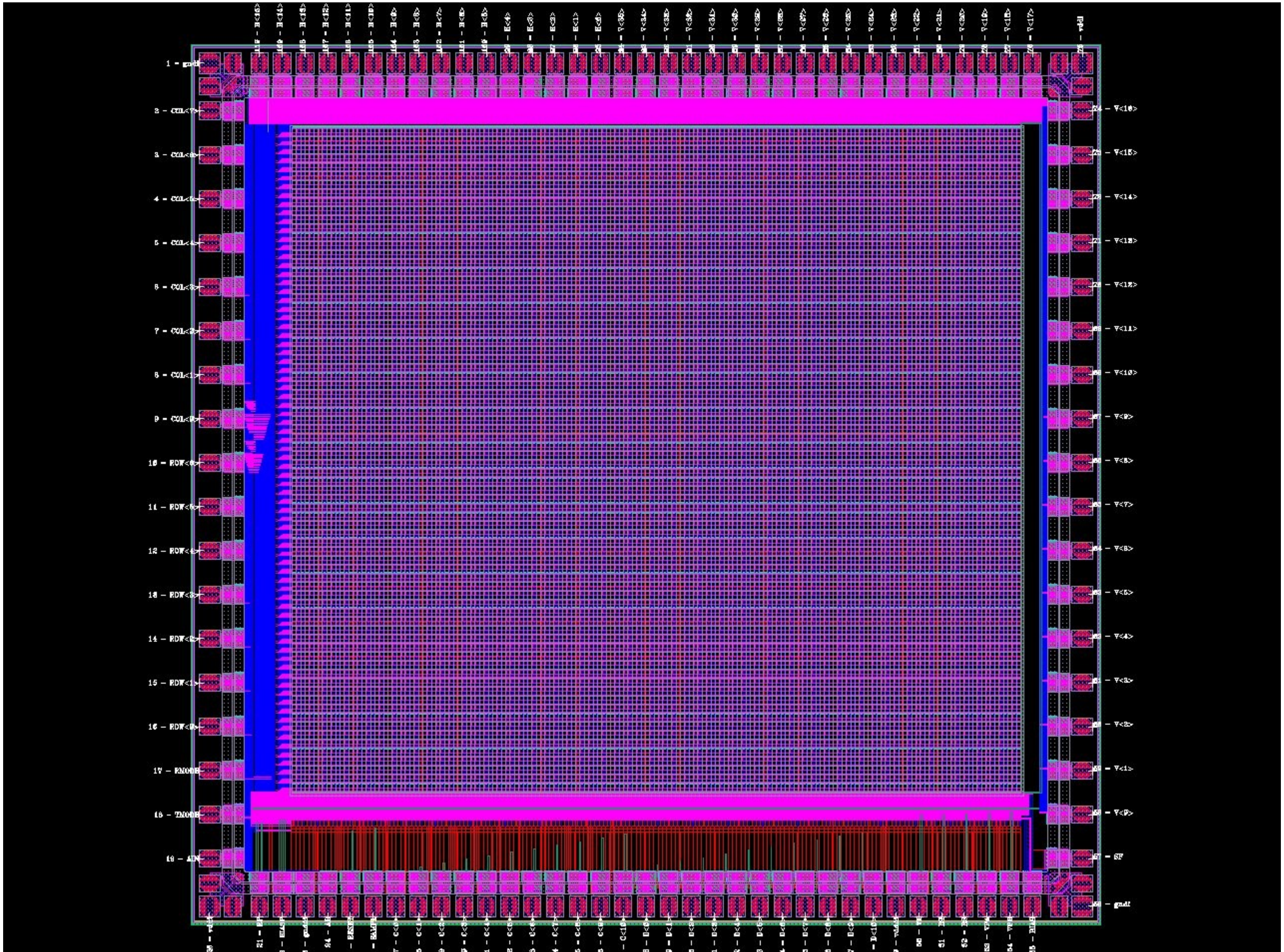
* Local optics are not integrated on this chip.

** K. Fife, A. El Gamal and H.-S. P. Wong, ISSCC 2008, p48-49*

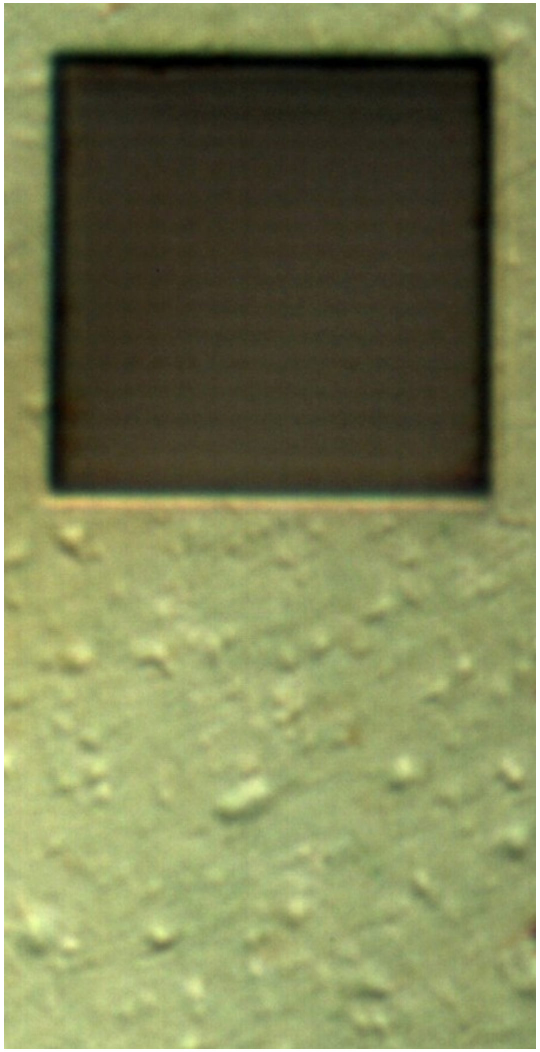
Block Diagram of Fabricated Chip

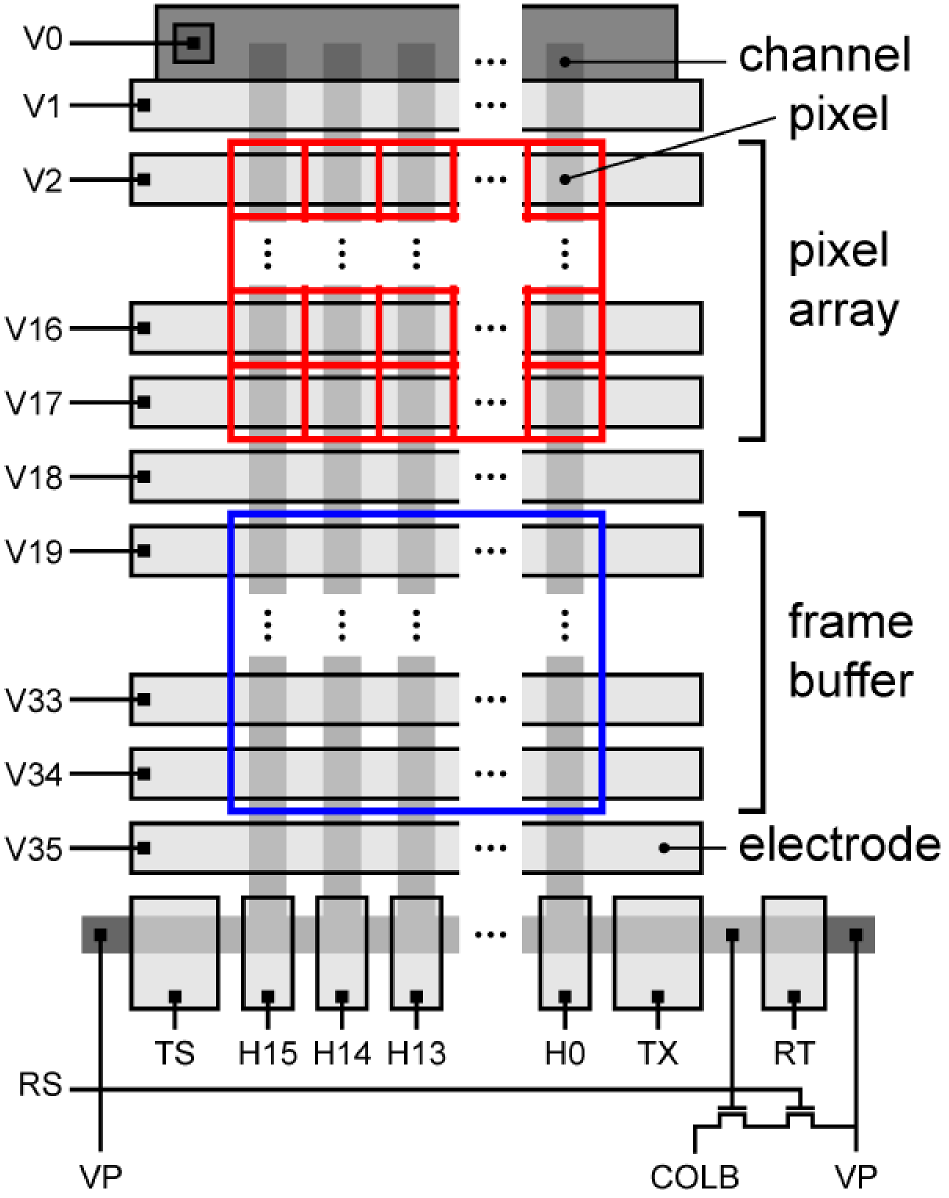


Layout Masks for Chip



16 x 16 FT-CCD schematic

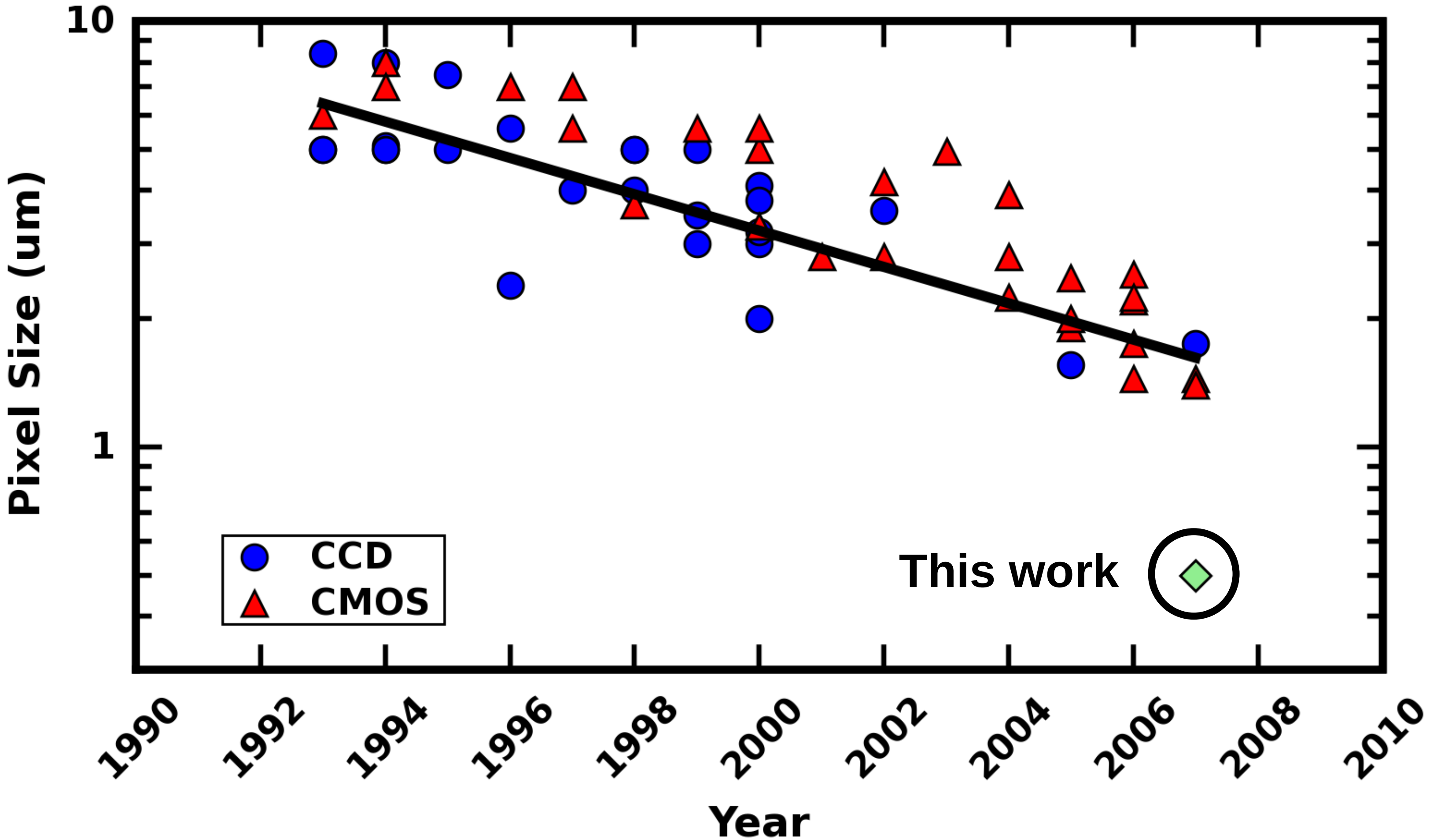




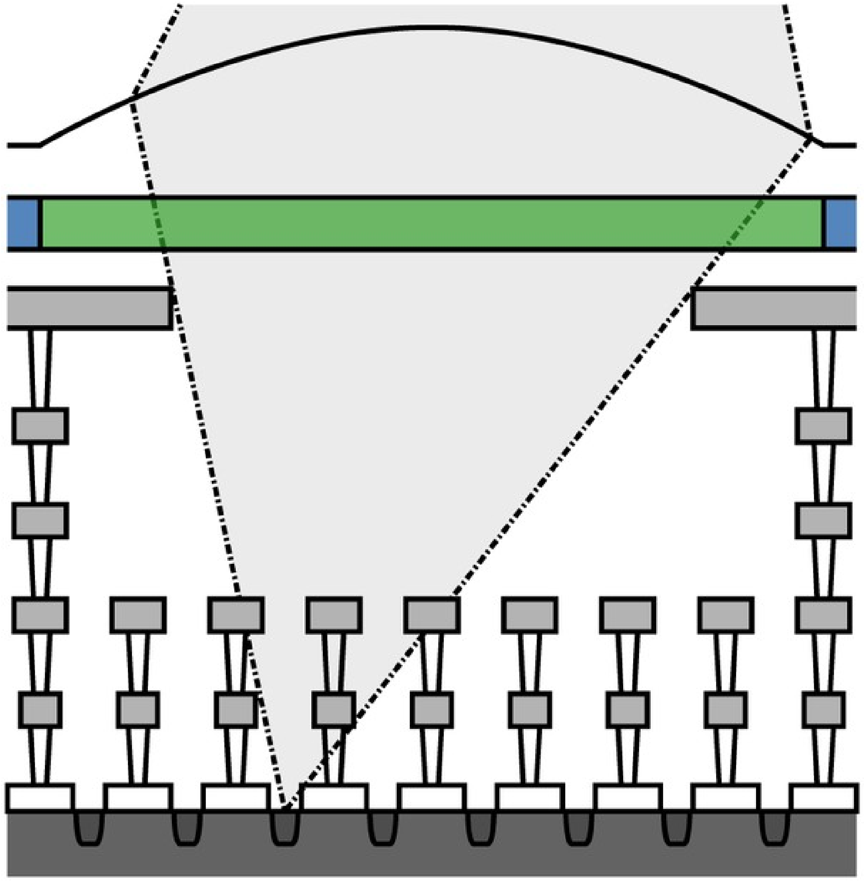
Relative Pixel Size for This Work

- Increase spatial resolution
- Decrease format size

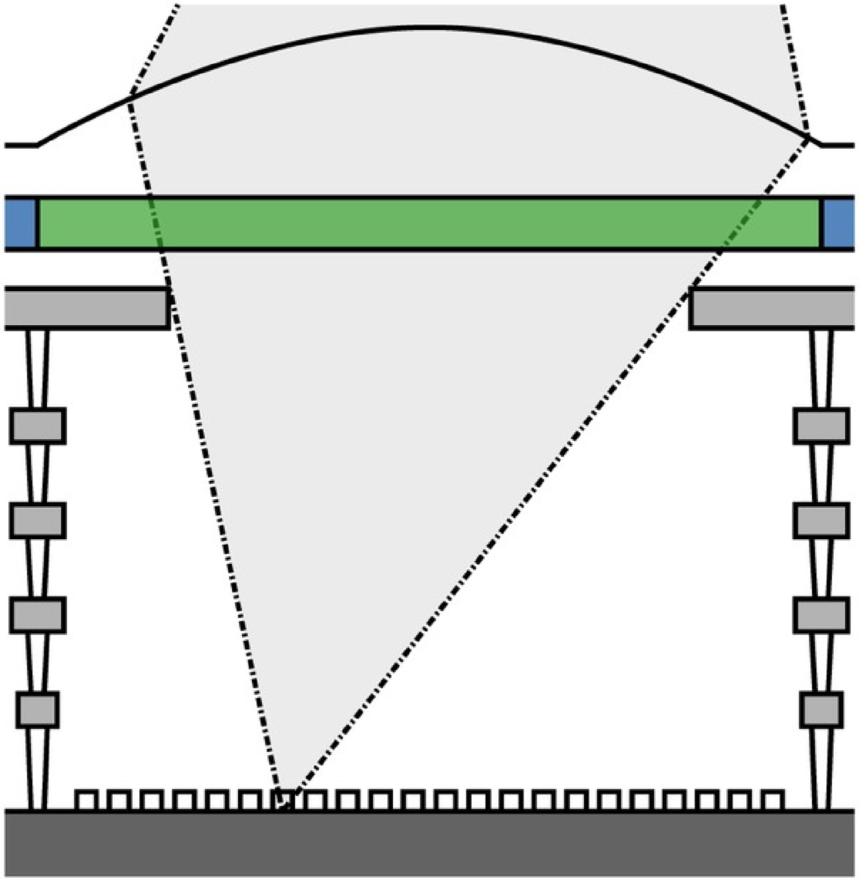
Pixel Sizes reported at IEDM, ISSCC, IISW



Multi-Aperture Optical Stack

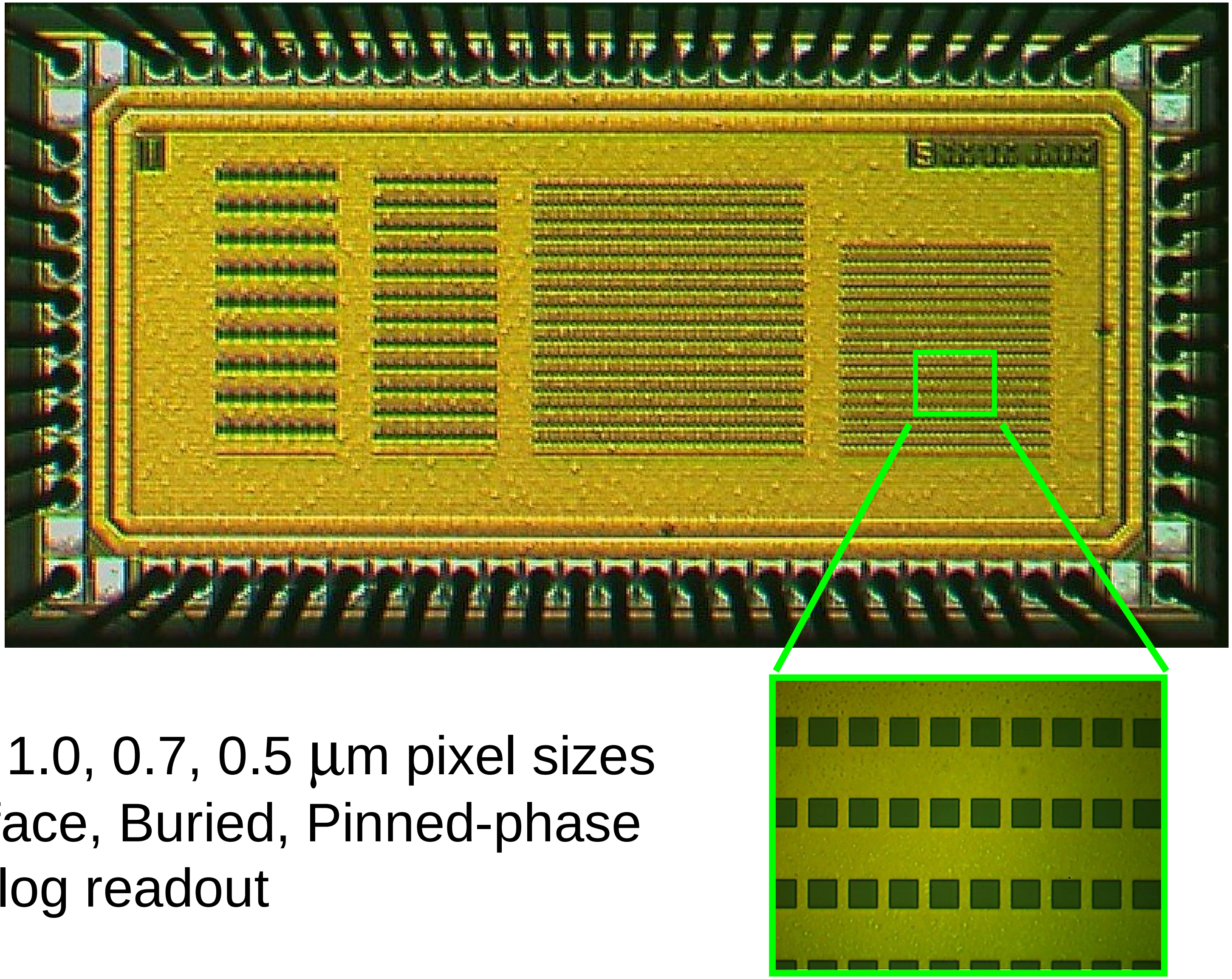


Using CMOS active pixels



Using FT-CCD pixels

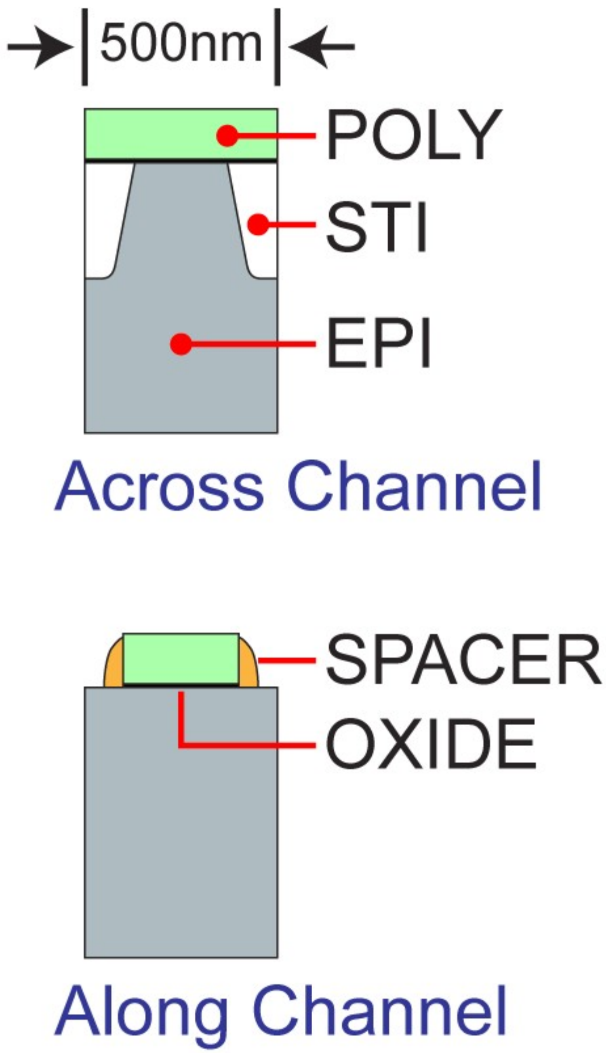
FT-CCD Test Chip

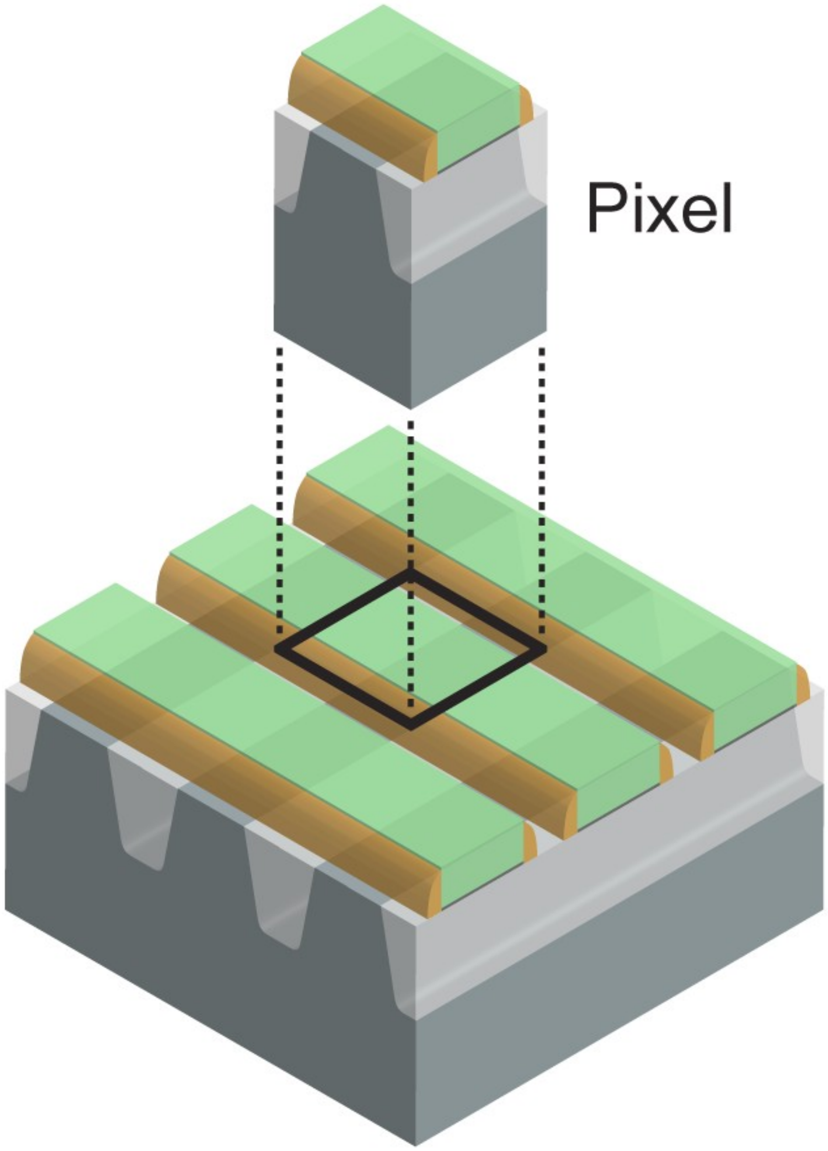


- 1.4, 1.0, 0.7, 0.5 μm pixel sizes
- Surface, Buried, Pinned-phase
- Analog readout

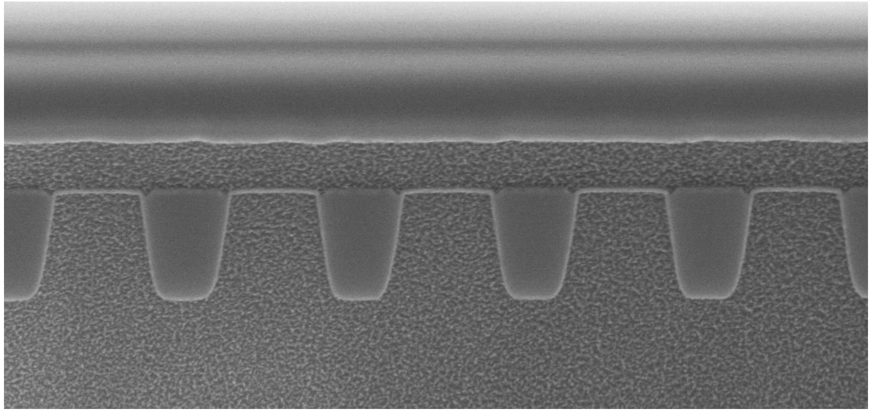
** K. Fife, A. El Gamal and H.-S. P. Wong, IEDM 2007, p1003-1006*

The 0.5µm Pixel

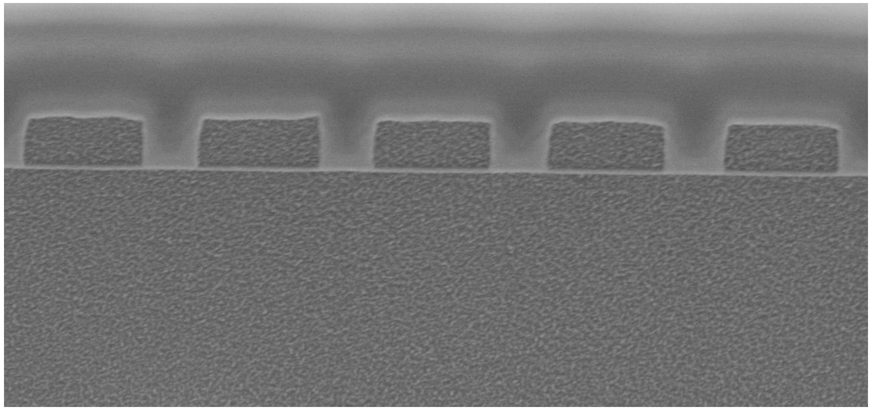




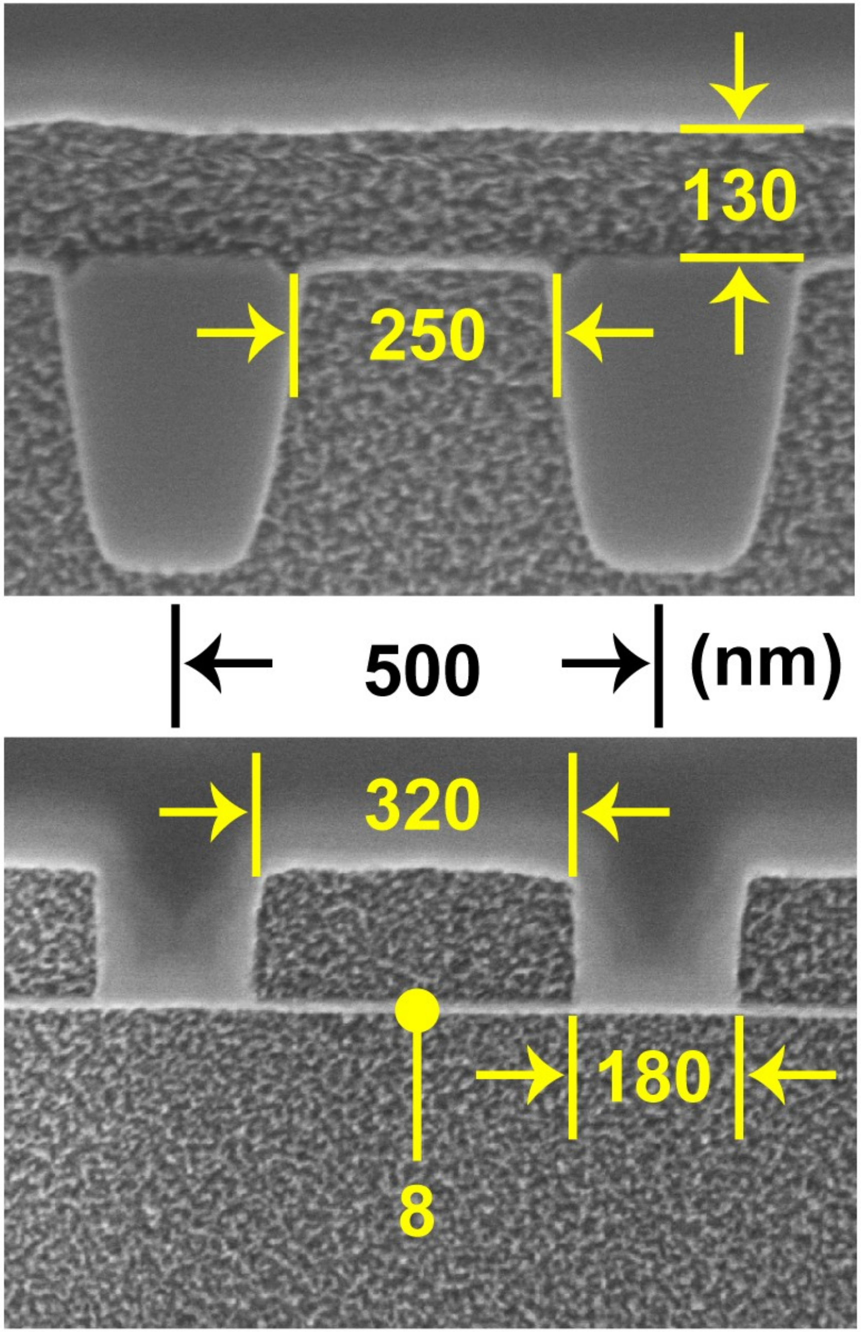
CCD Structure



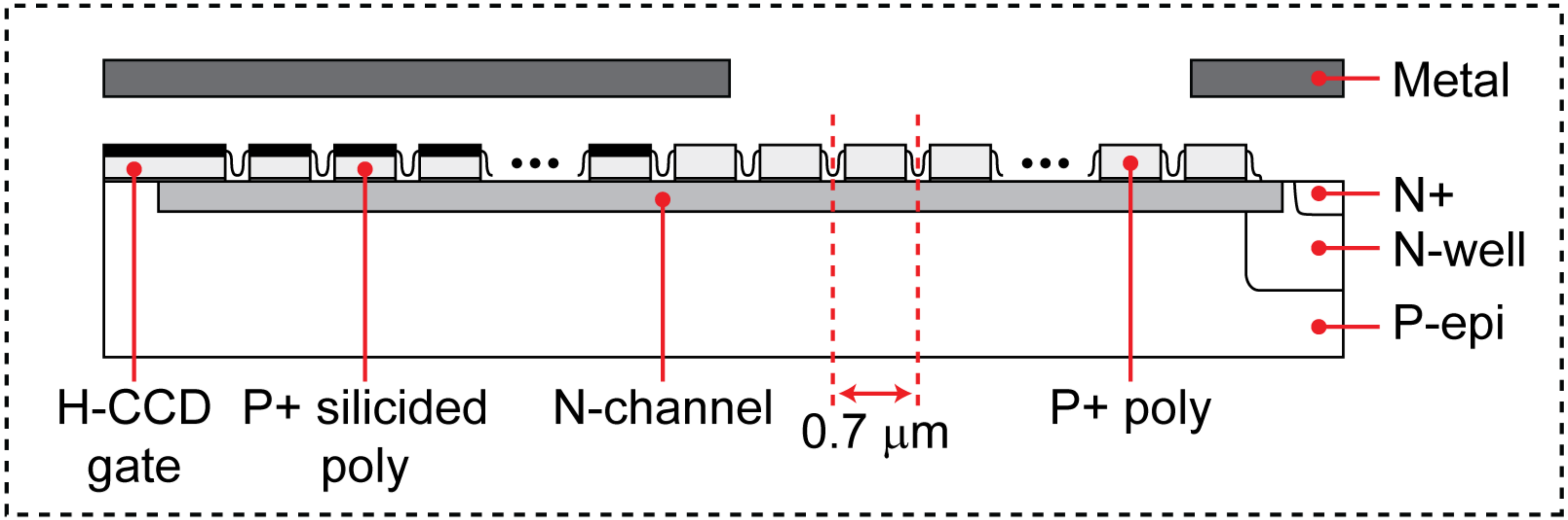
STI forms the channel stop



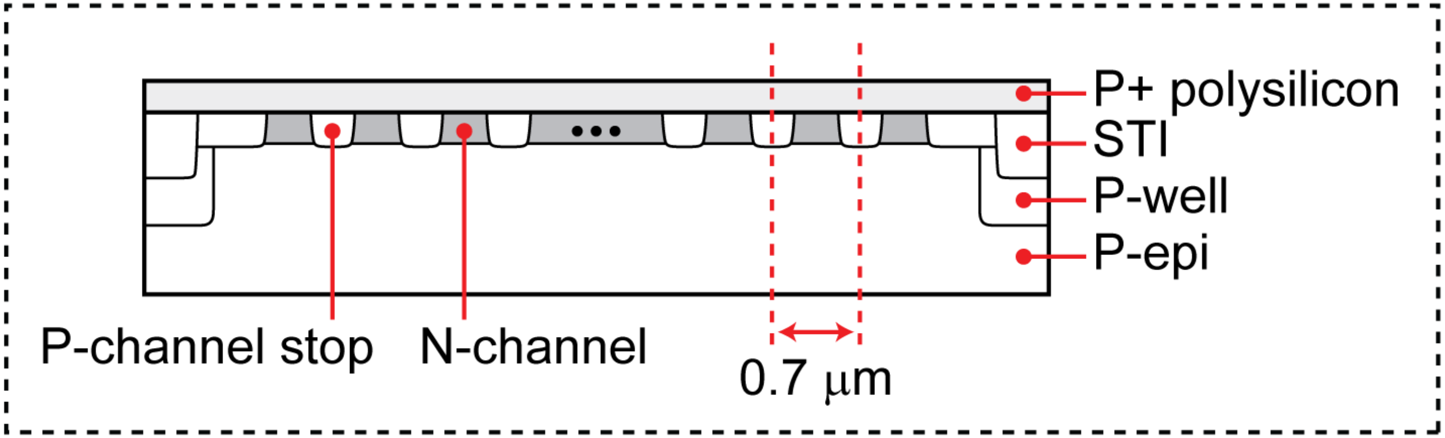
Single-level poly electrodes



The 0.7μm Buried Channel Pixel

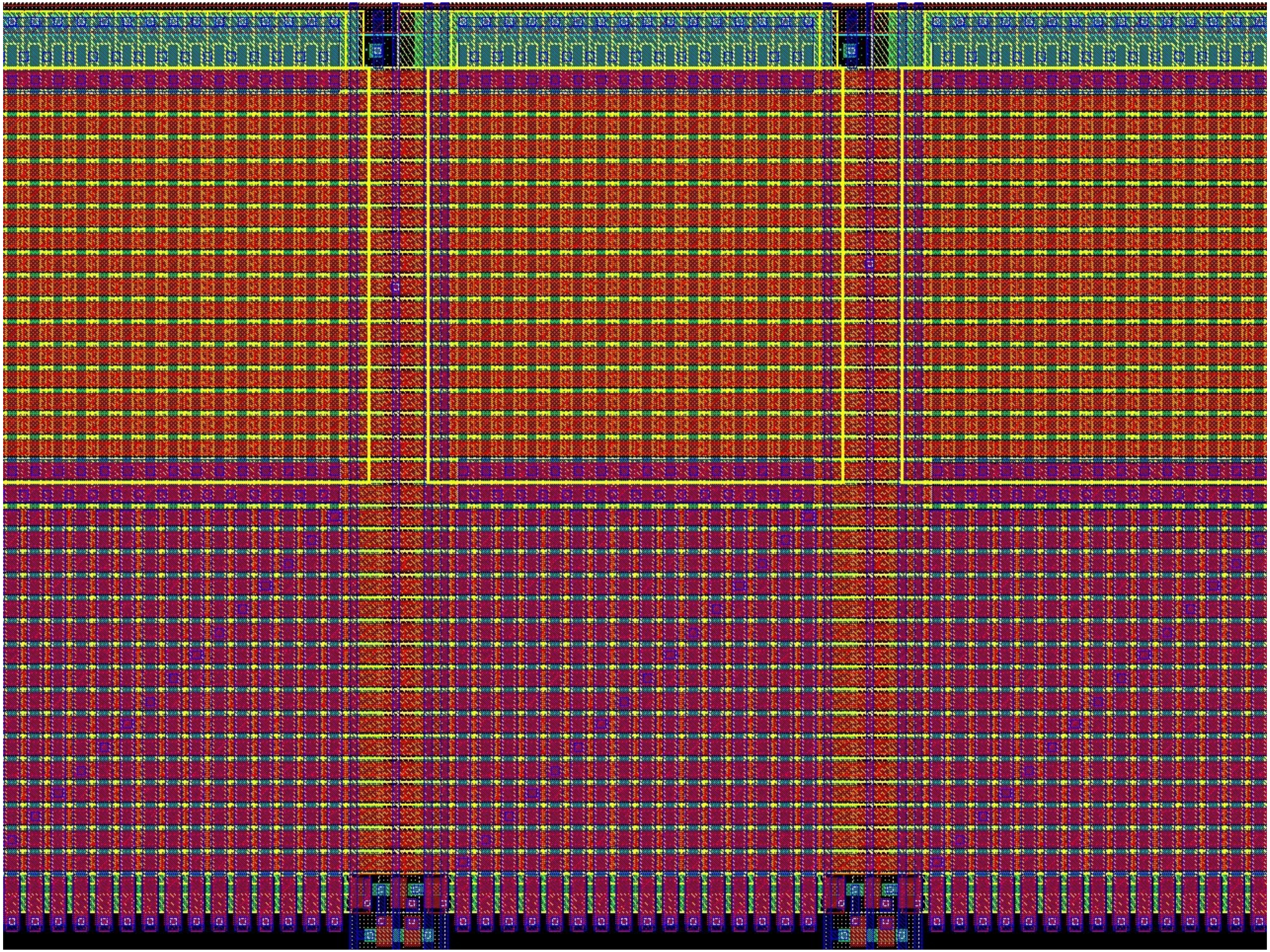


cross section along channel



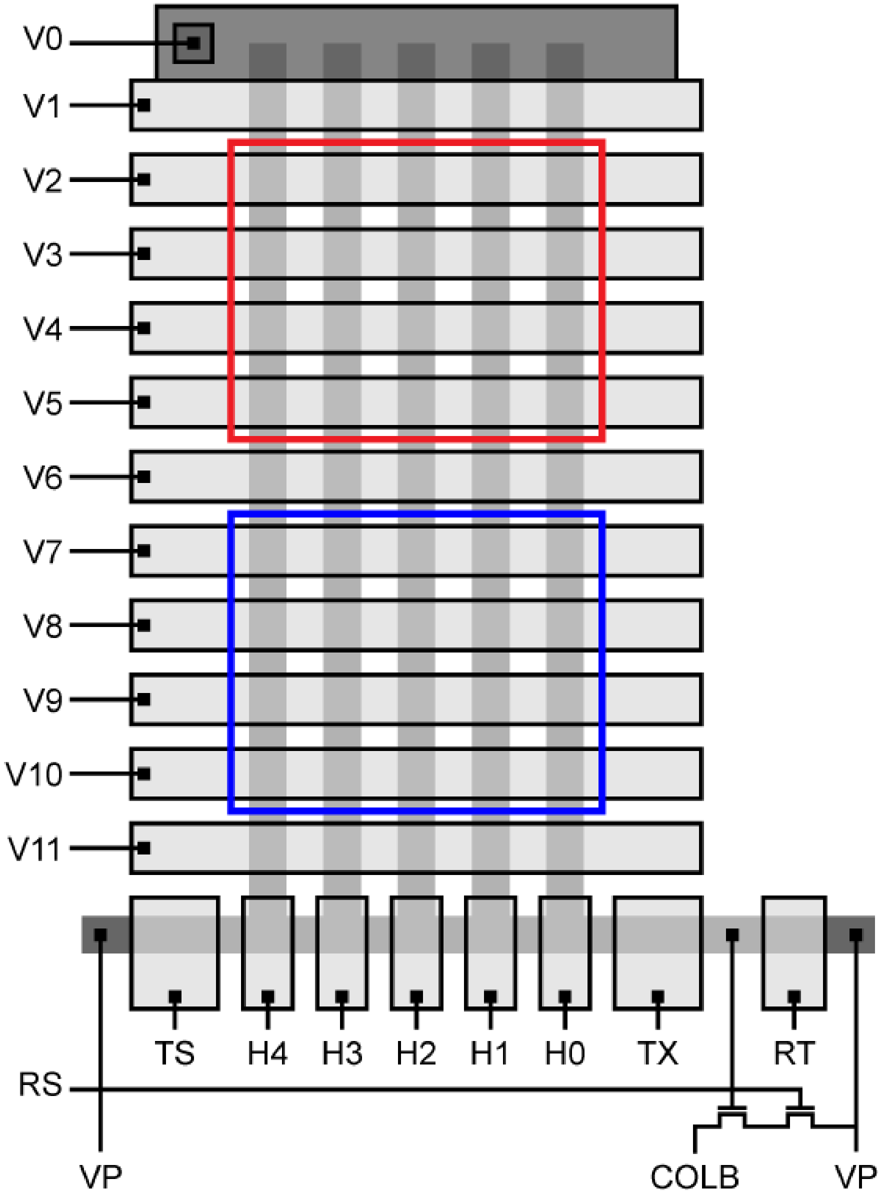
cross section against channel

Layout Masks for Buried Channel CCD

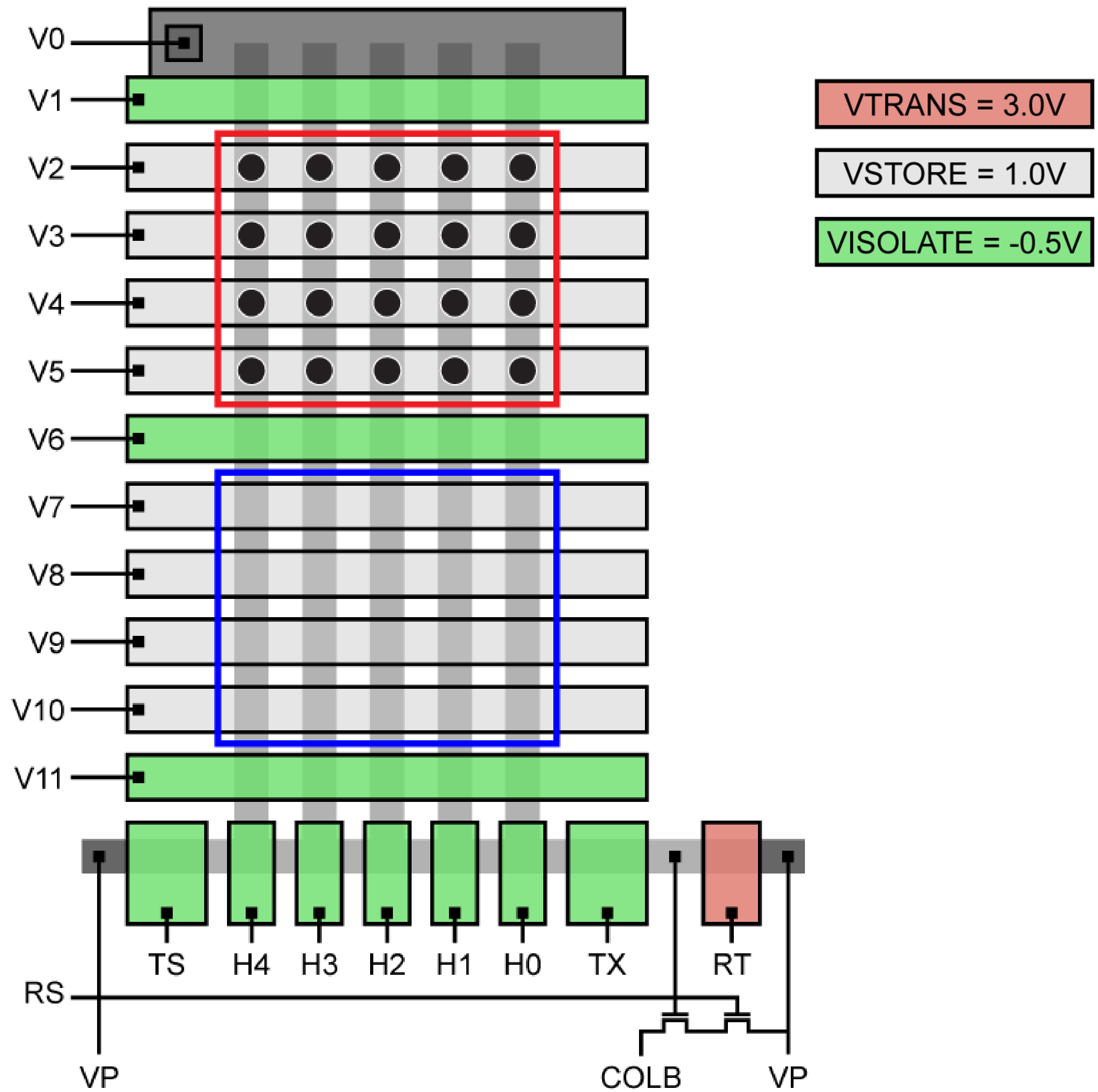


Operation

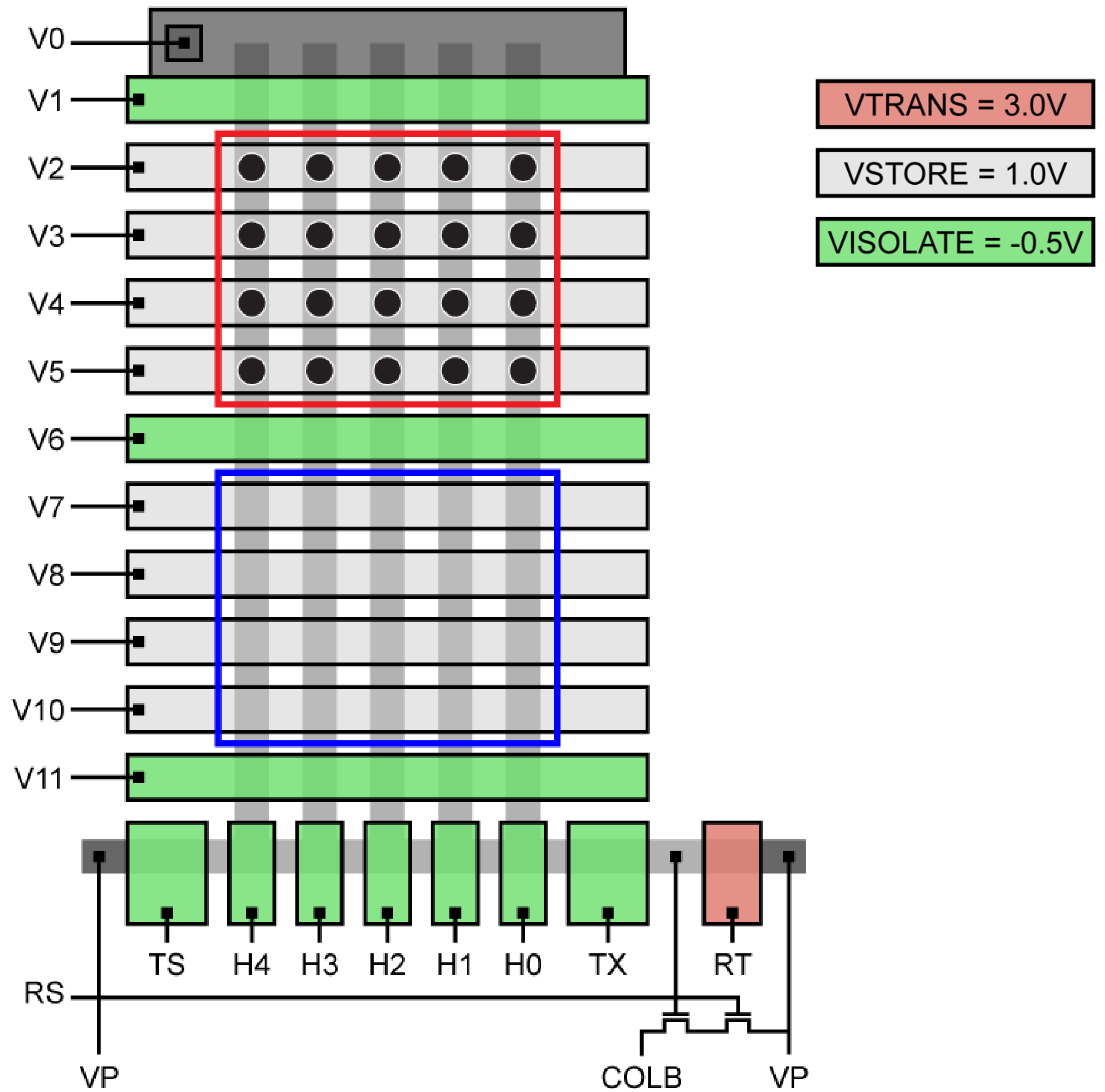
- Flush
- Integrate
- Frame Transfer
- Horizontal Readout



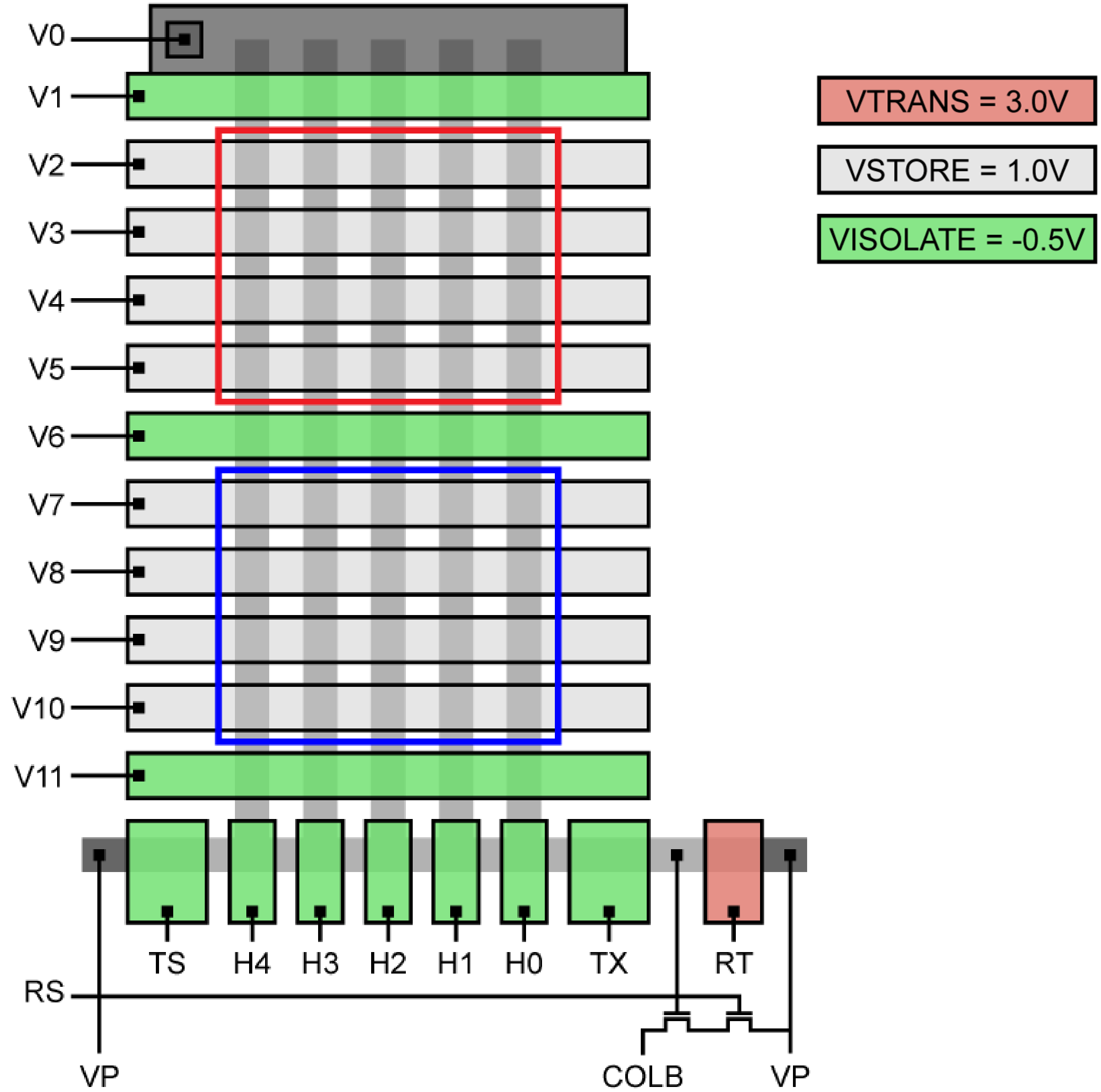
Operation (Flush)



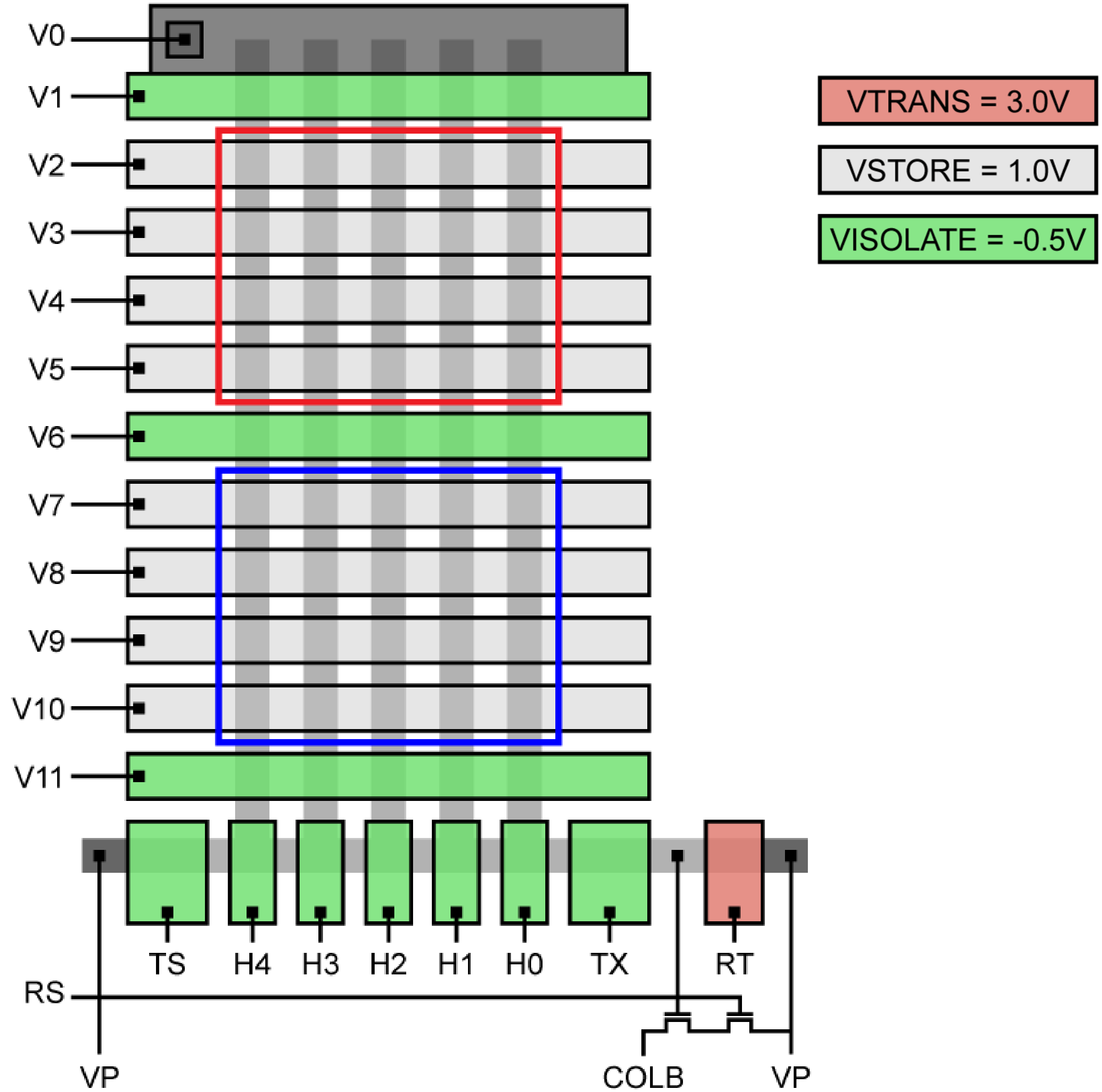
Operation (Flush)



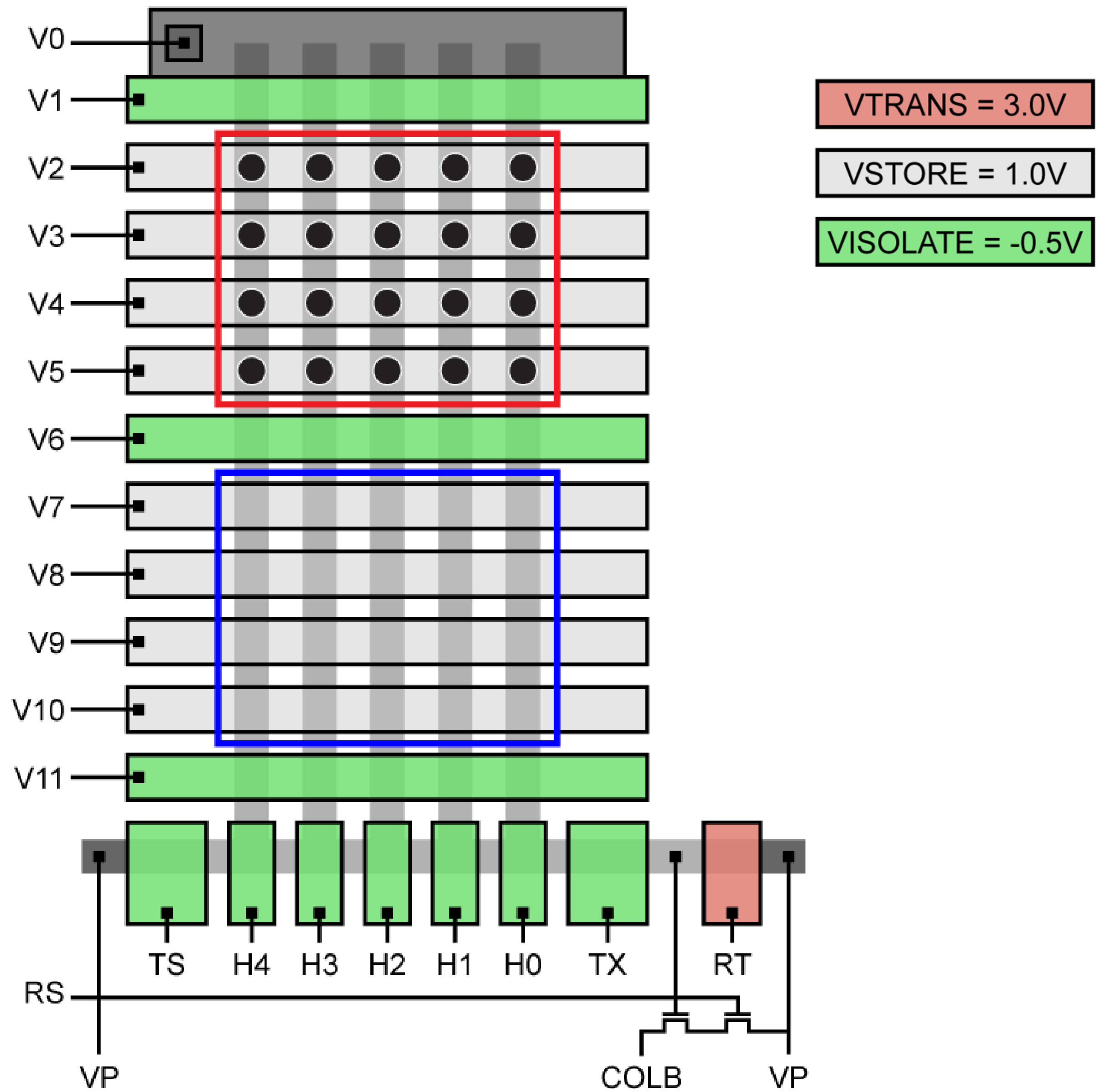
Operation (Integrate)



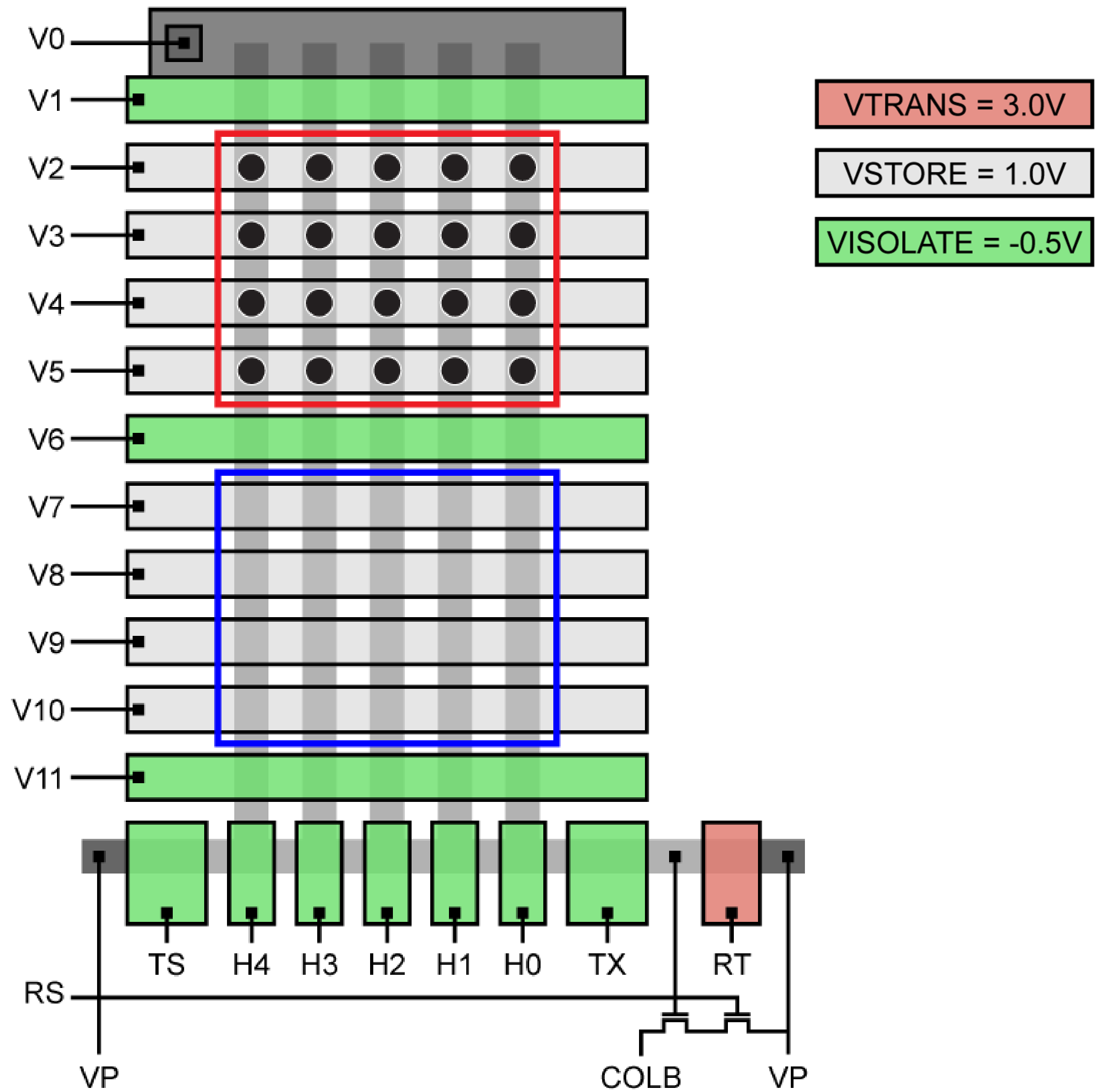
Operation (Integrate)



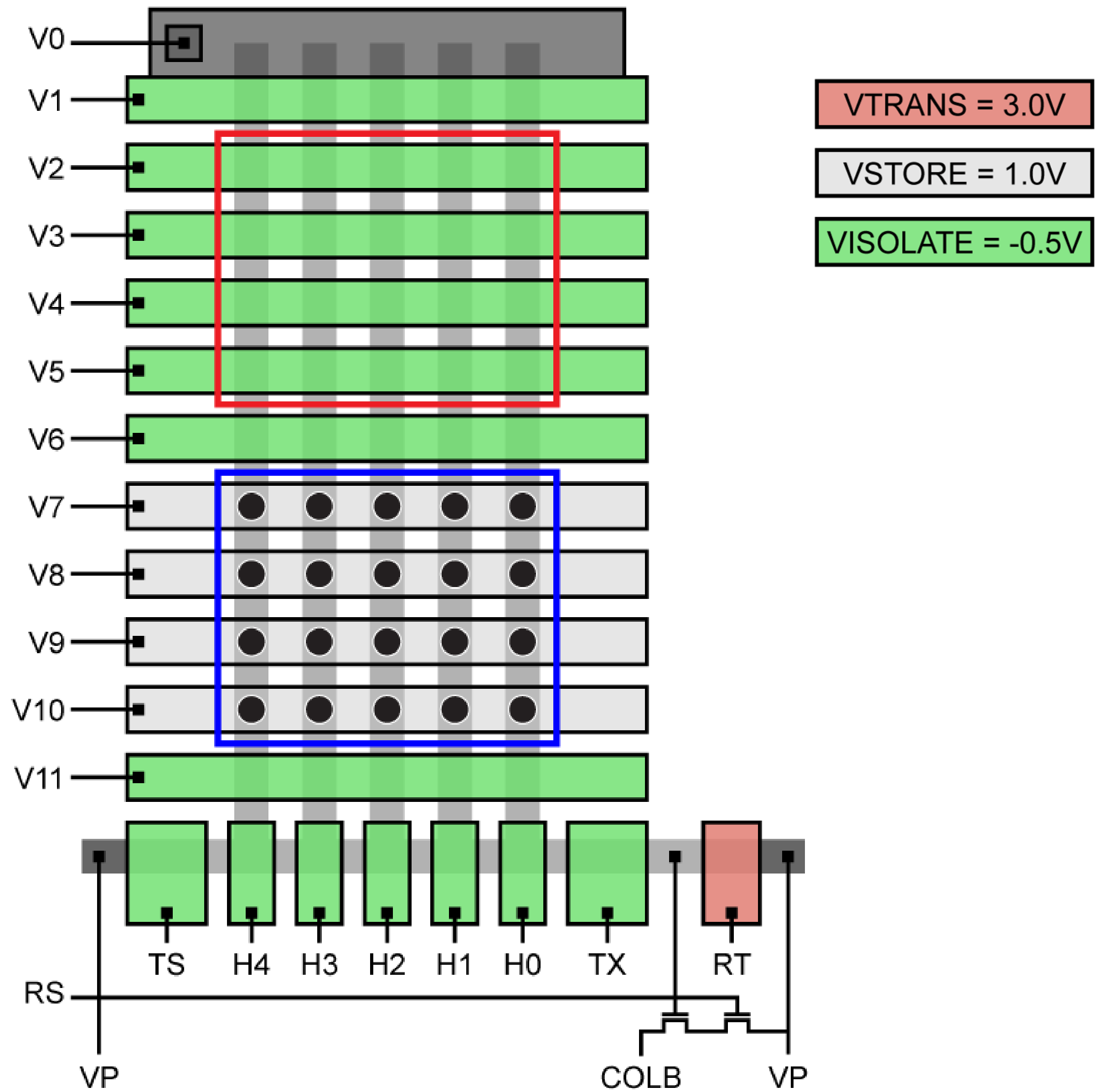
Operation (Frame Transfer)



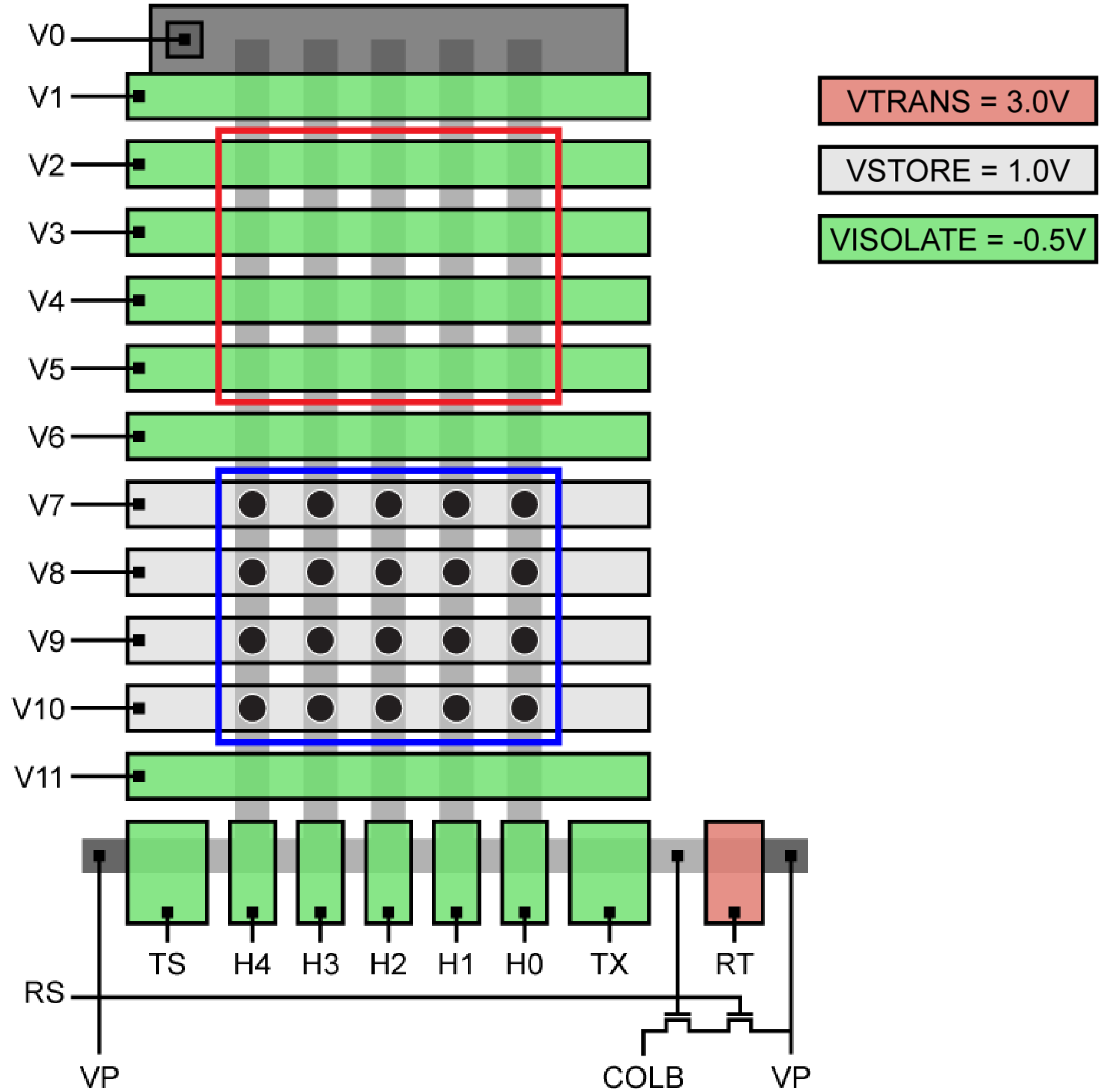
Operation (Frame Transfer)



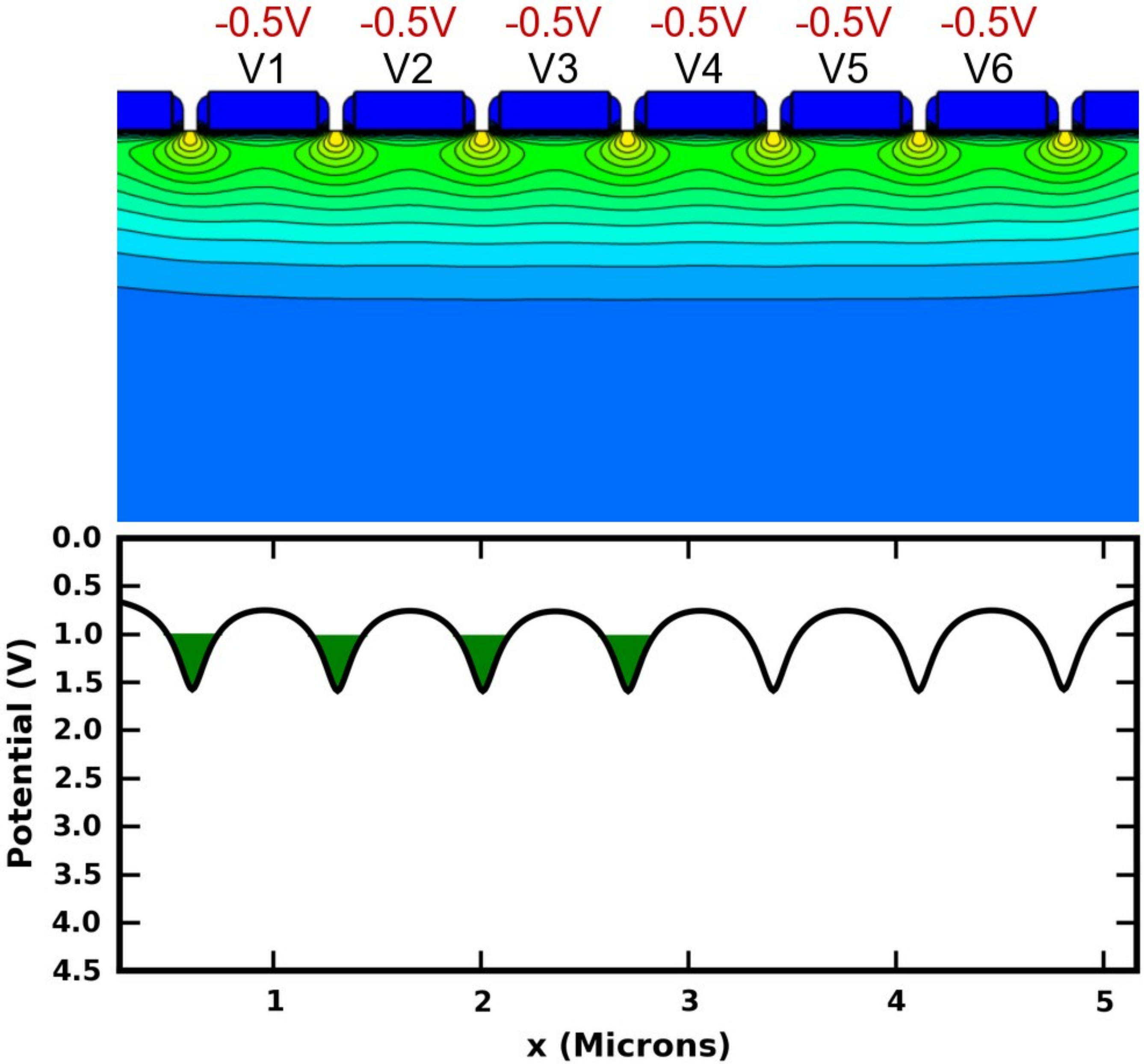
Operation (Horizontal Transfer)



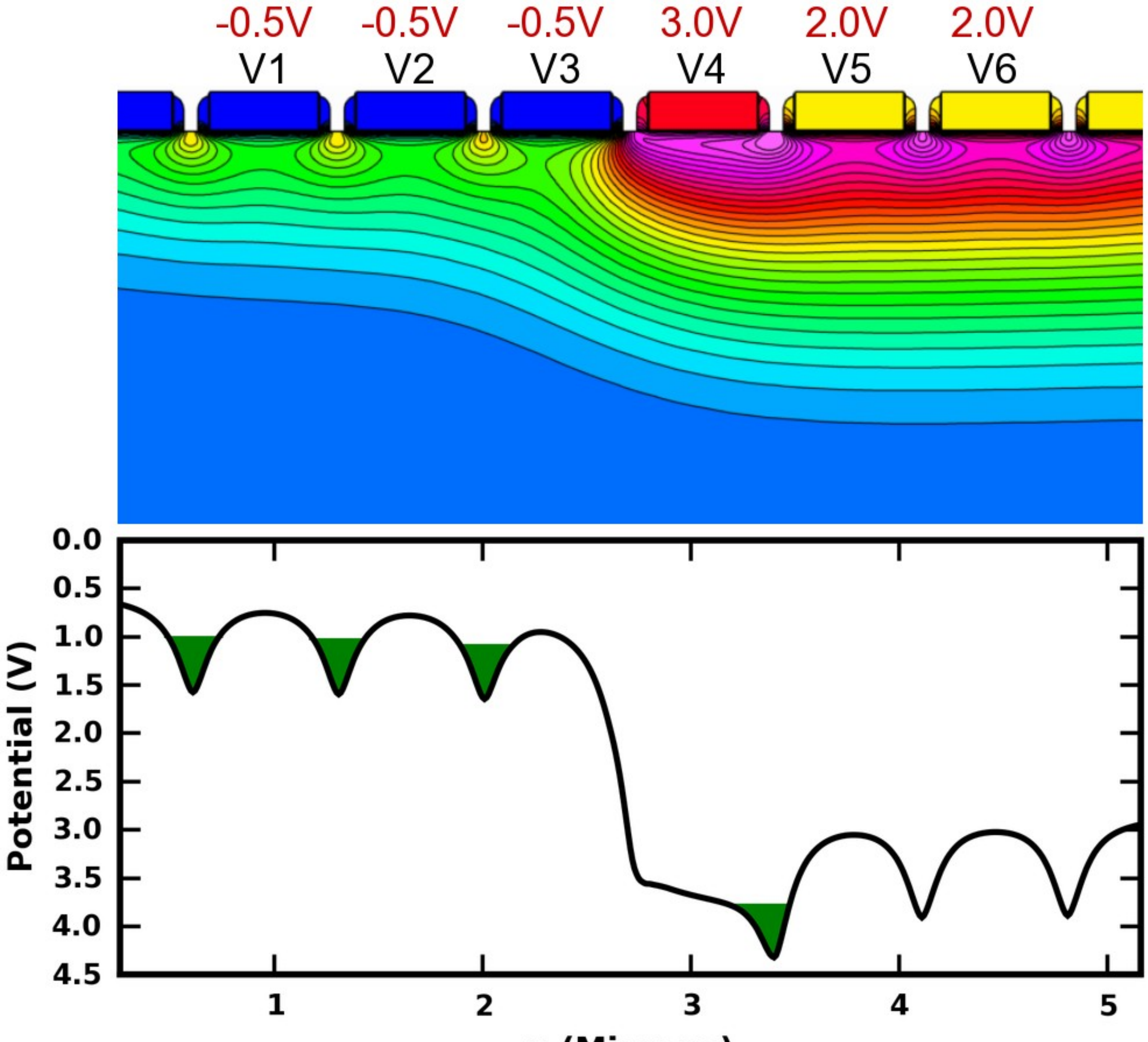
Operation (Horizontal Transfer)



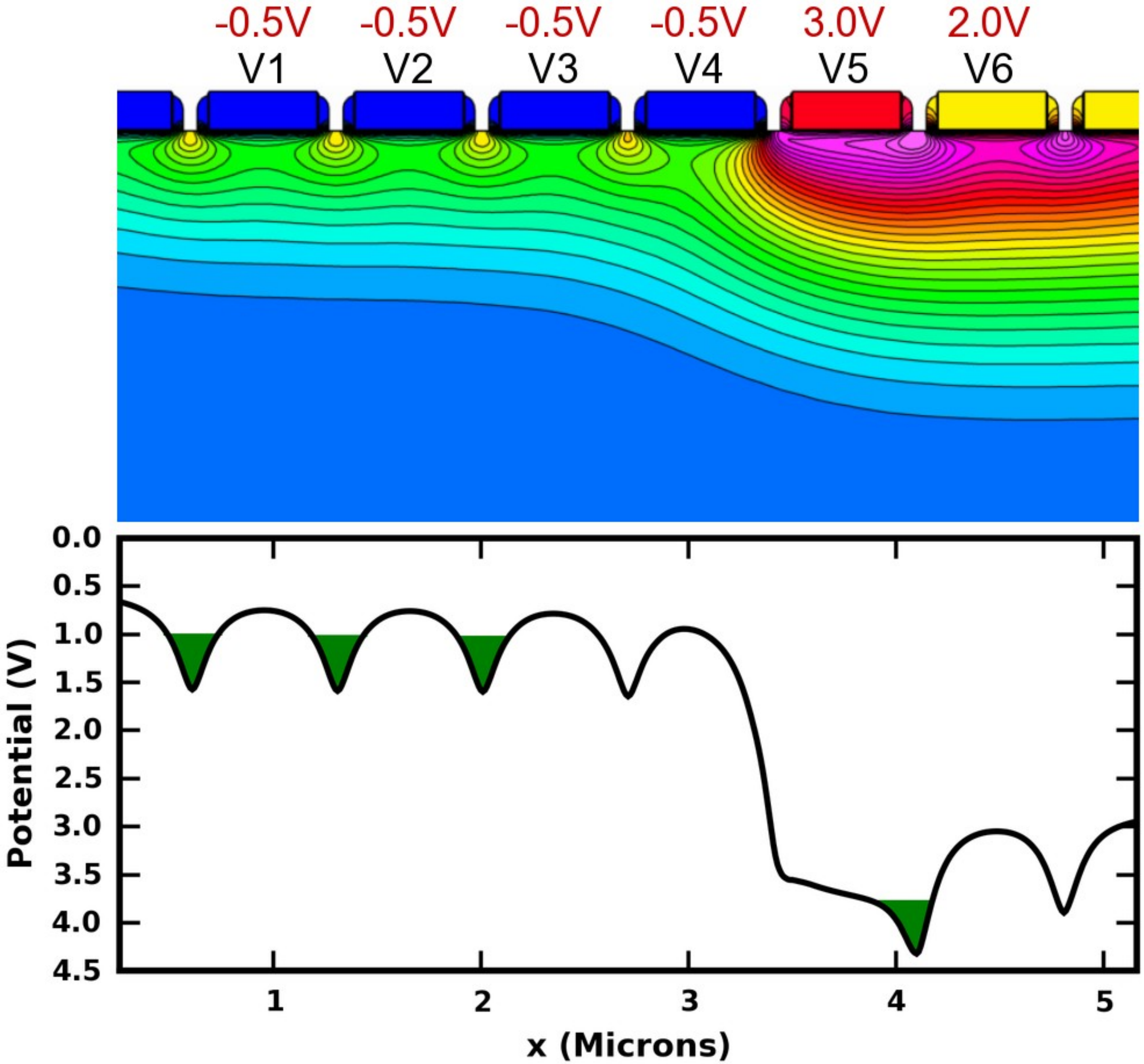
Potential Profile Along Channel



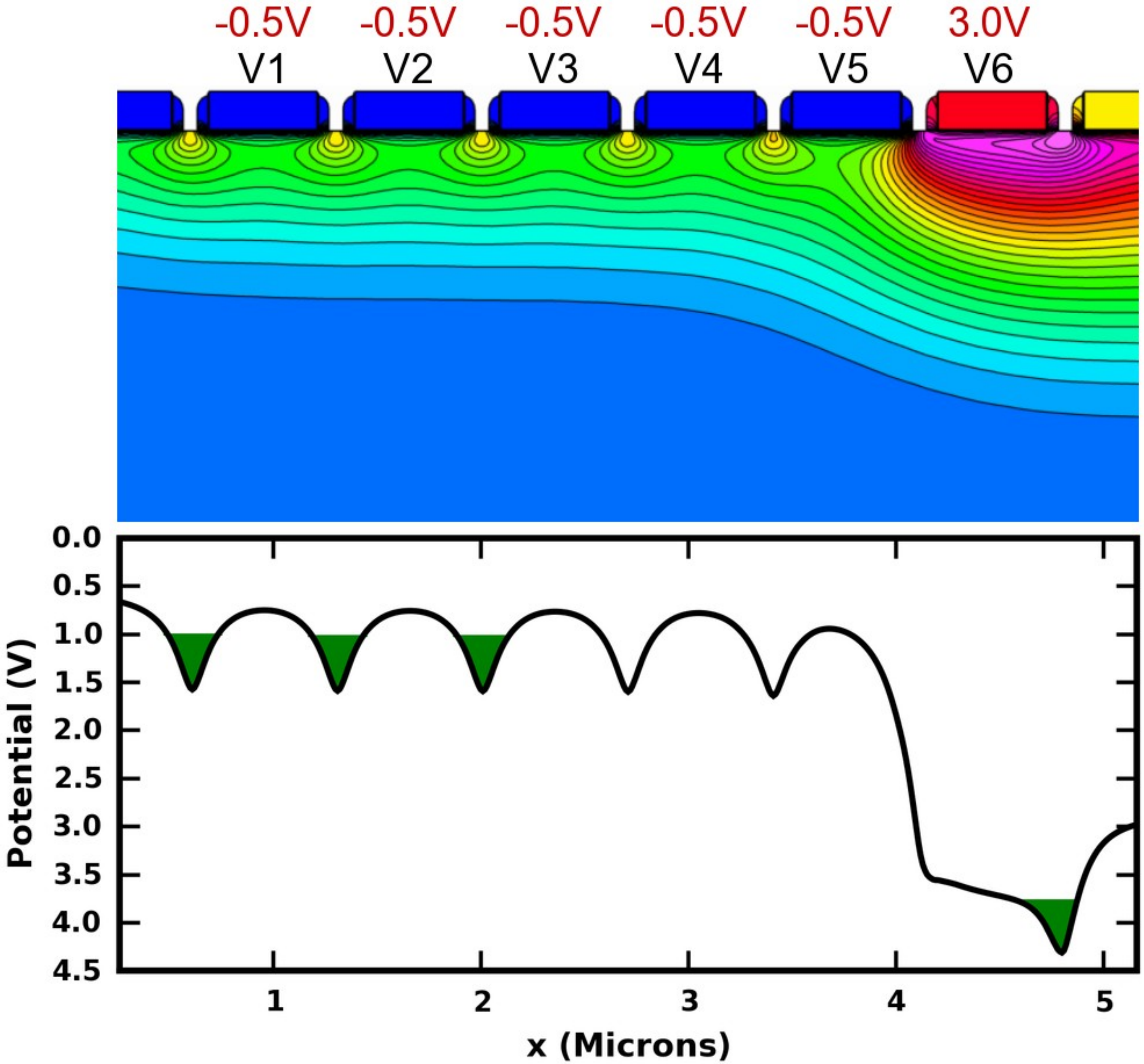
Potential Profile Along Channel



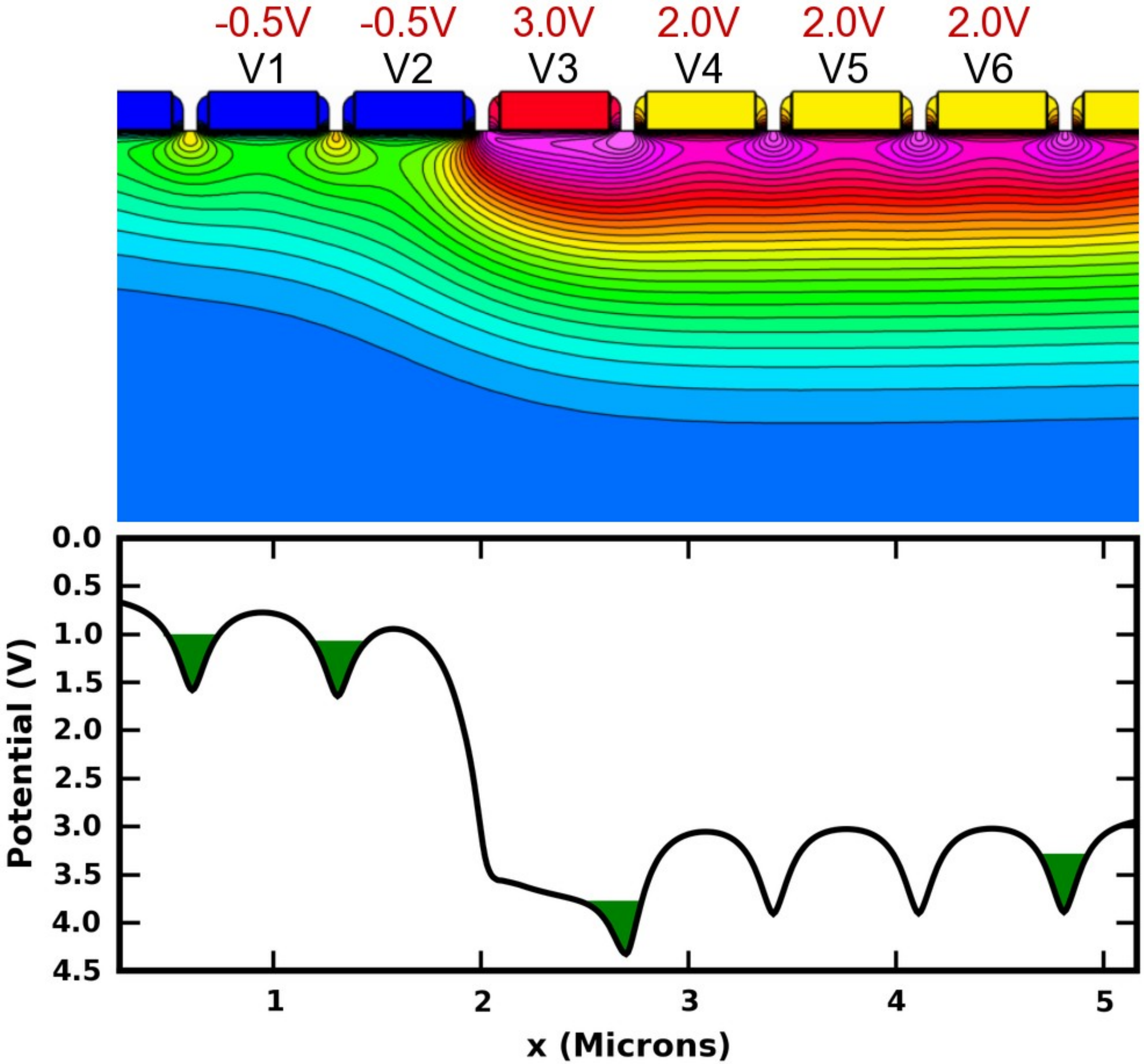
Potential Profile Along Channel



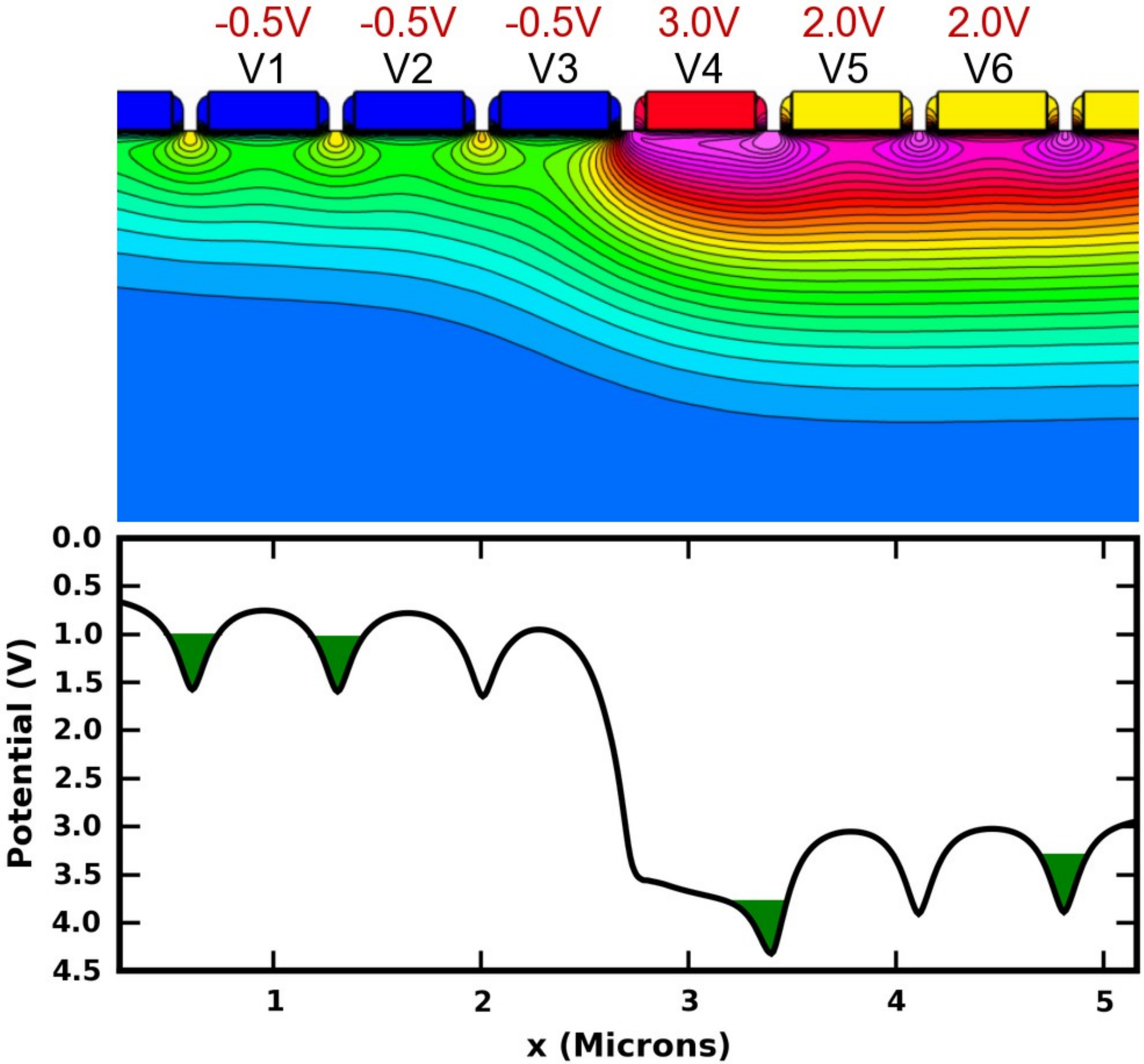
Potential Profile Along Channel



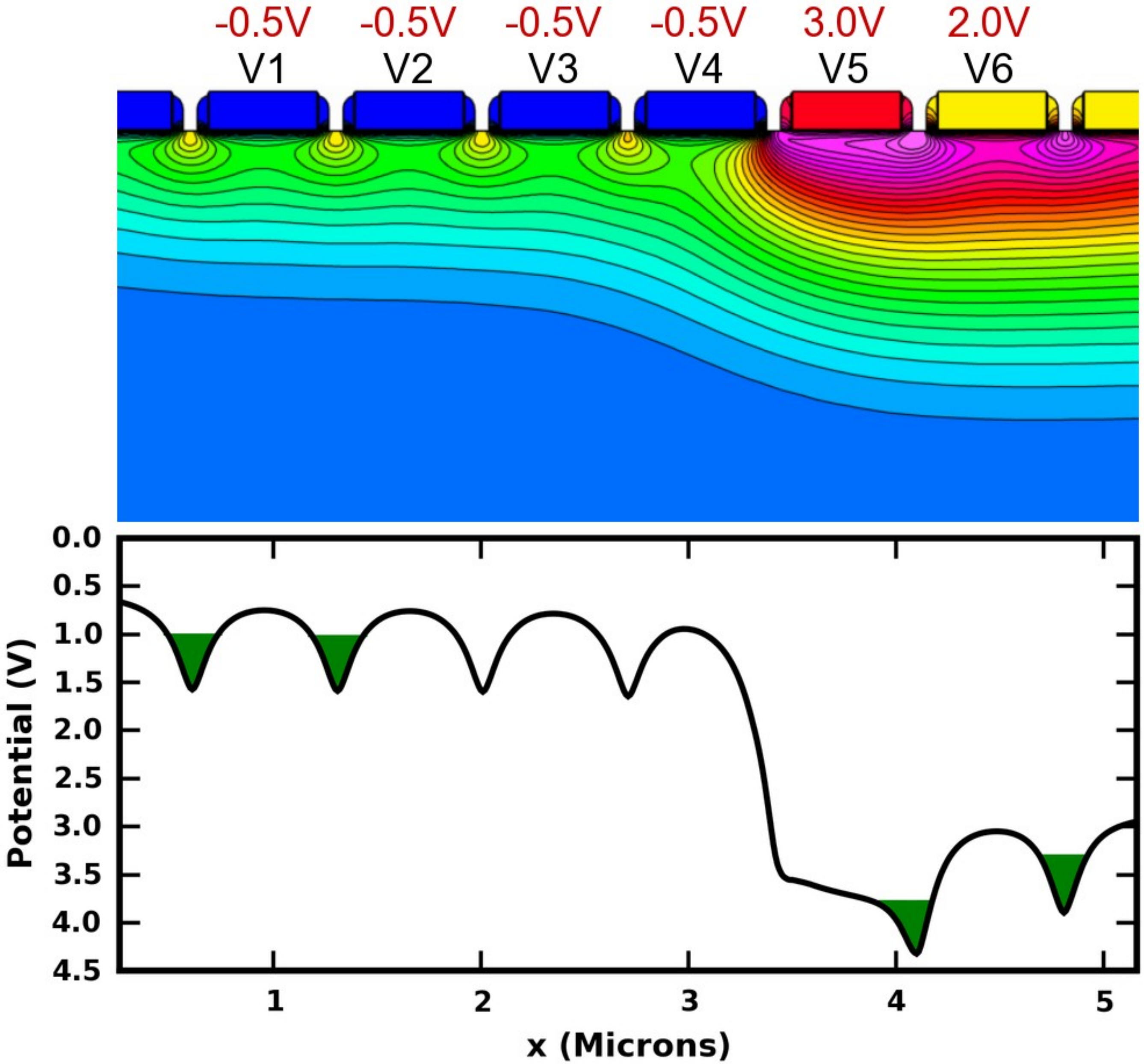
Potential Profile Along Channel



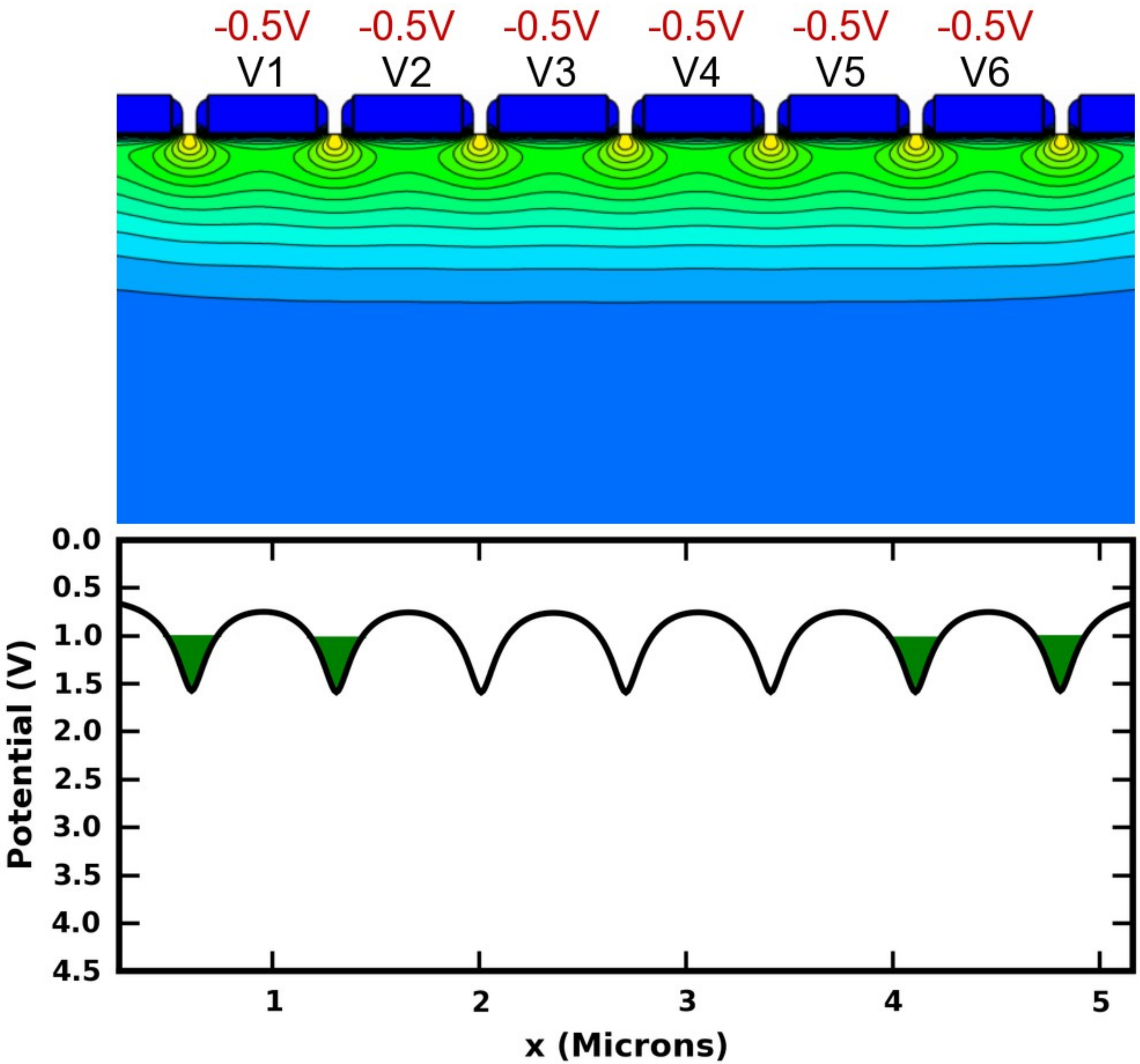
Potential Profile Along Channel



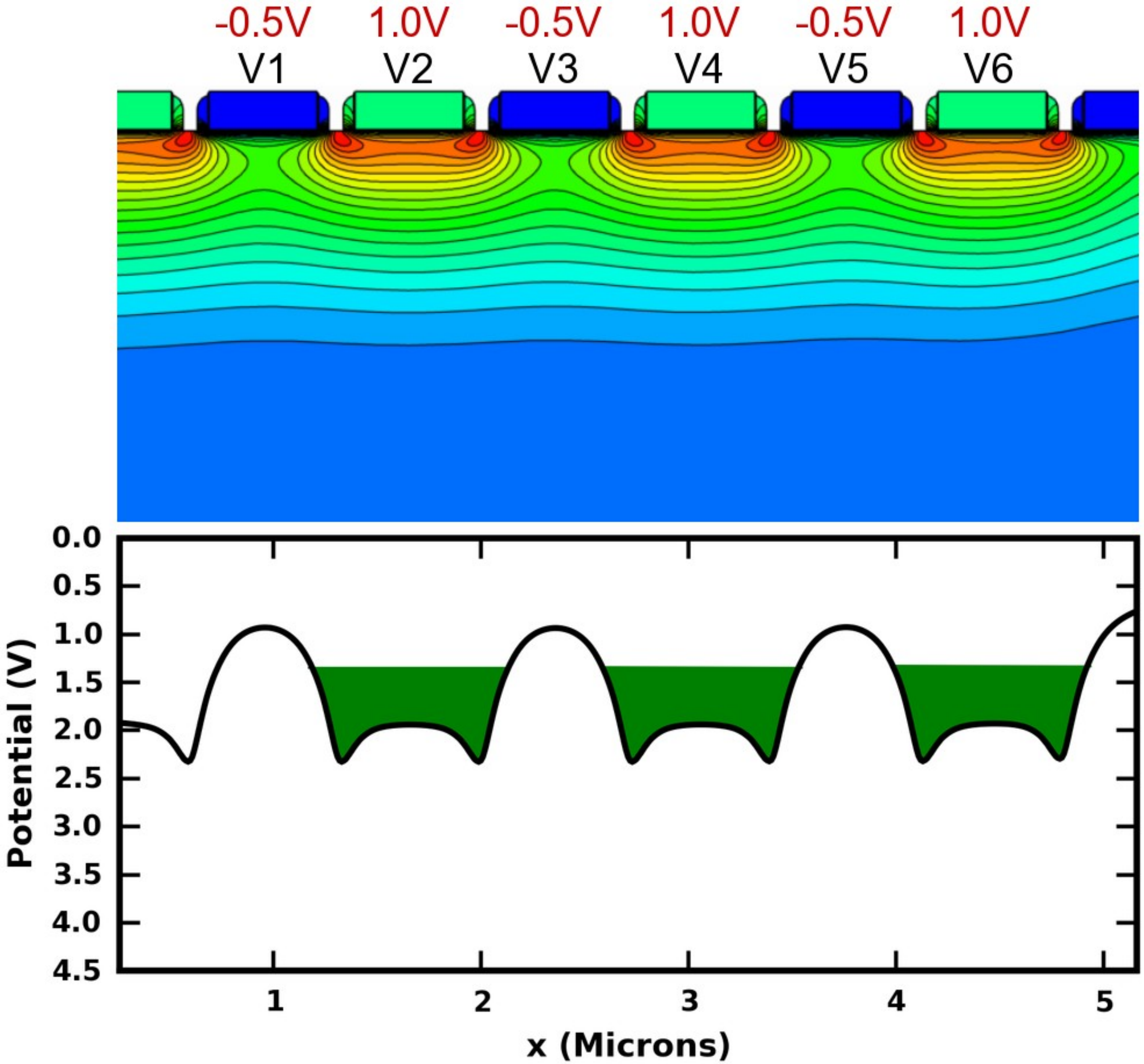
Potential Profile Along Channel



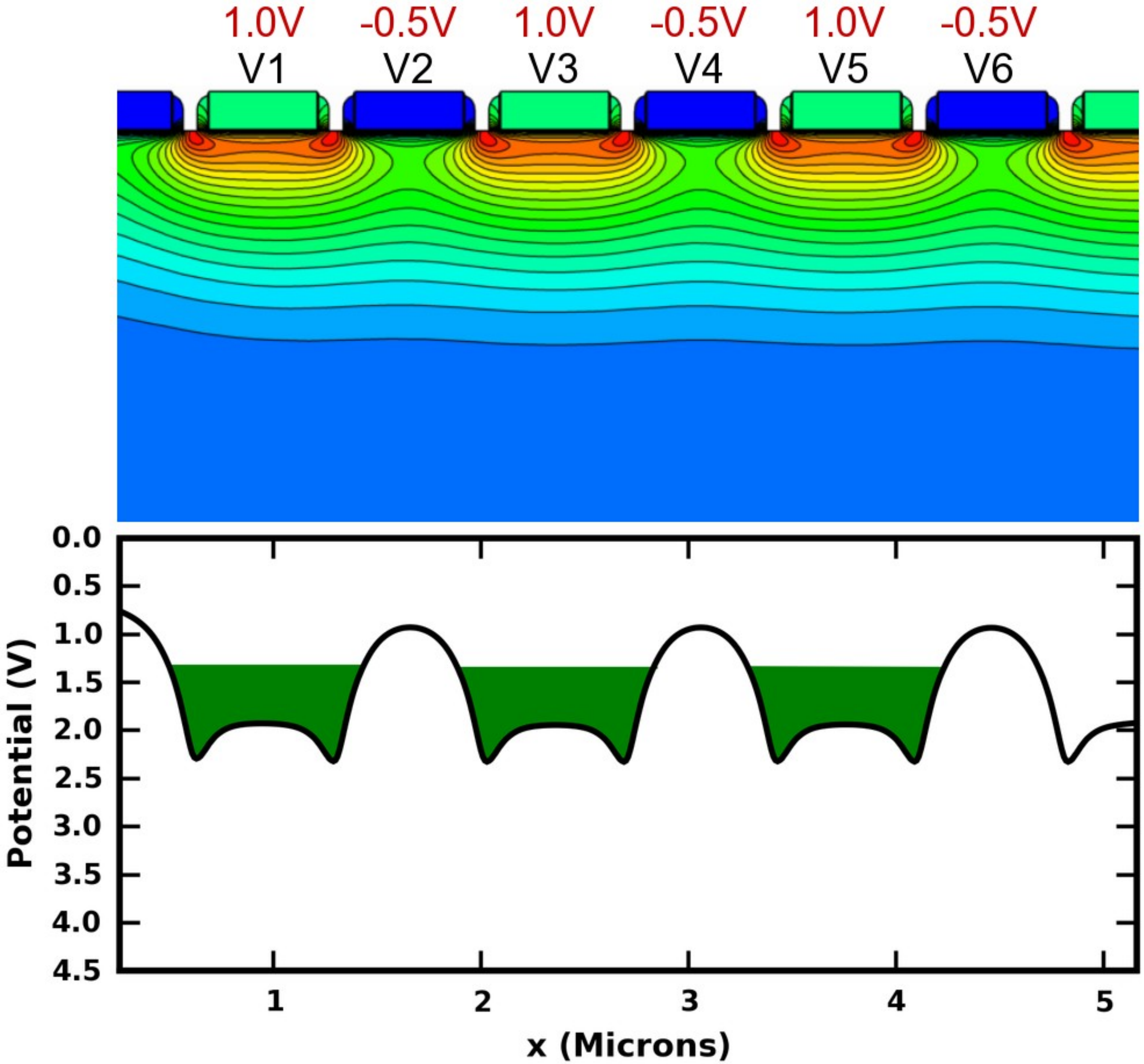
Potential Profile Along Channel



Interlaced Mode (Even Field)

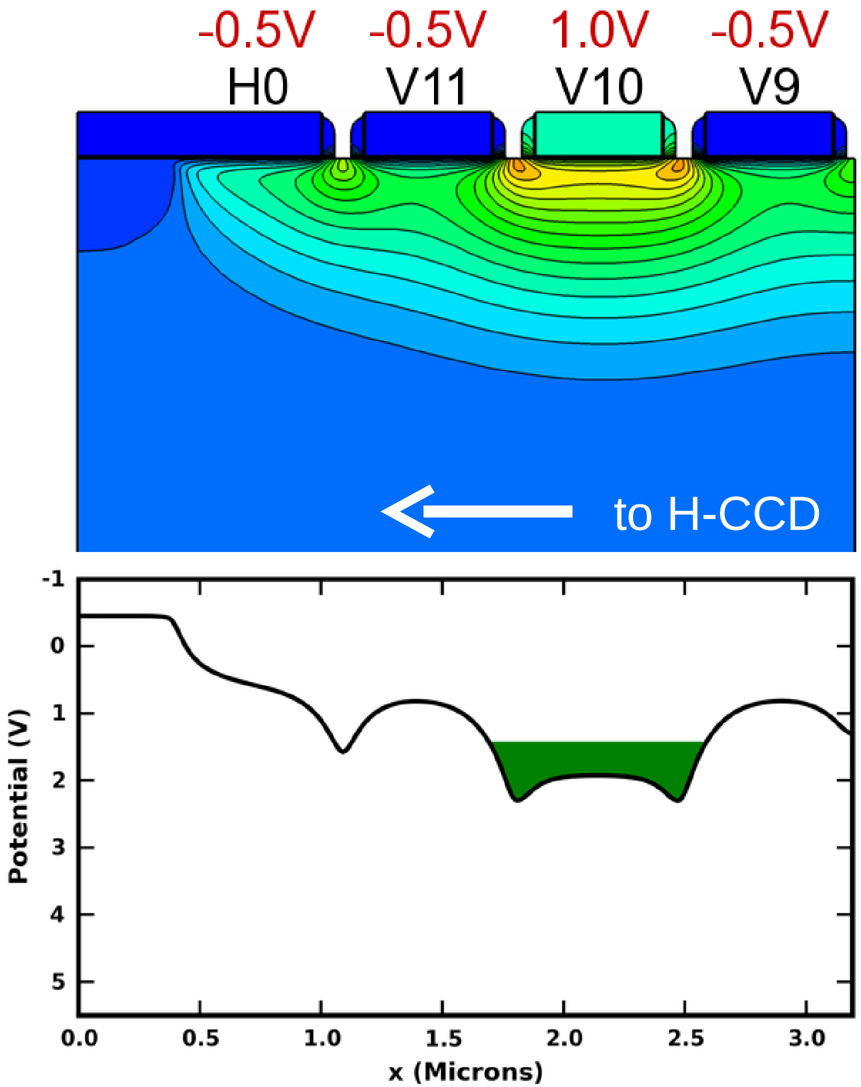


Interlaced Mode (Odd Field)

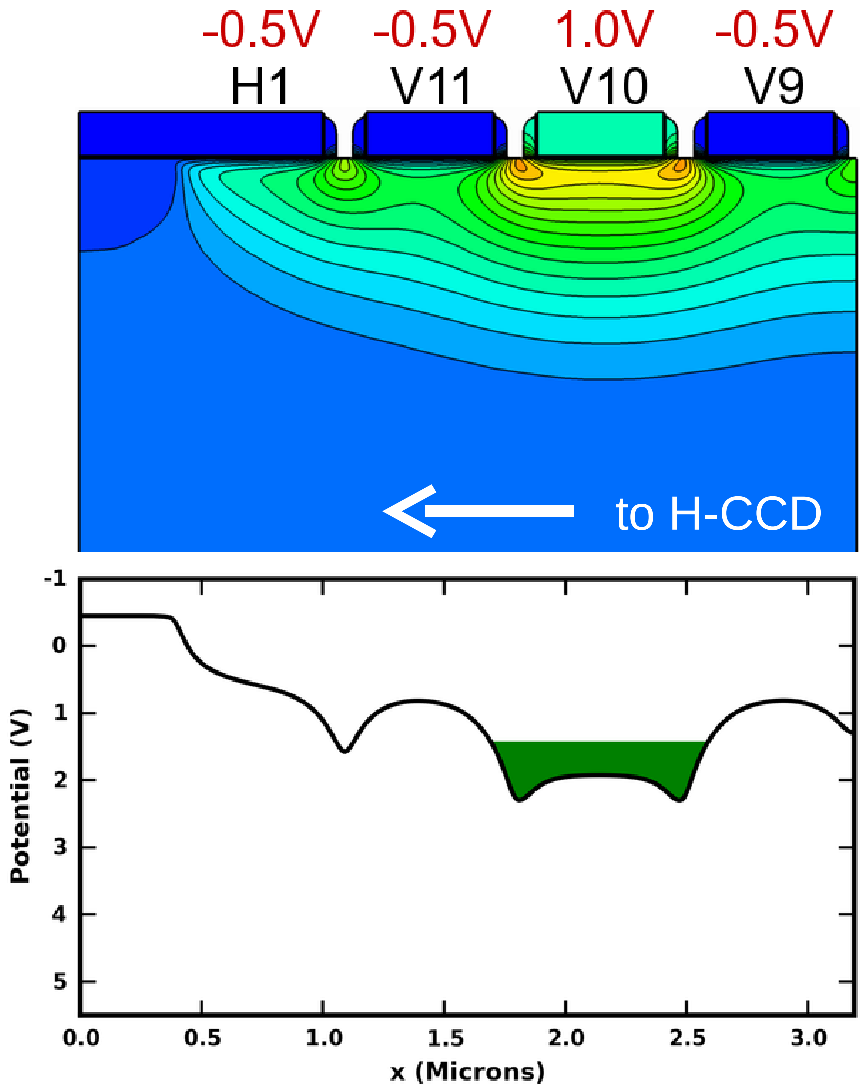


Vertical to Horizontal Transfer

Even column

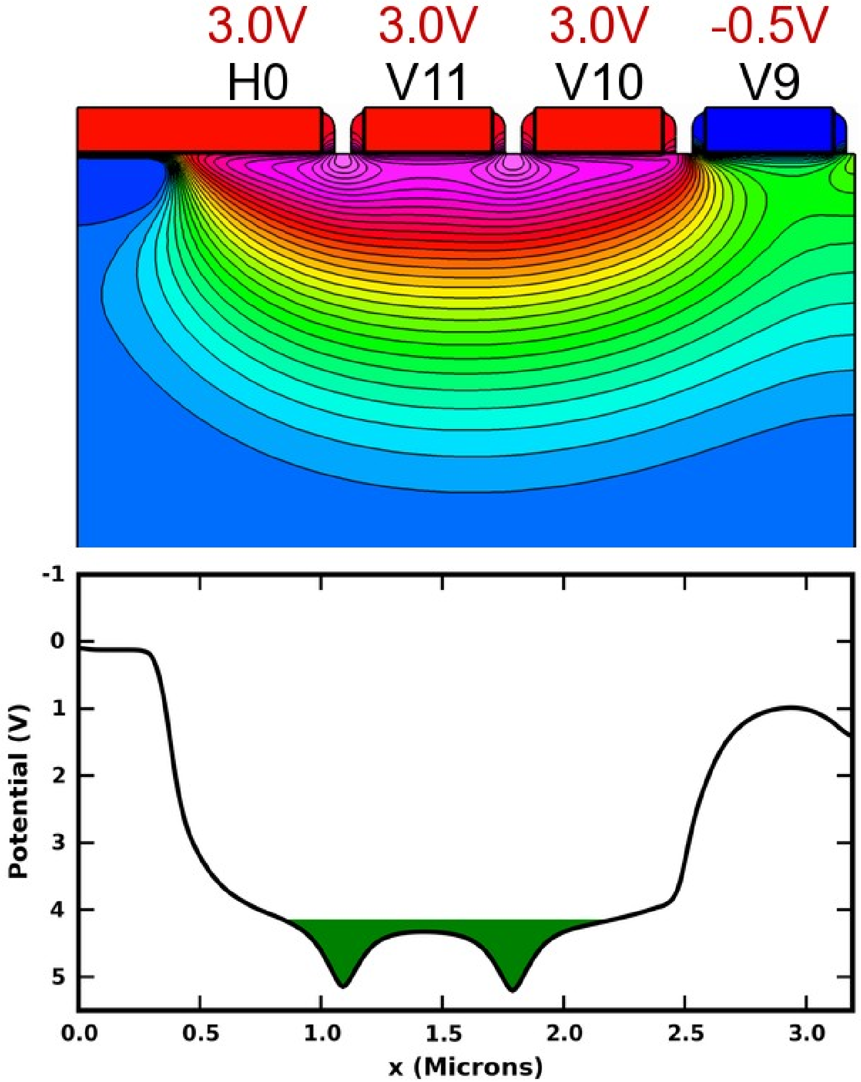


Odd column

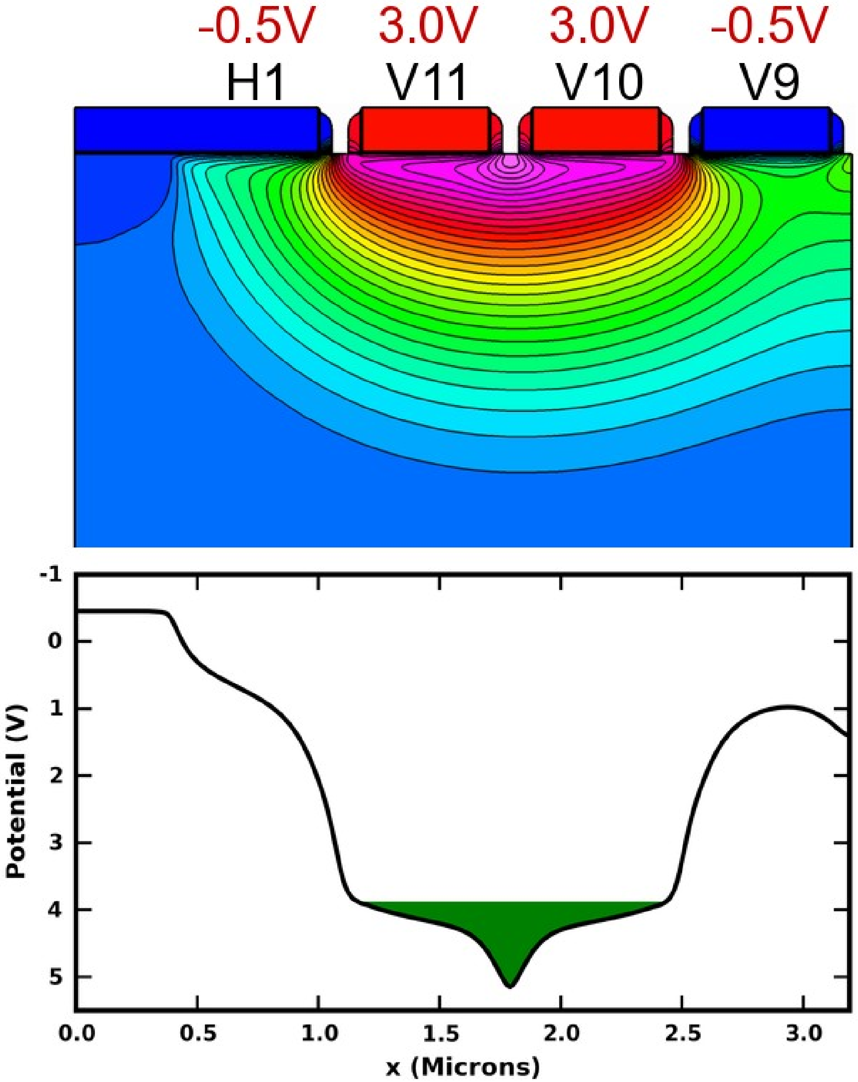


Vertical to Horizontal Transfer

Even column

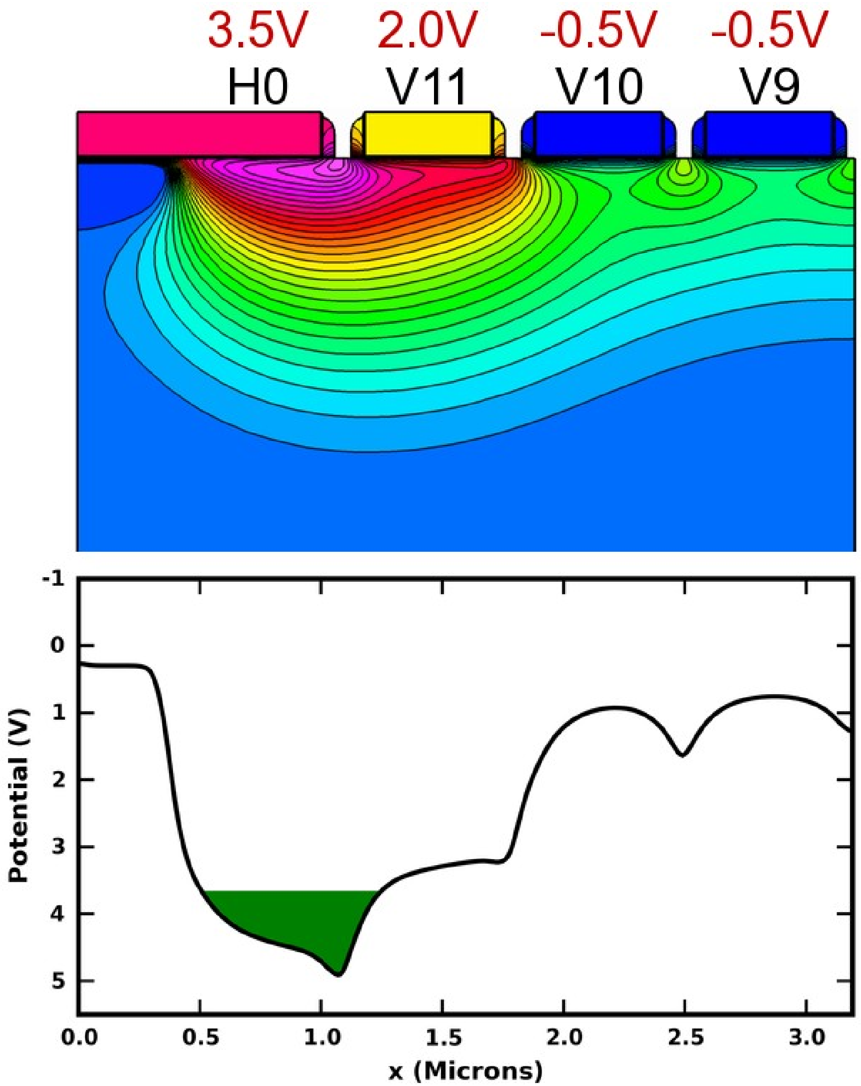


Odd column

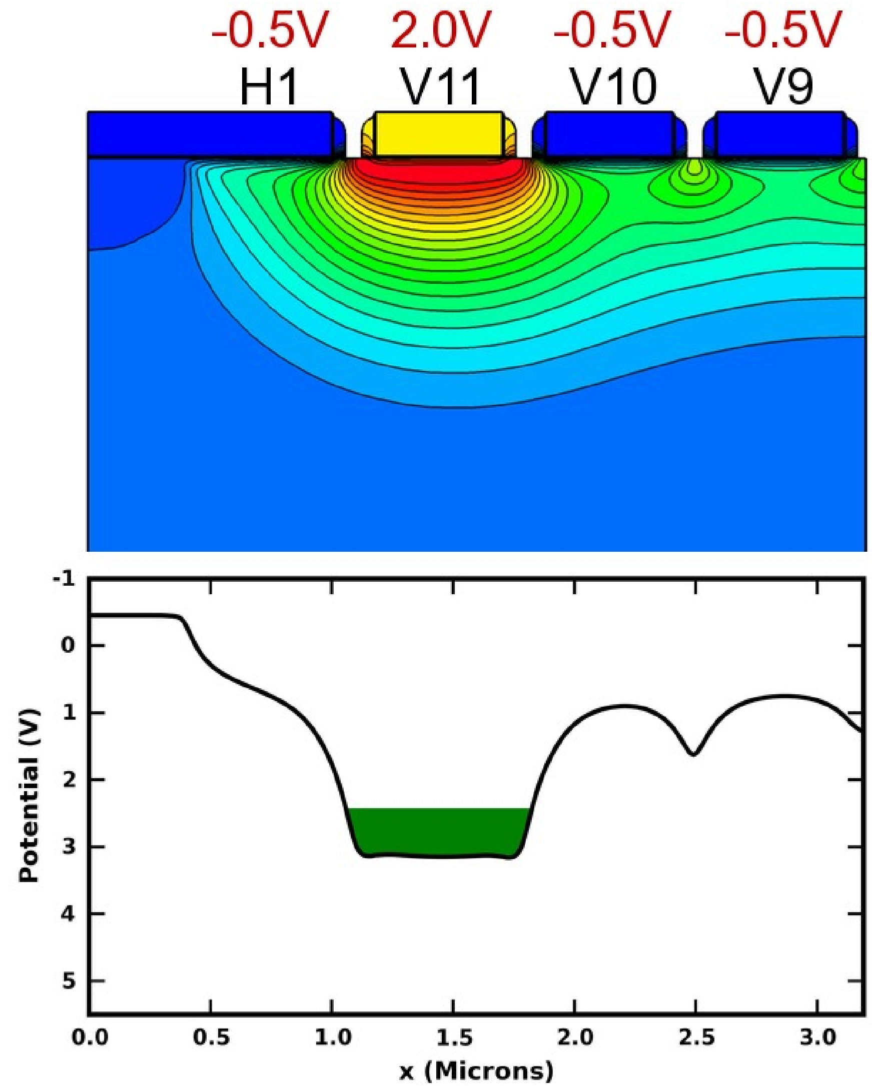


Vertical to Horizontal Transfer

Even column

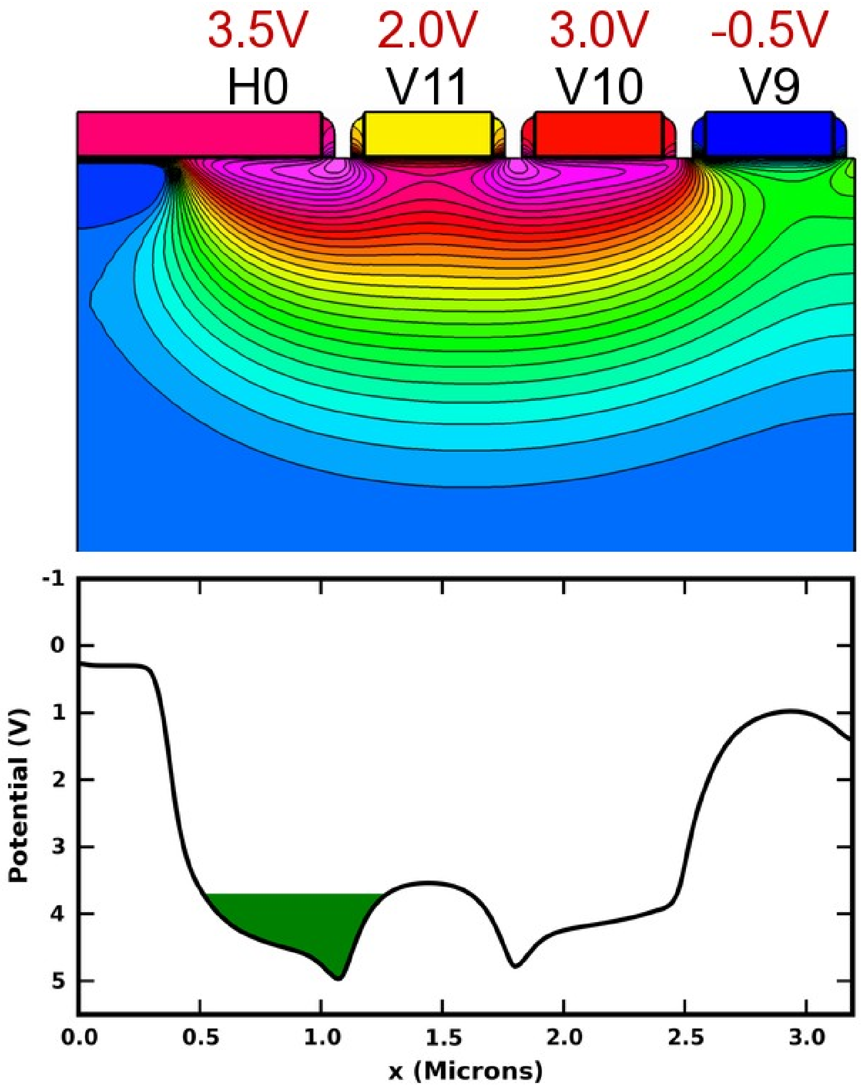


Odd column

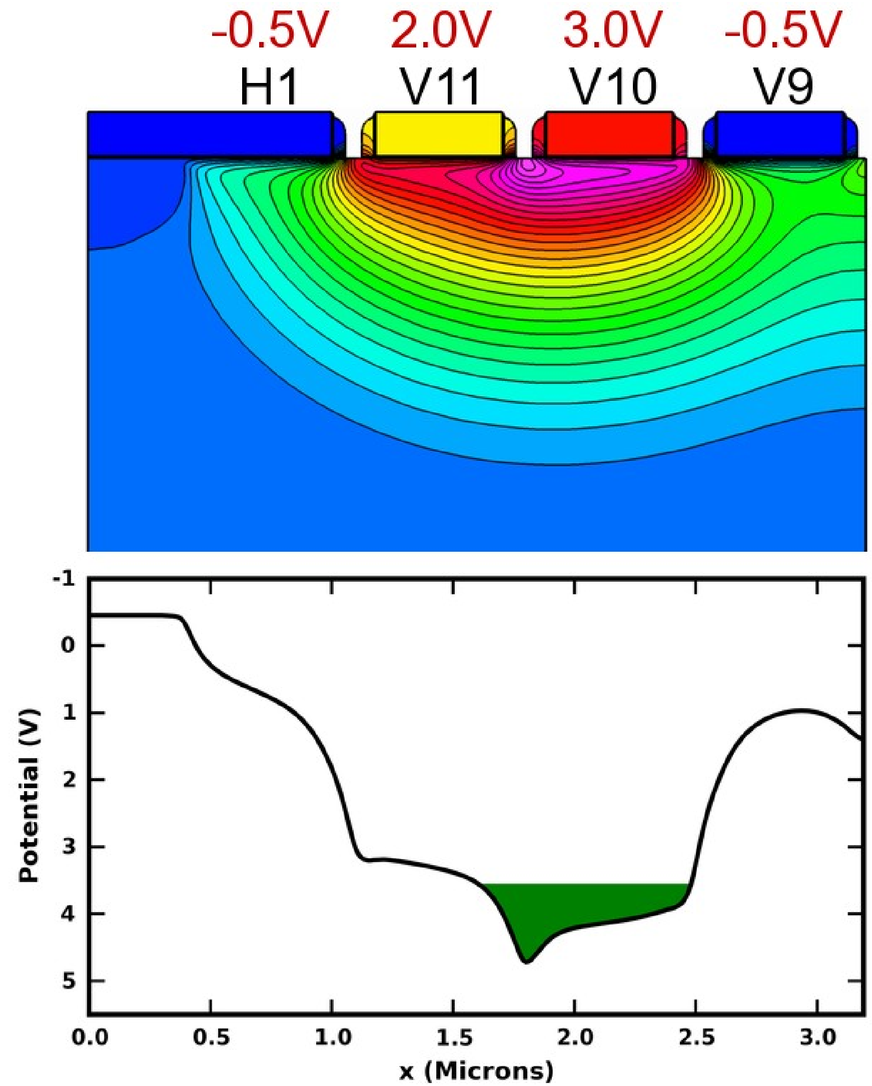


Vertical to Horizontal Transfer

Even column

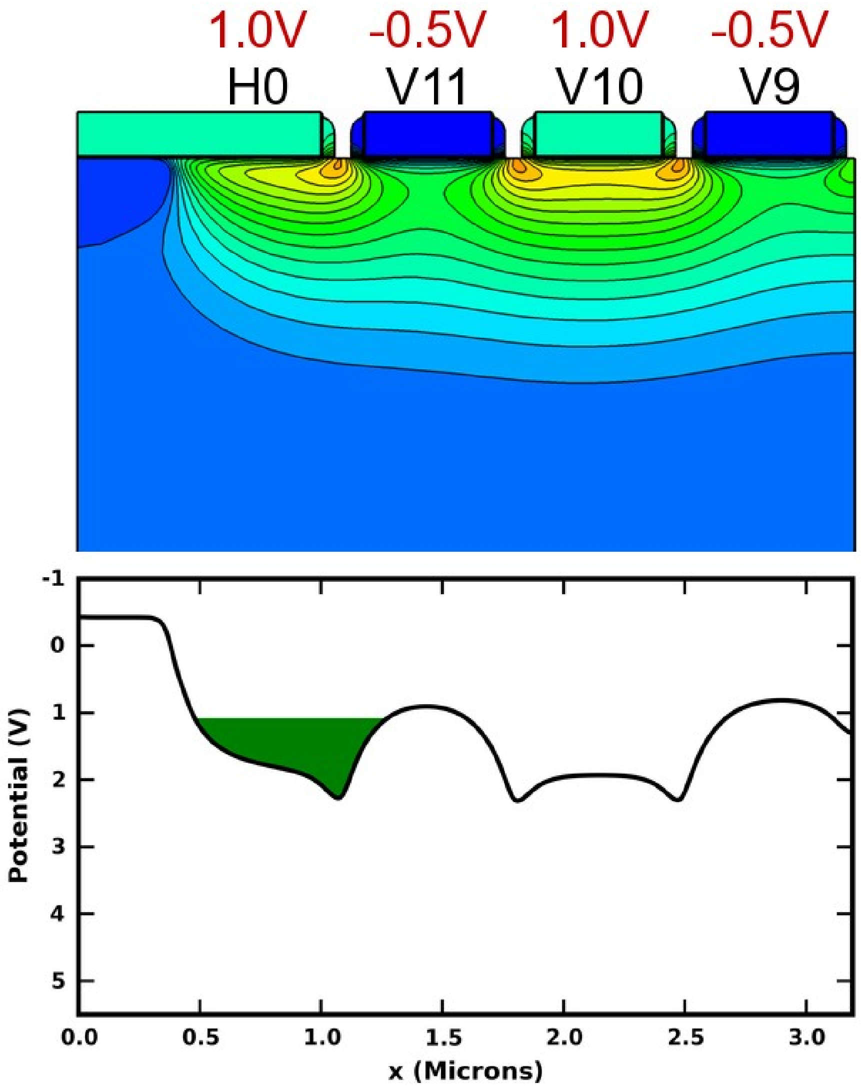


Odd column

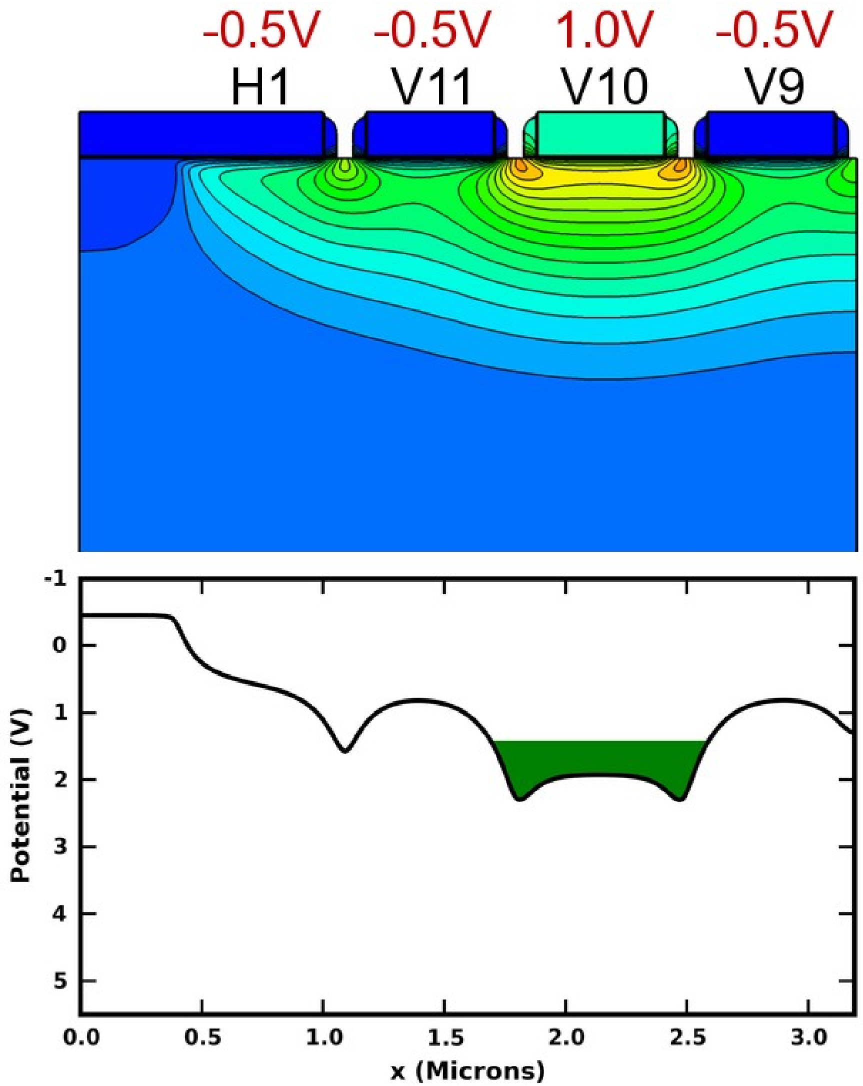


Vertical to Horizontal Transfer

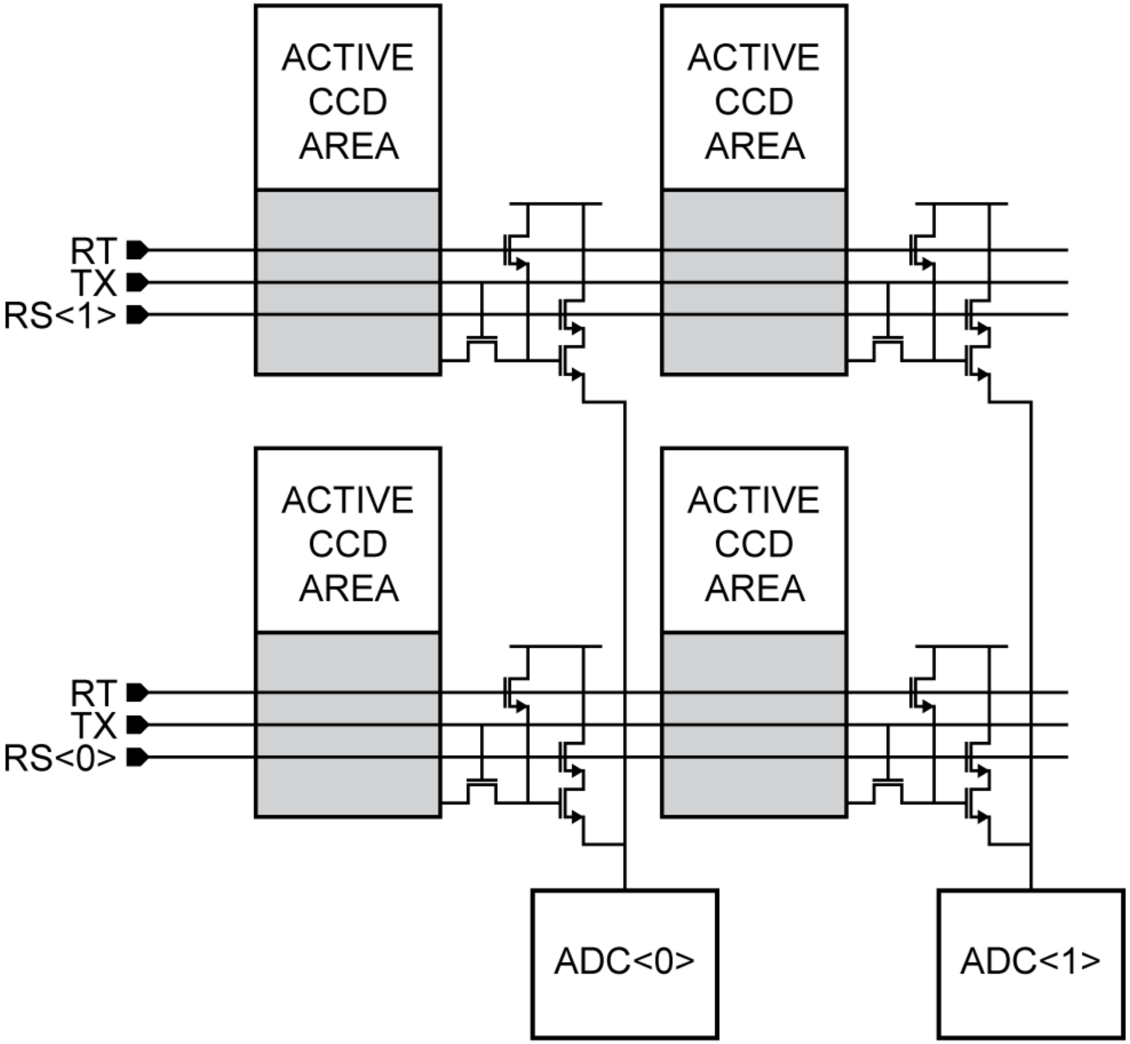
Even column



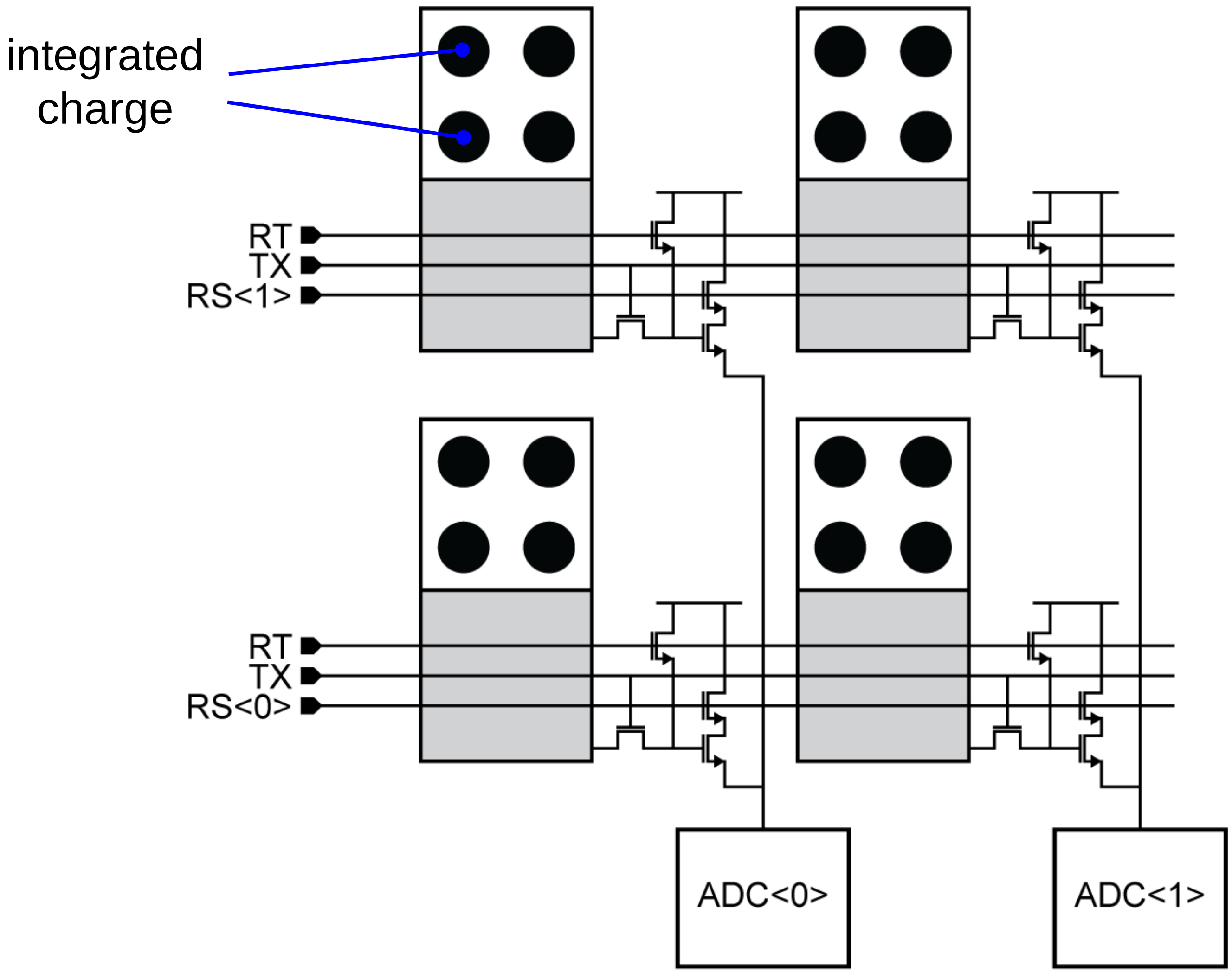
Odd column



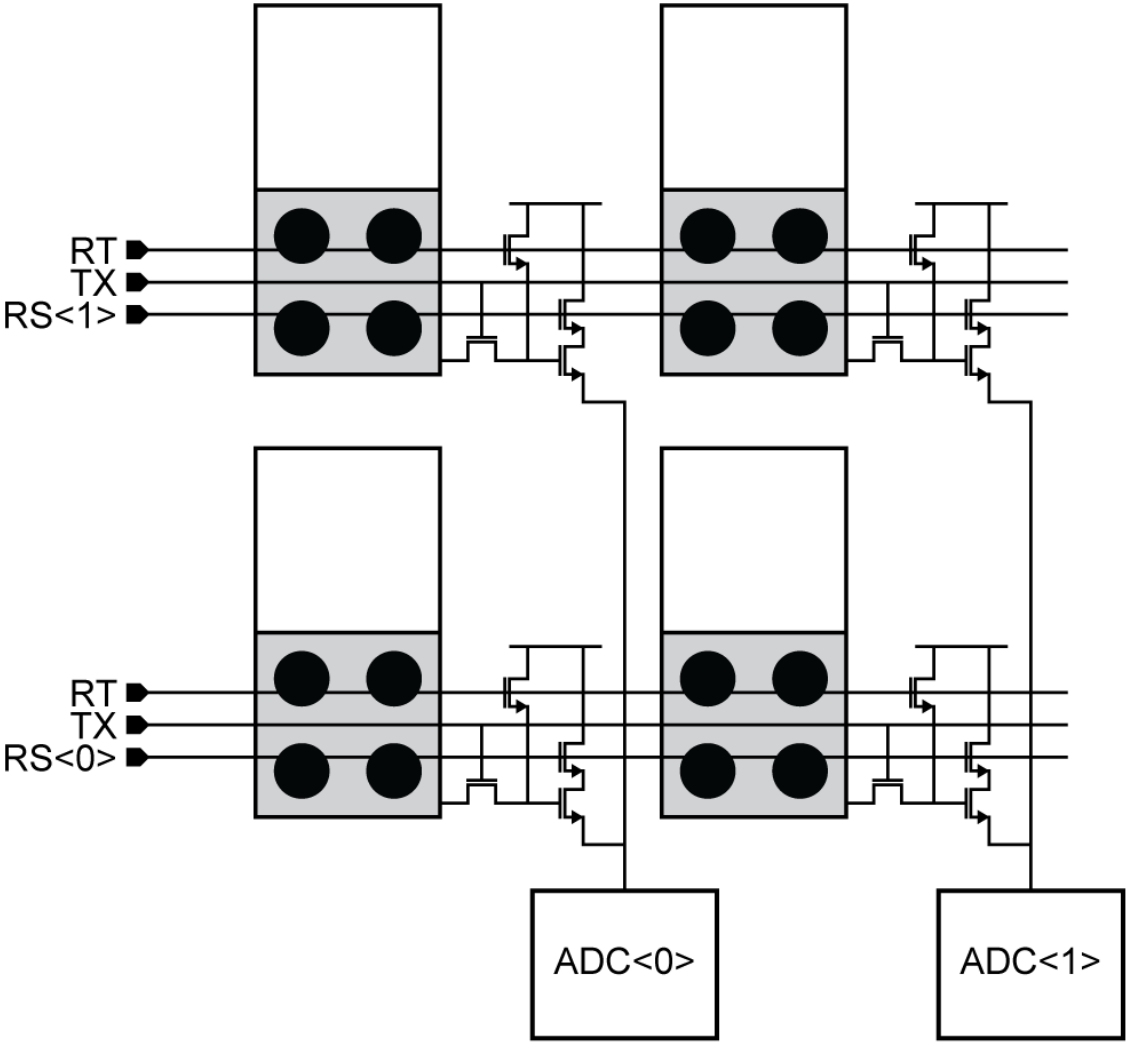
Chip Operation



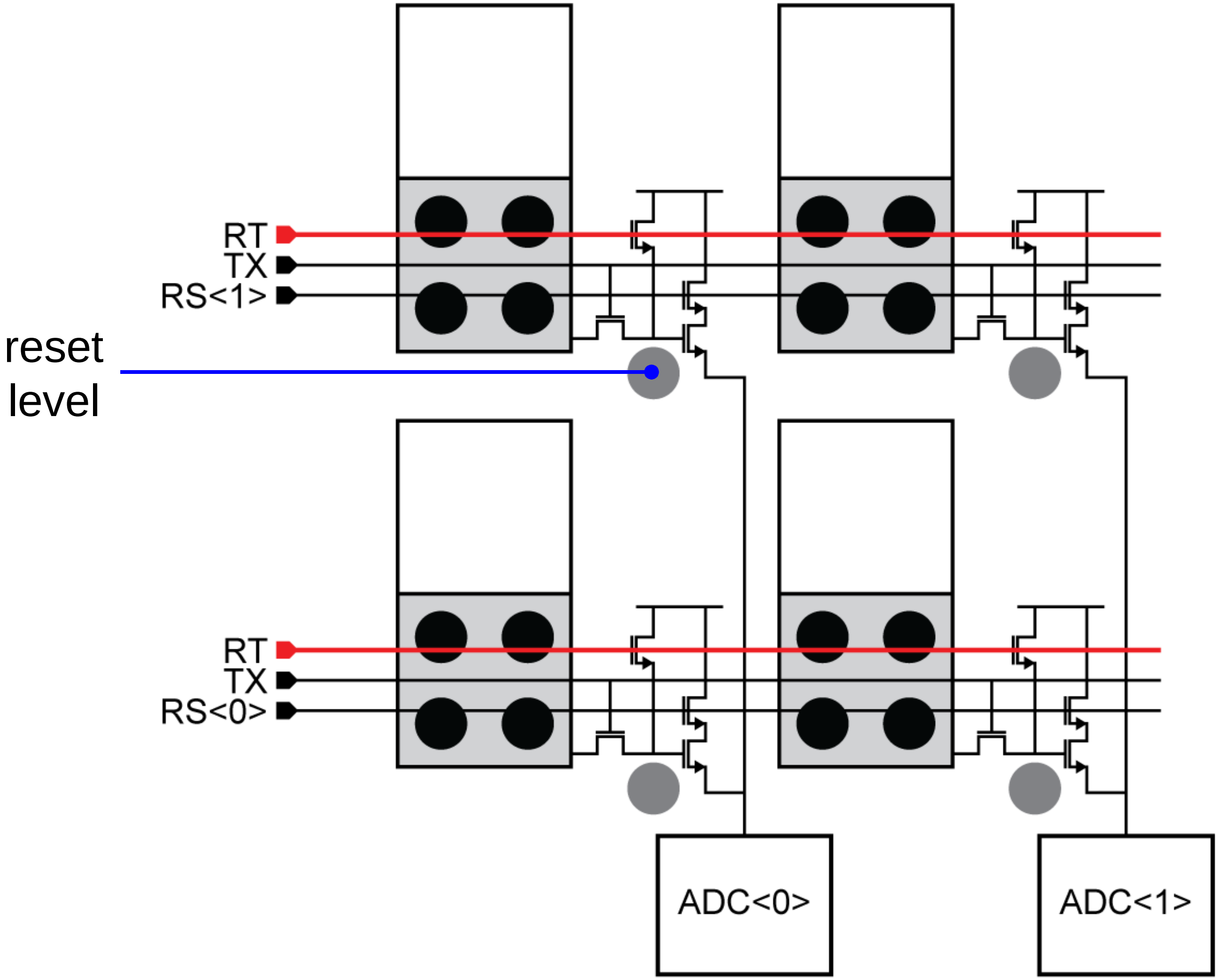
Chip Operation (Integrate)



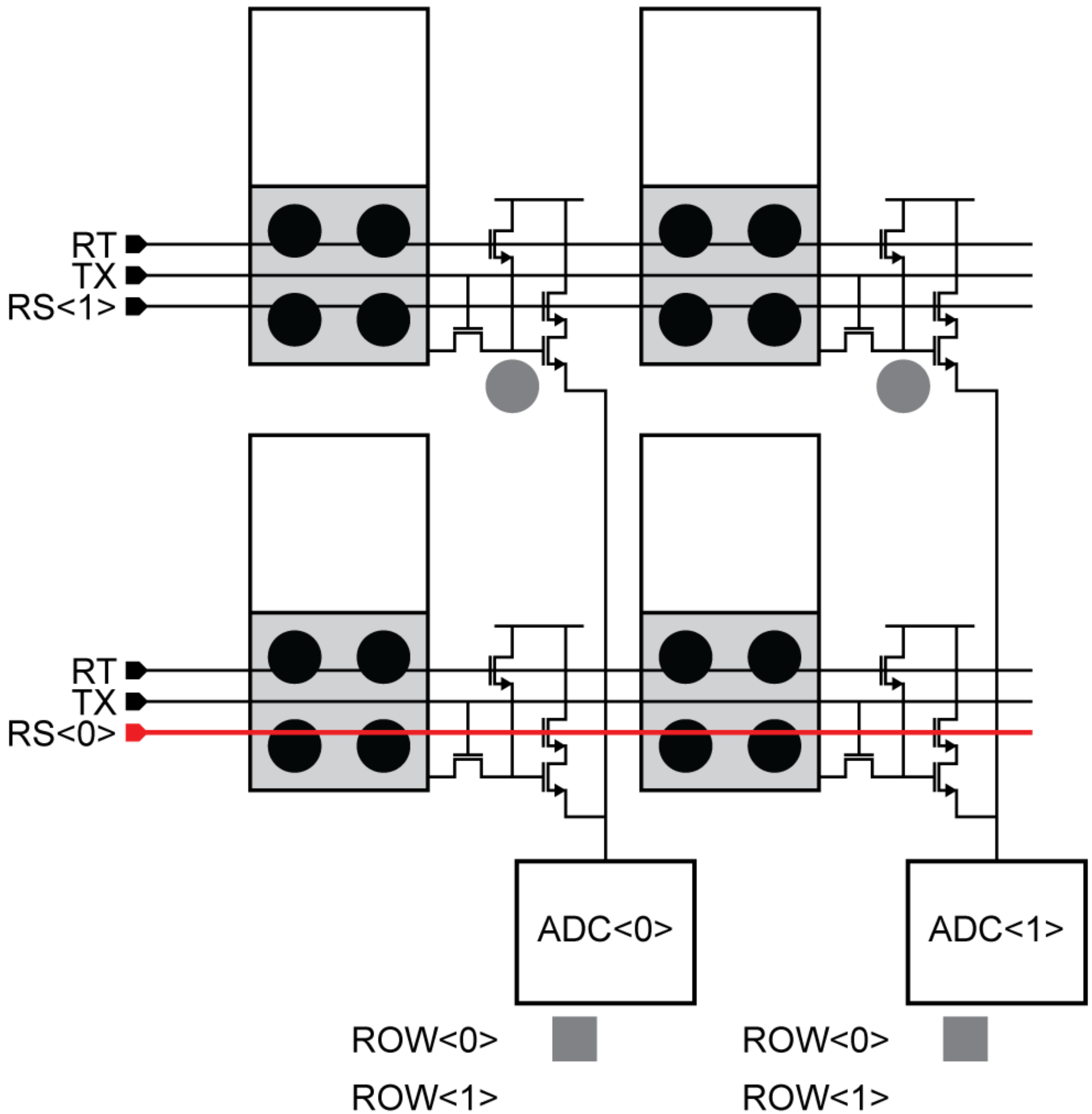
Chip Operation (Frame Transfer)



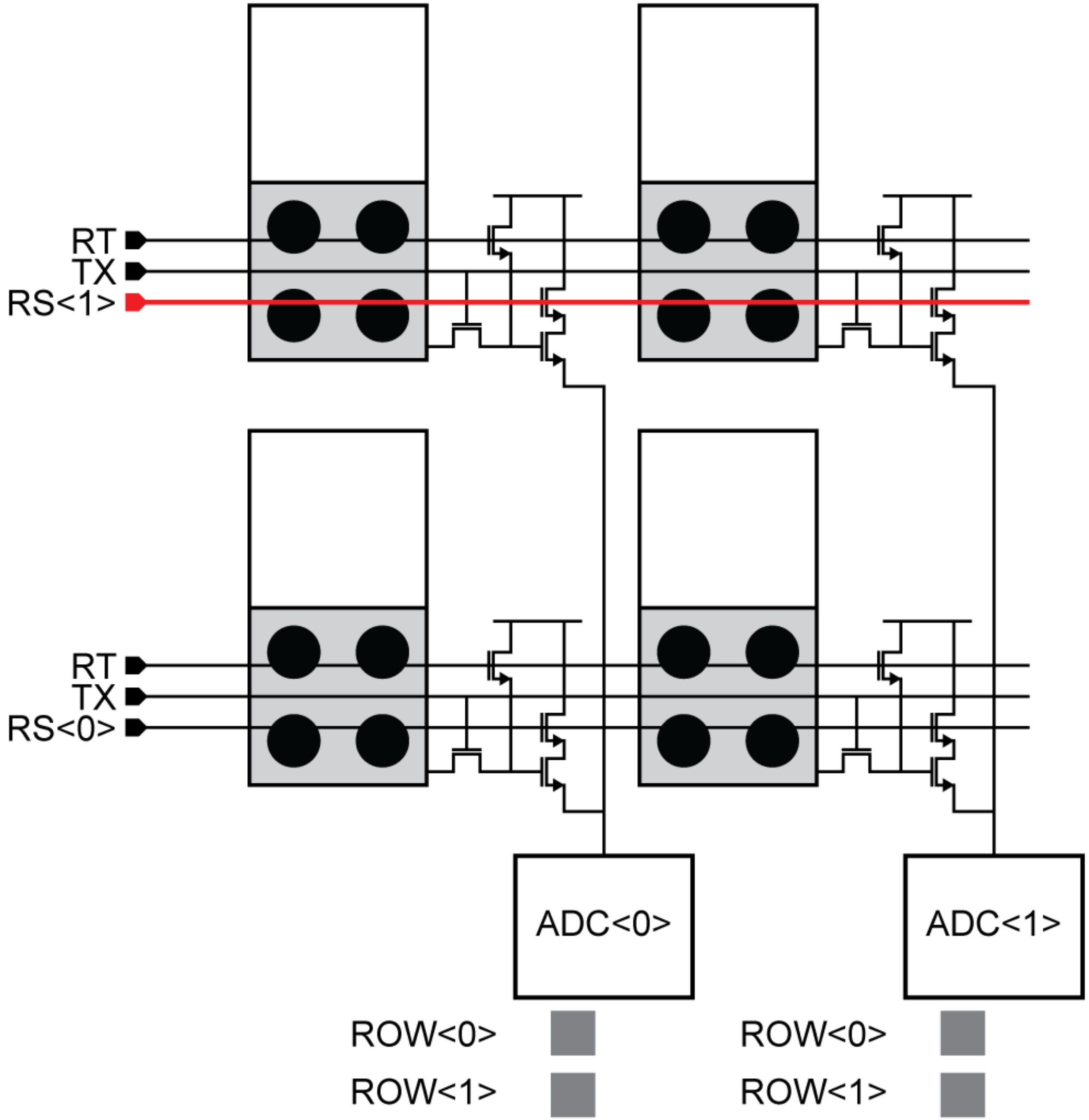
Chip Operation (Reset FD)



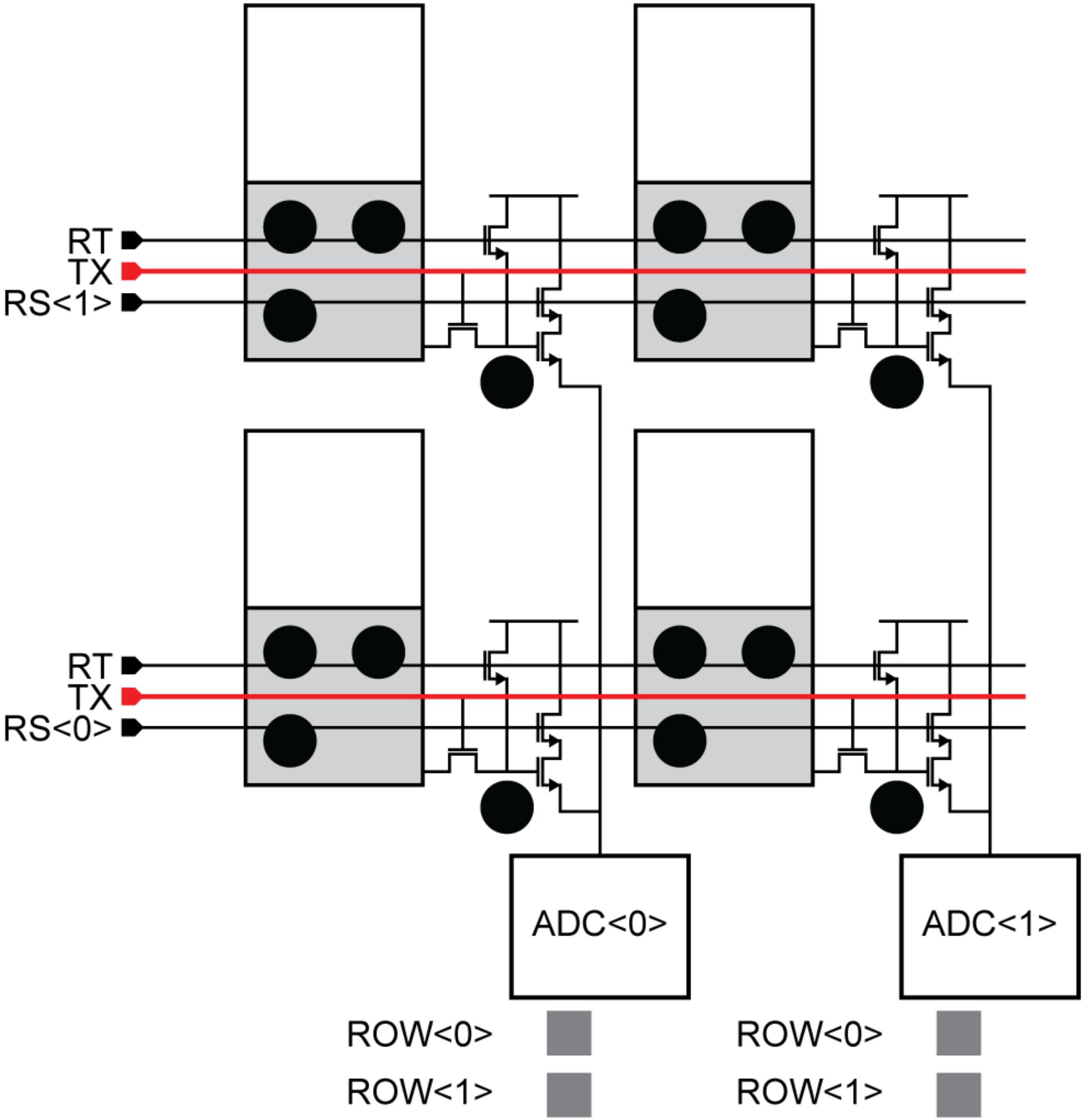
Chip Operation (Read Row<0>)



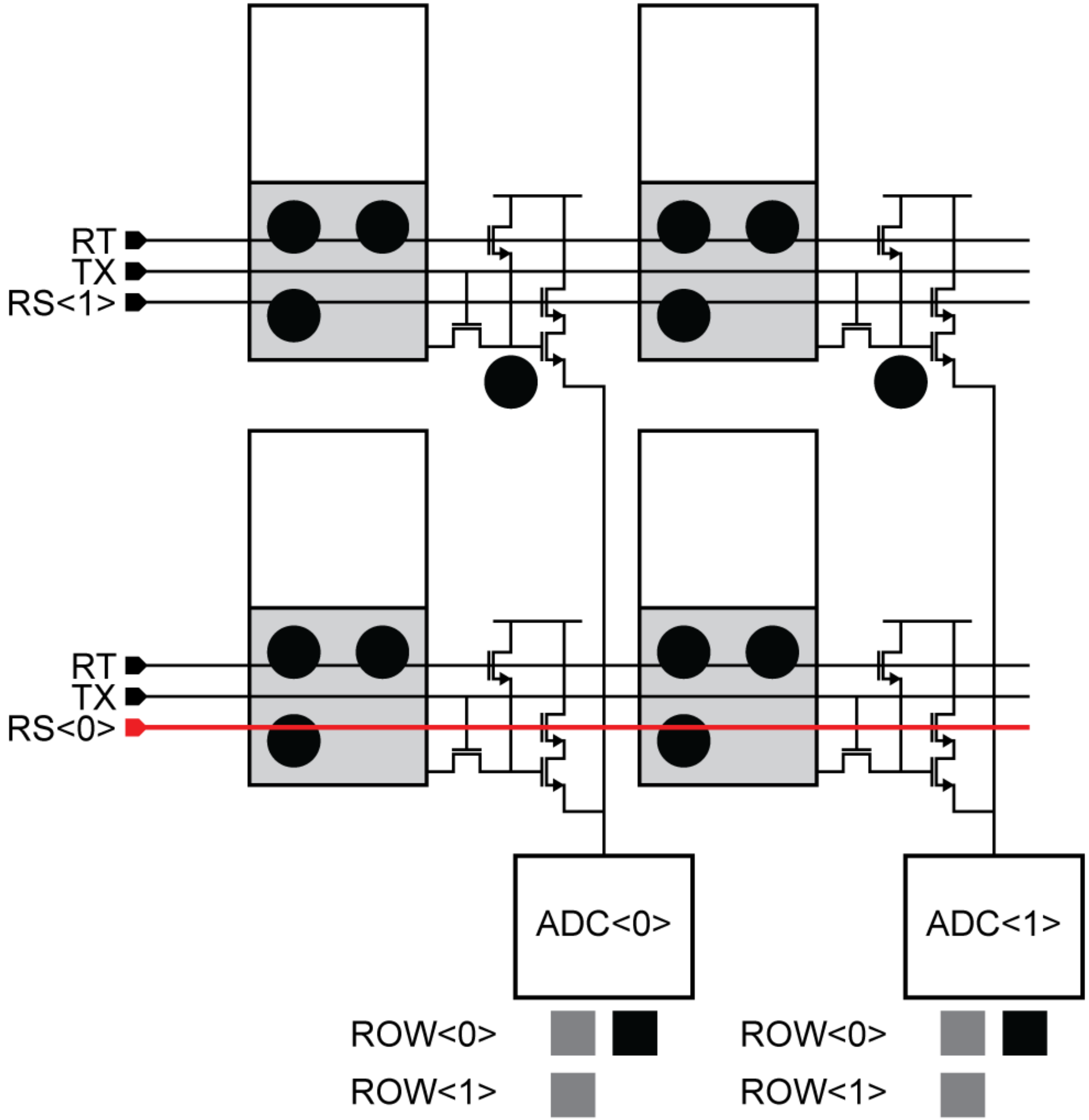
Chip Operation (Read Row<1>)



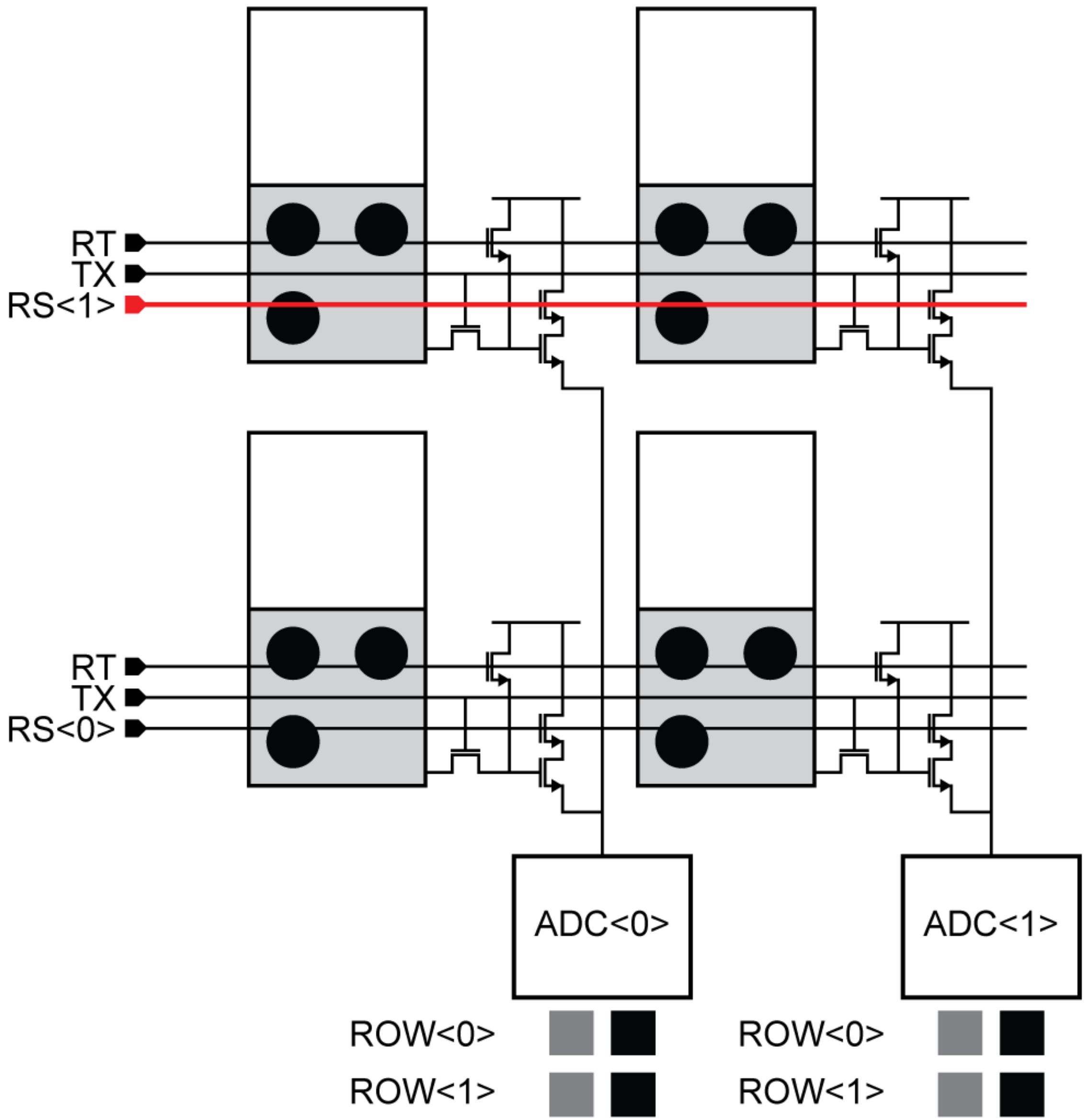
Chip Operation (Transfer Charge)



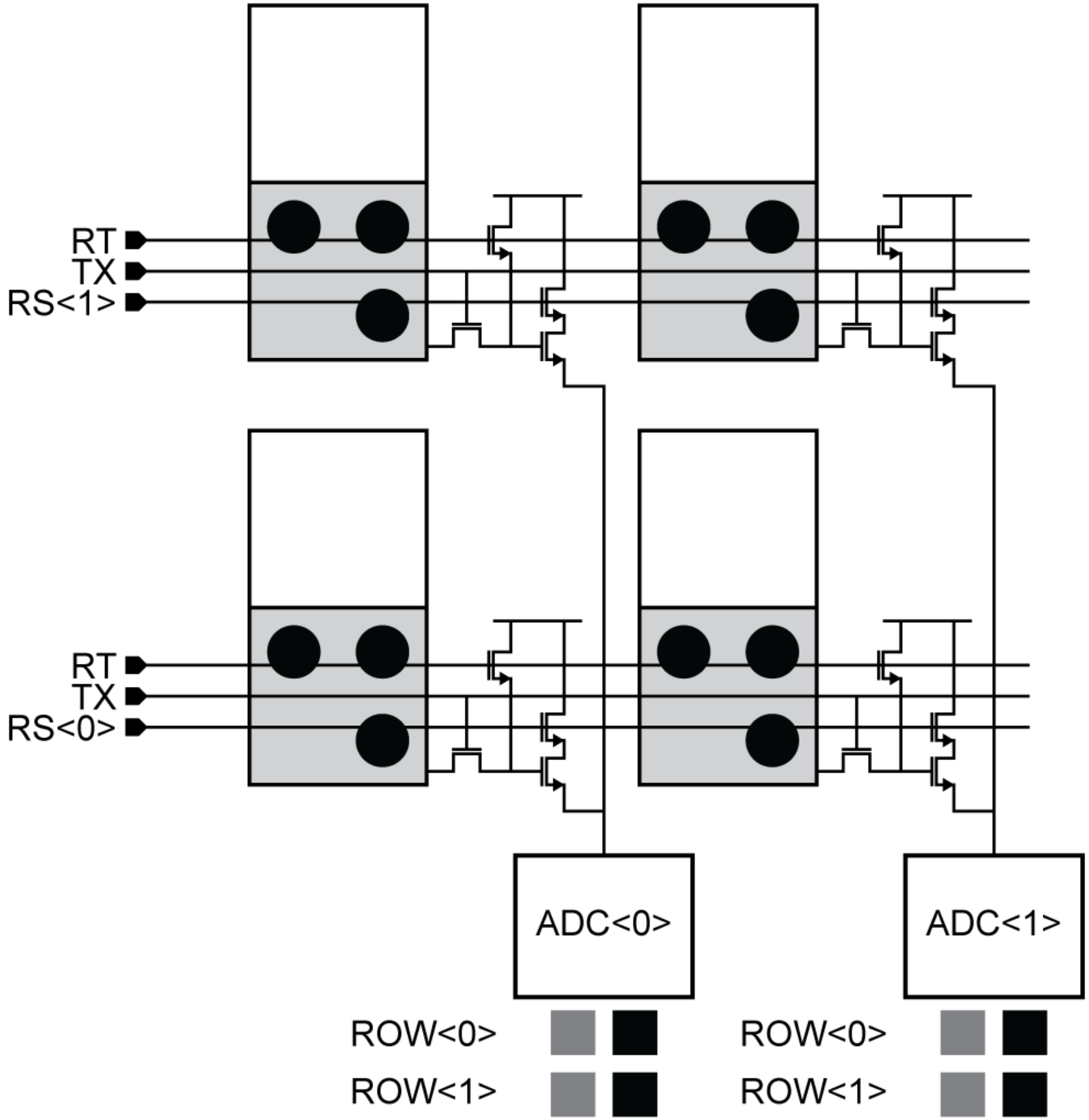
Chip Operation (Charge Row<0>)



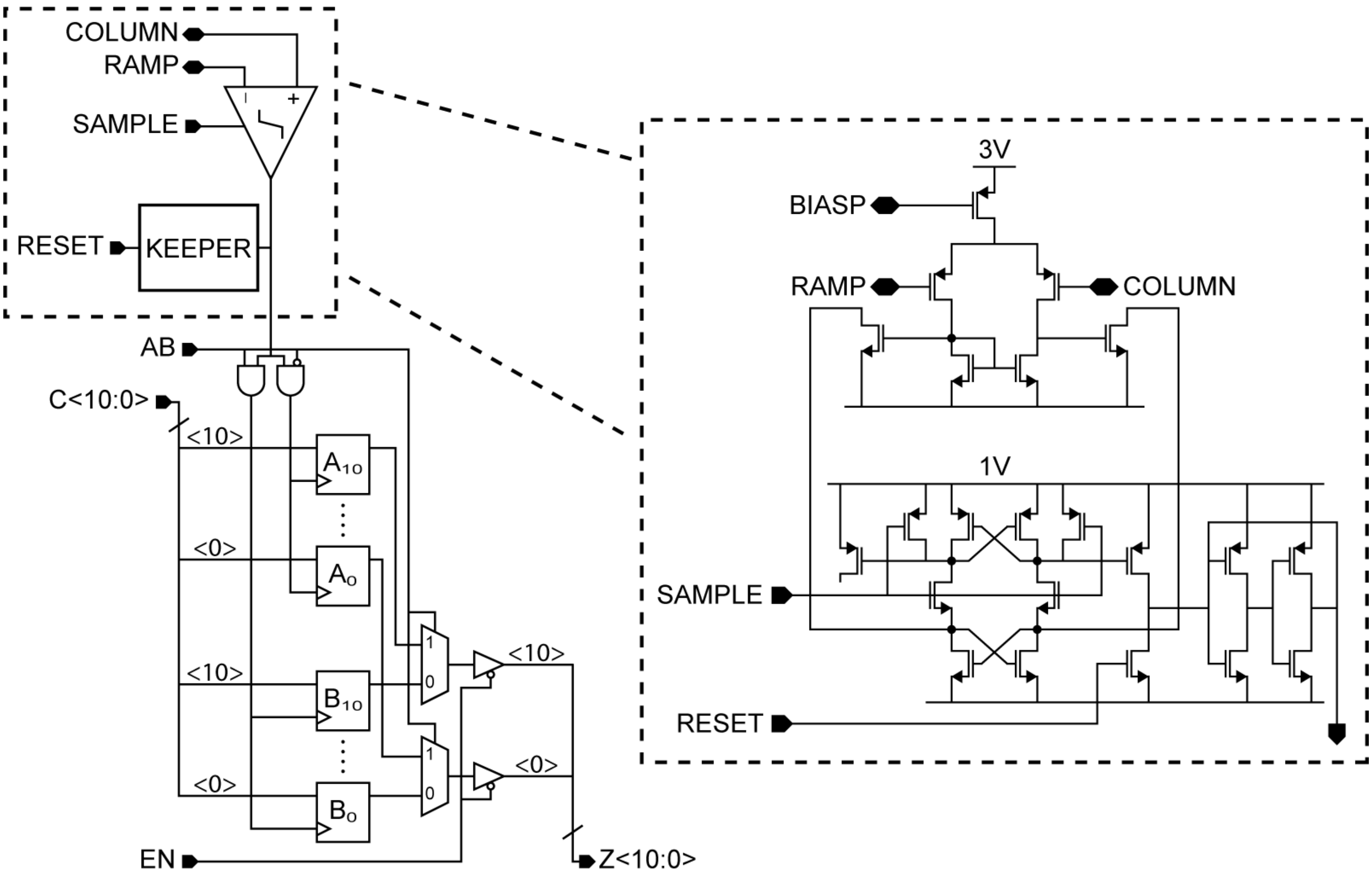
Chip Operation (Charge Row<1>)



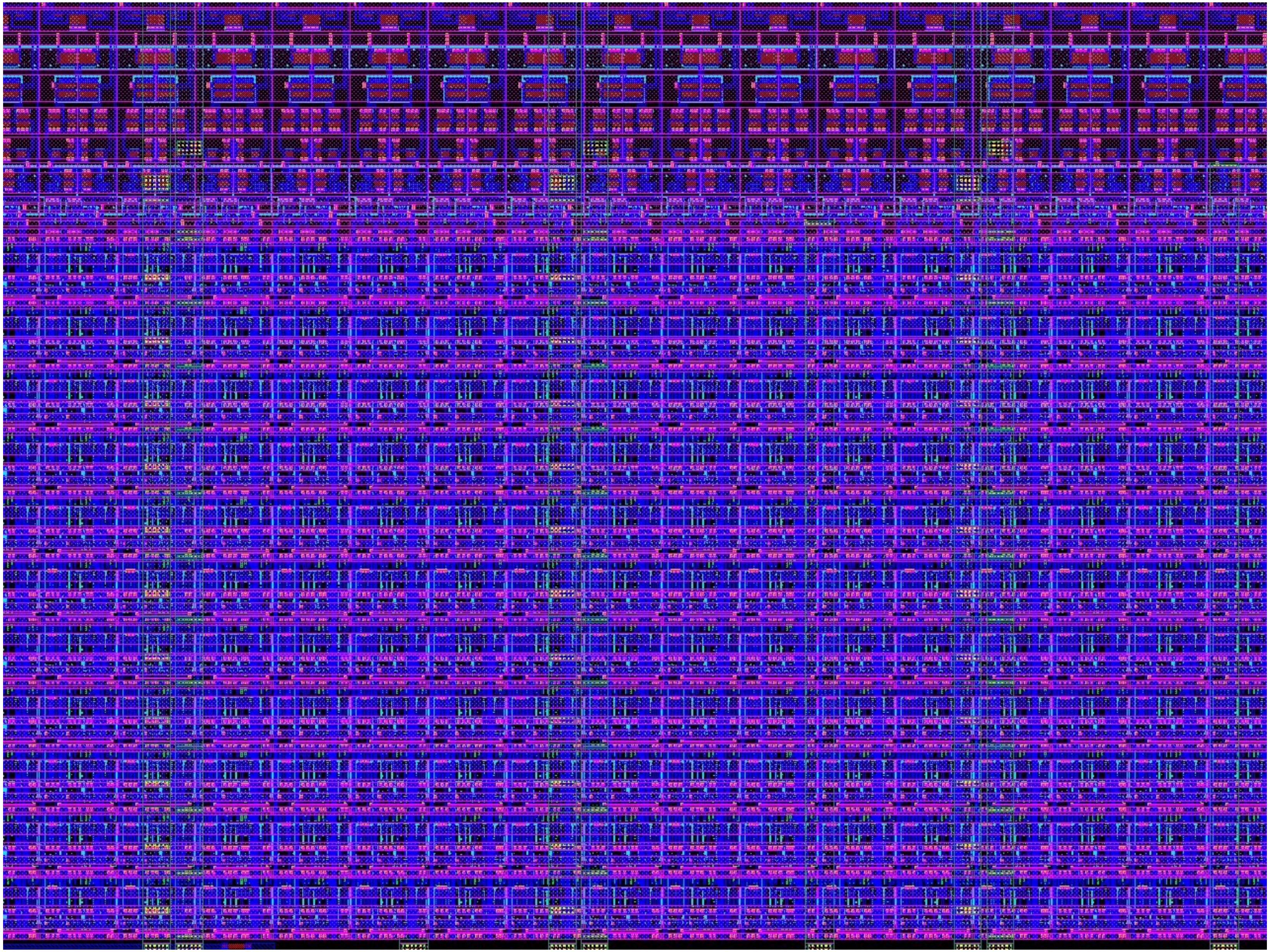
Chip Operation (Shift Charge)



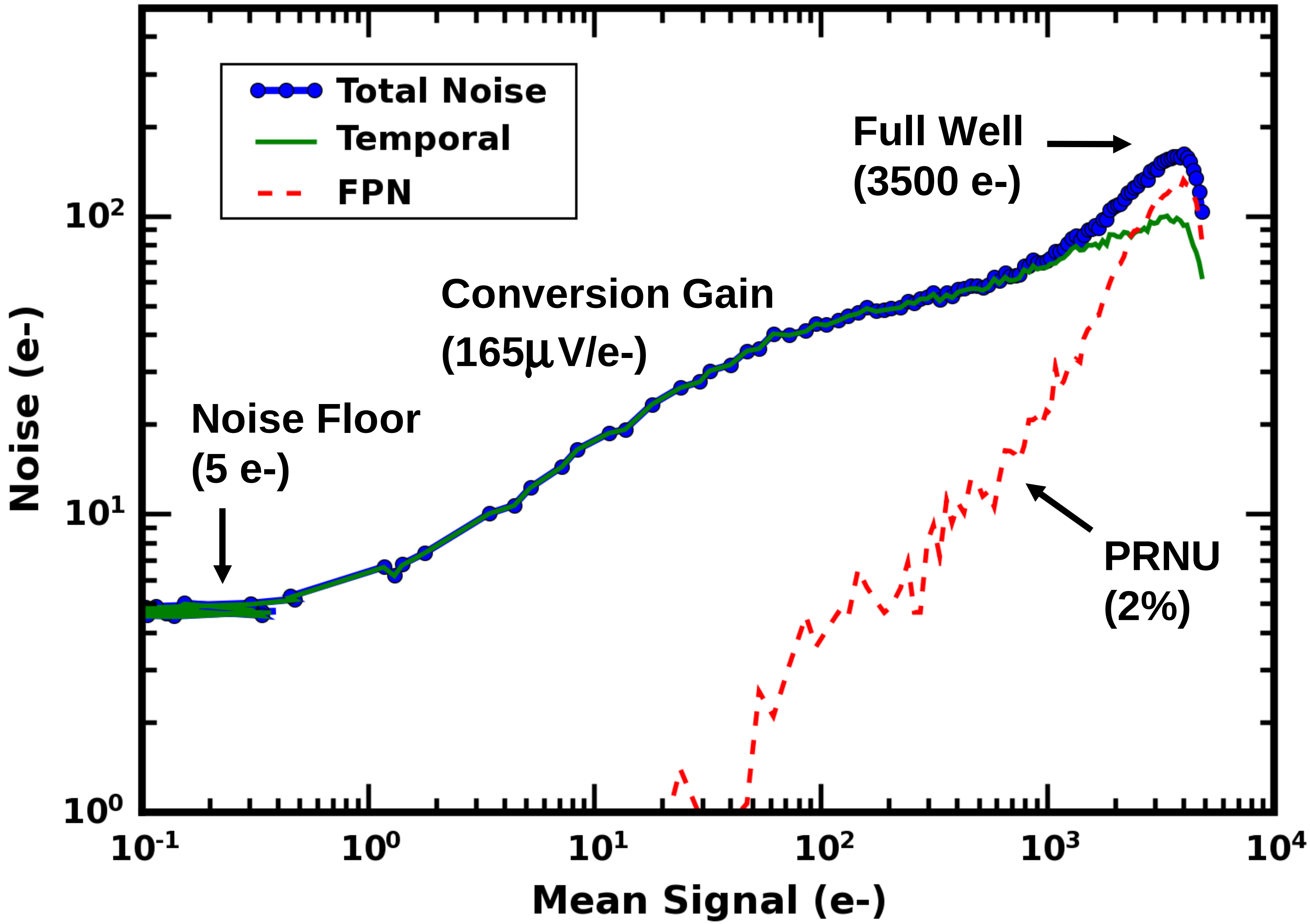
Column ADC Schematic



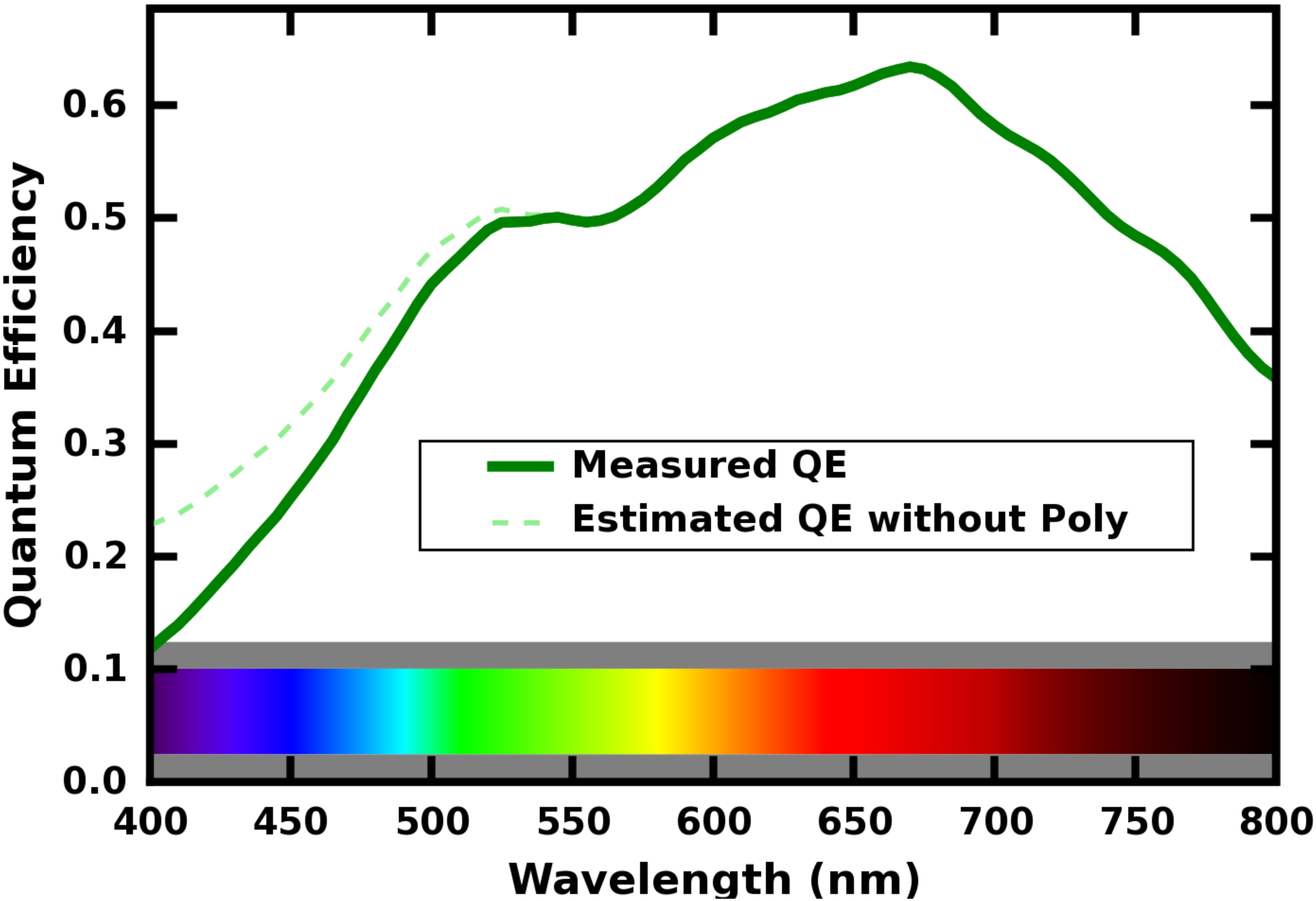
Layout Masks for ADC



Photon Transfer Curve (0.7μm Pixel)



Measured Quantum Efficiency

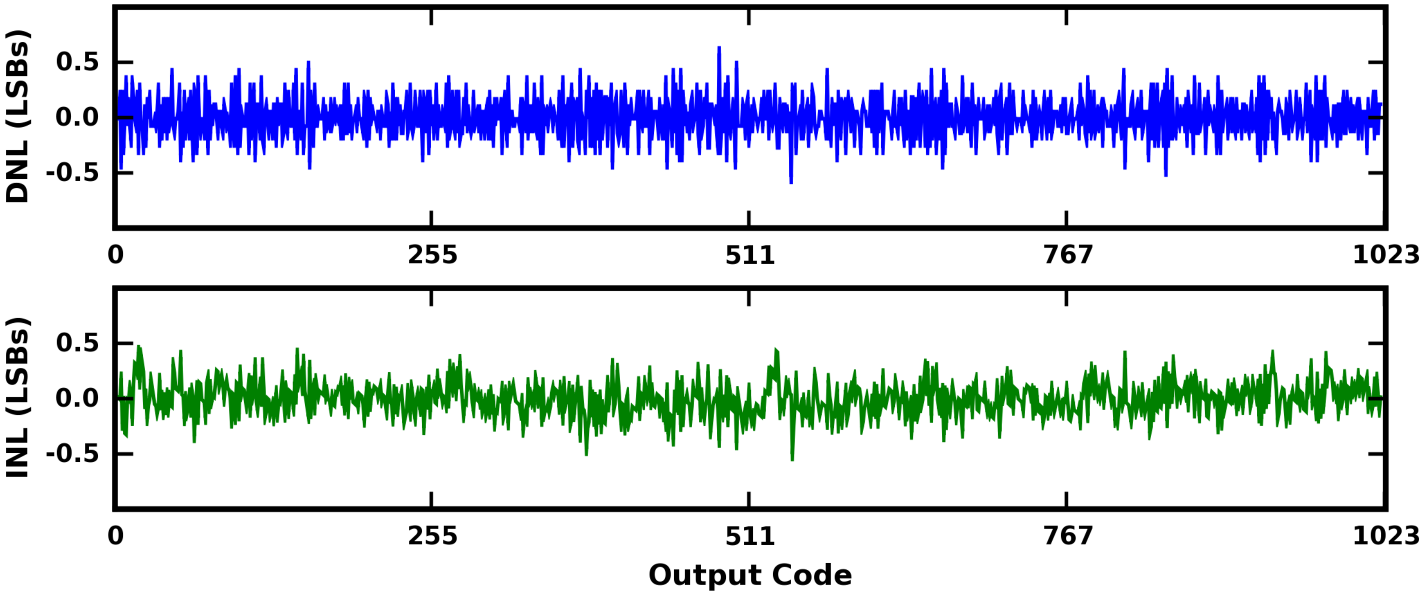


Measured Pixel Characteristics

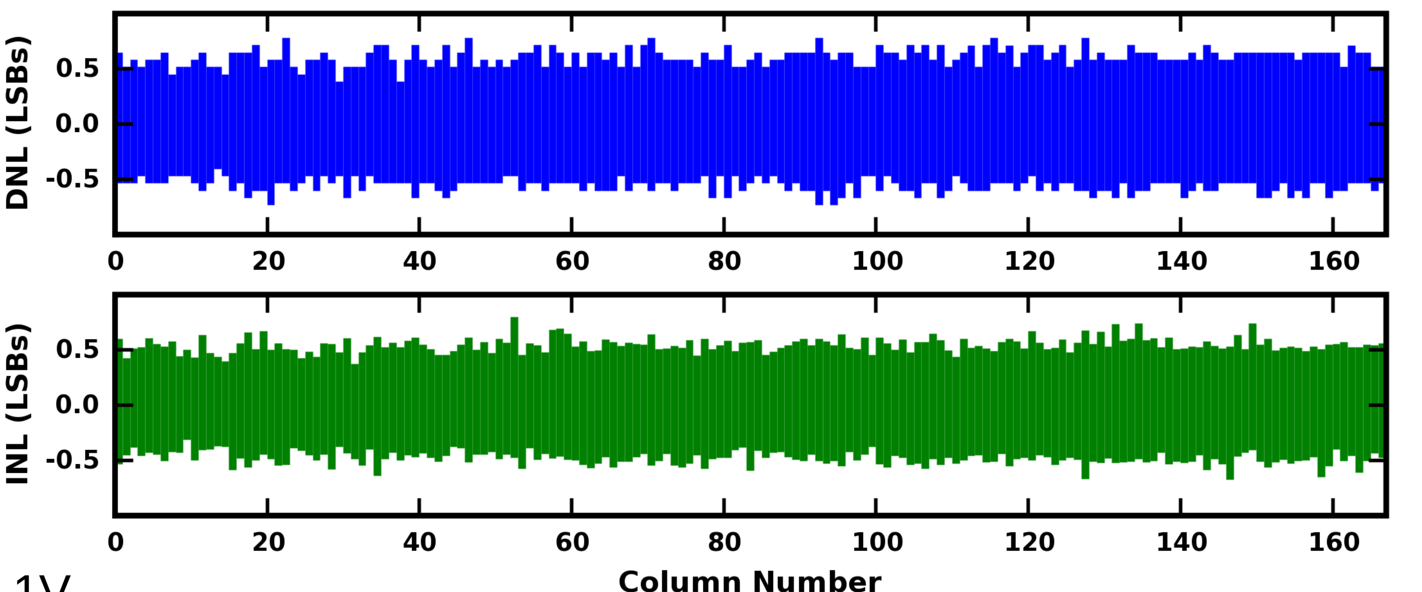
Well capacity	3500 e-
Conversion gain	165 μV/e-
Sensitivity at 550 nm	0.15V/lux-sec
QE at 450, 550, 650 nm	20, 48, 65 %
Pixel read noise	5 e- rms (1mV)
Dark current at RT	33 e-/sec (5.5 mV/sec)
DSNU	35 % rms
PRNU	2 % rms
Peak SNR	35 dB
Dynamic range	57 dB

Measured ADC Linearity

Single Column (10-b)

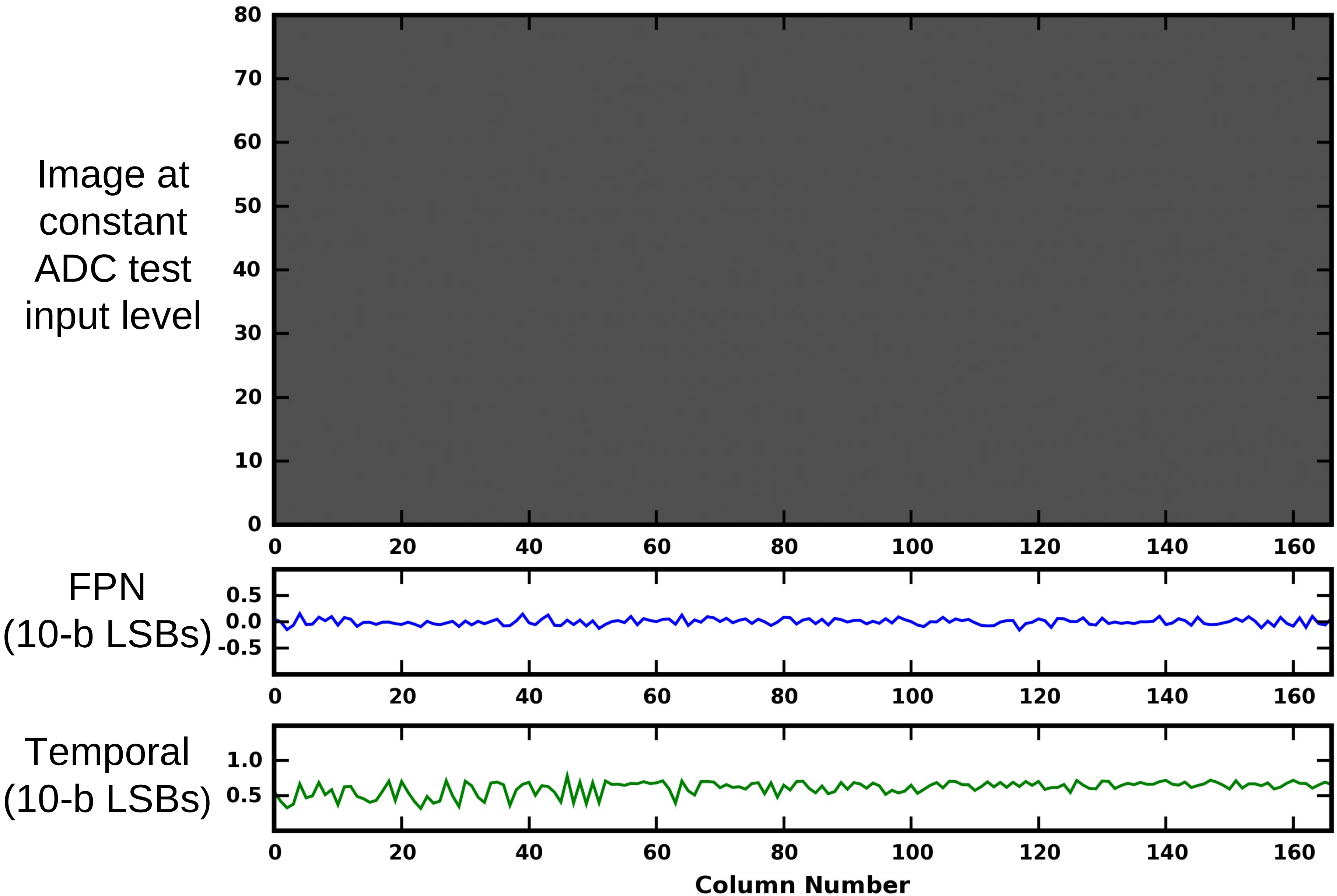


All Columns (10-b)

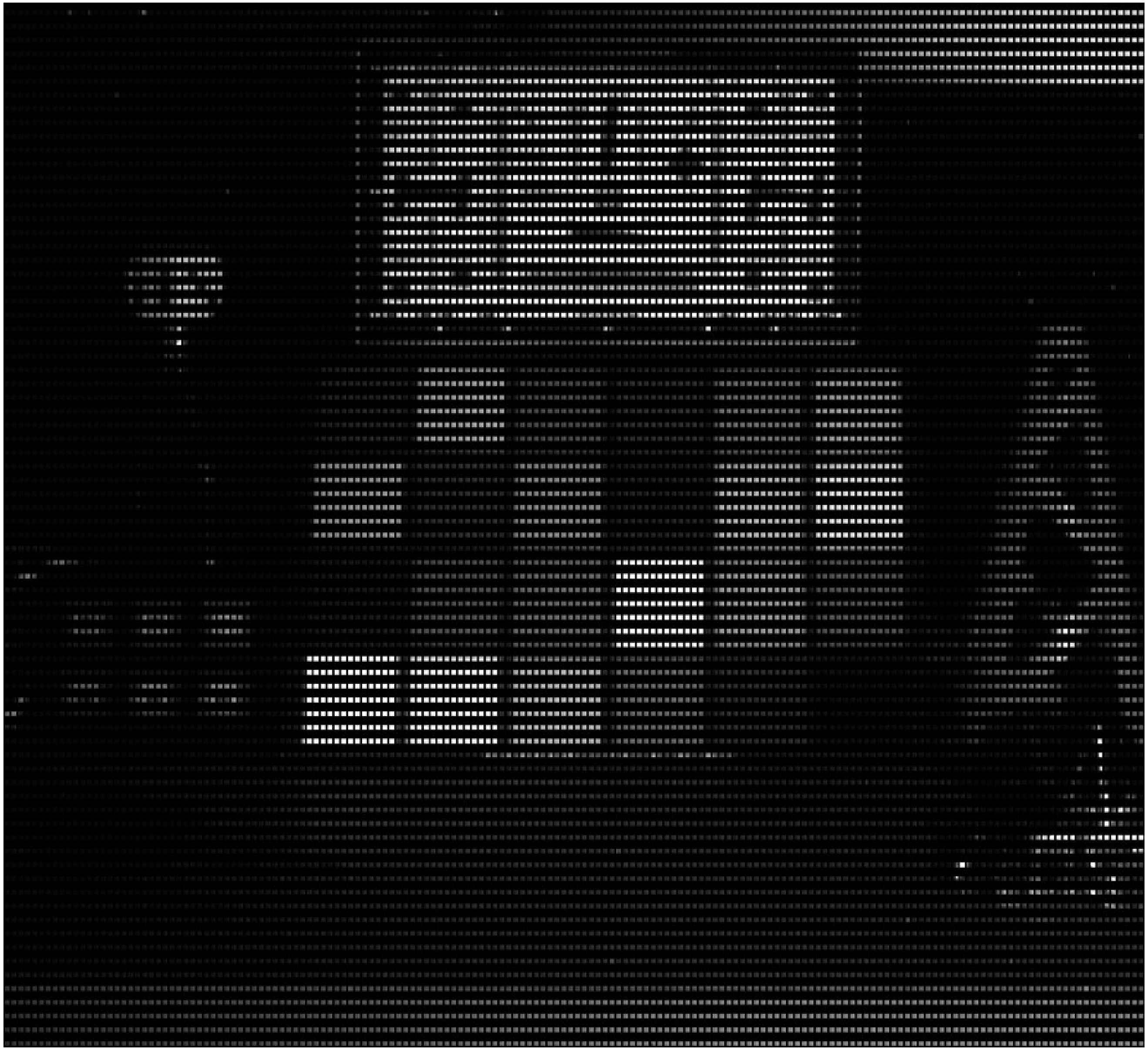


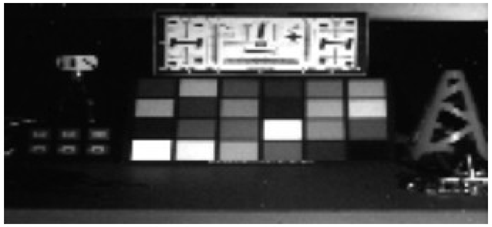
Input Range = 1V

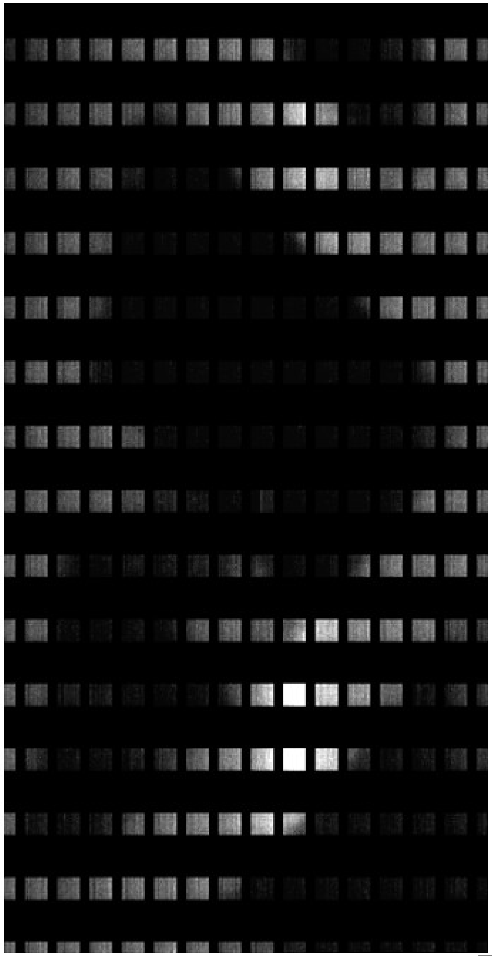
Measured ADC Noise



Sample Image

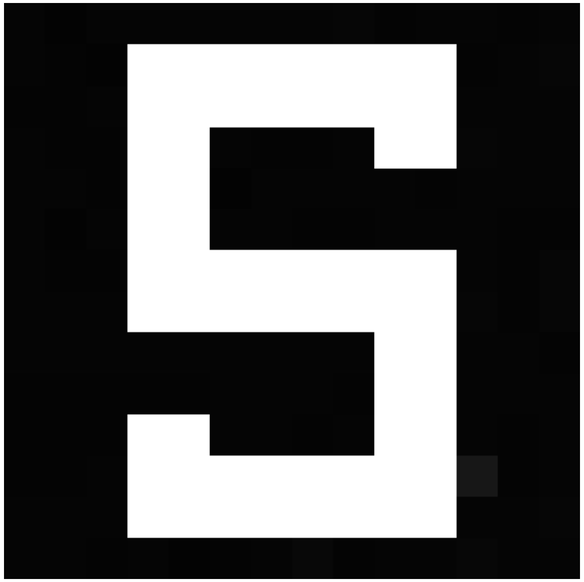






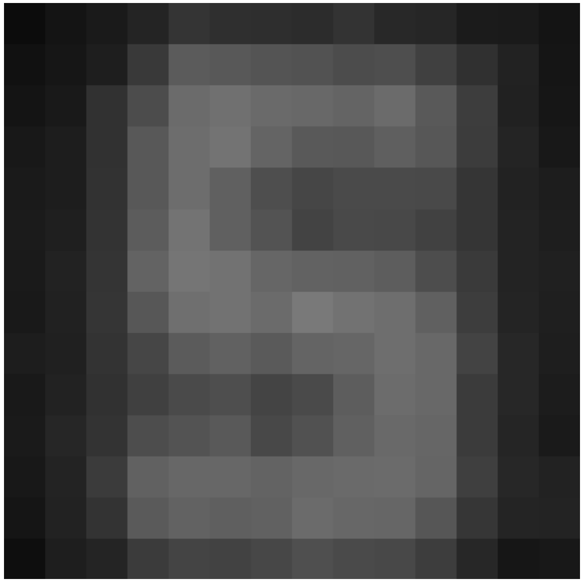
Images from Single Subarray

Electrical



3000 electron charge packets from fill/spill input

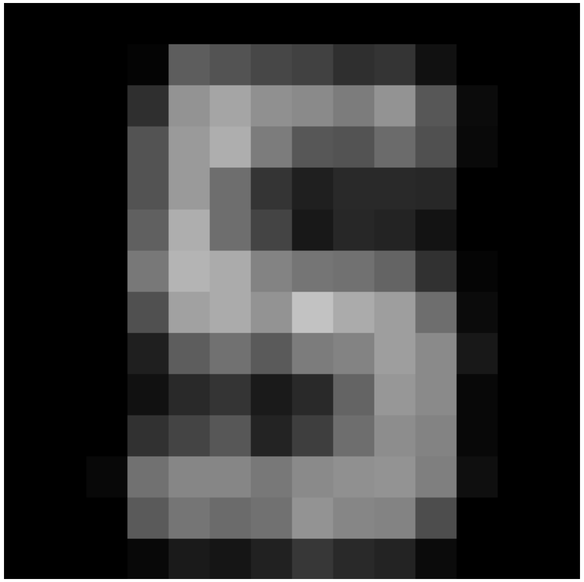
Optical



Raw data

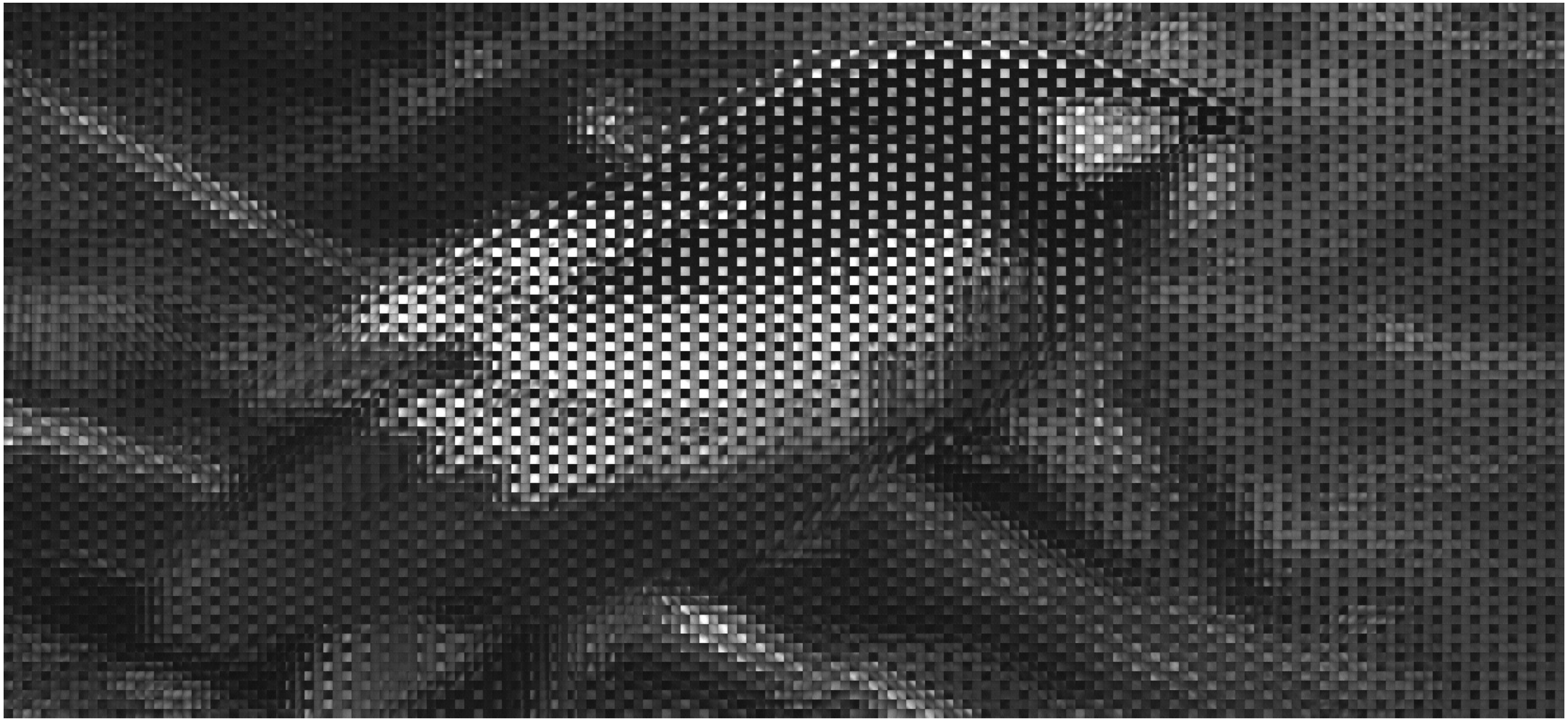
Captured with F/2.8, f=6mm lens at 1/10 sec

Optical



Added contrast

Raw Image Captured with Multi-Aperture Views



Processed Multi-Aperture Image

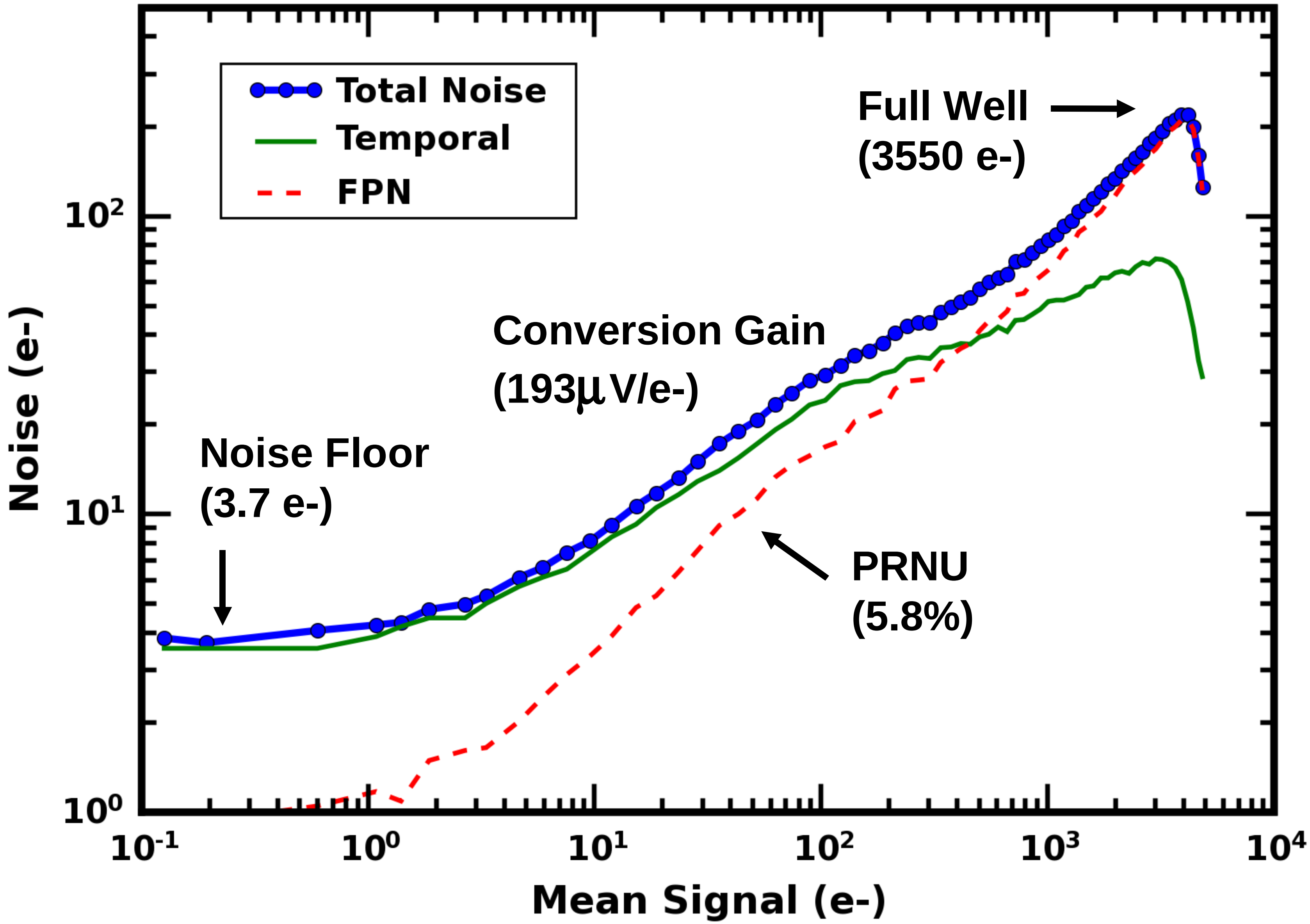
Summary

- Designed and characterized the first integrated multi-aperture image sensor
- Achieved good imaging performance with submicron pixels
  - FT-CCD structure in deep submicron CMOS
  - Ripple charge transfer
- Extensible architecture well suited for ultra-high pixel count imagers
- Many potential applications or benefits
  - Depth
  - Close proximity imaging
  - Color imaging with good spectral separation
  - High defect tolerance
  - Relaxed external optical requirements
- Results suggest that further scaling while maintaining performance is possible

Acknowledgement

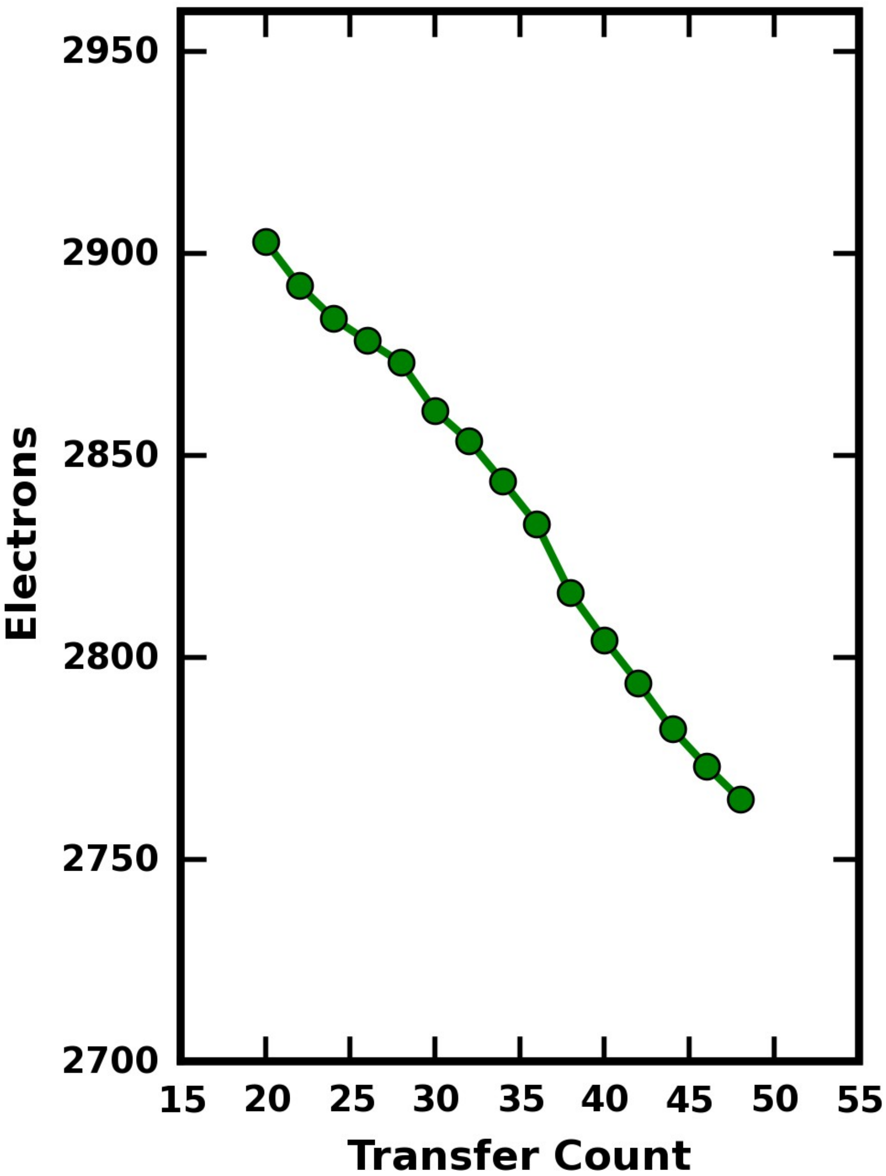
- Orals Committee
  - Abbas El Gamal
  - H.-S. Philip Wong
  - Bruce Wooley
  - Mark Horowitz
- Stanford University
  - Outstanding people and resources
- Hertz Foundation
  - Fellowship support
- TSMC
  - C.H. Tseng, David Yen, C.Y. Ko, J.C. Liu, Ming Li, and S.G. Wuu for process customization and fabrication
- Lane Brooks, MIT EECS
  - Collaboration on the design of the testing platform and software system
- GNU/Linux, FSF, open source community
  - Providing the best software development tools

Photon Transfer Curve (0.5μm Pixel)



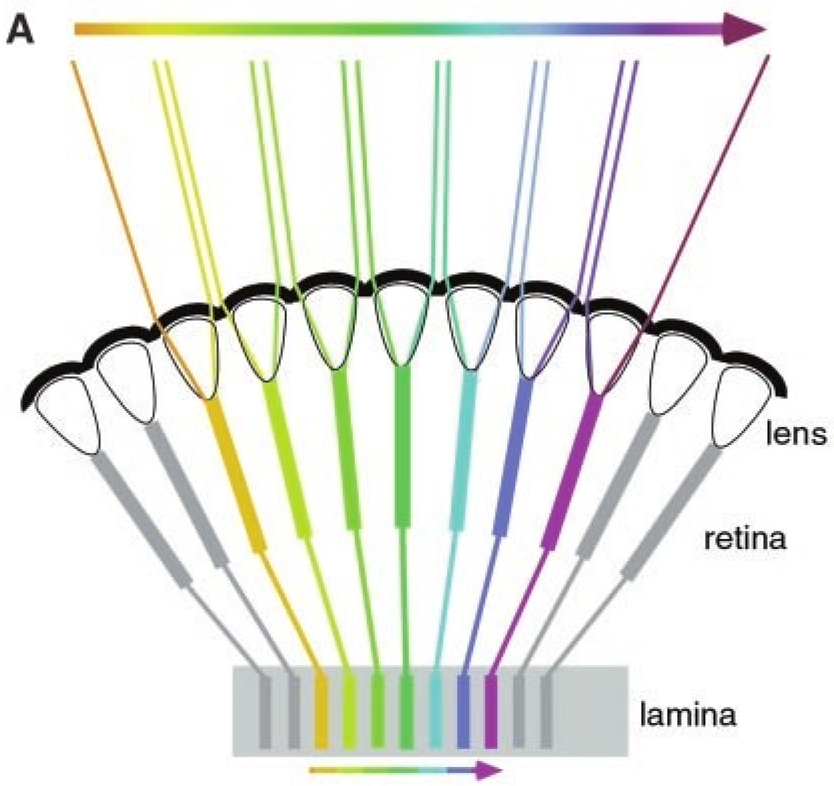
Measured Charge Transfer Efficiency

- CTE is 99.9% with 3000 electron charge packets
- CTE limited by surface interface traps
- CTE is reduced to 98% if holes are accumulated between storage electrodes.



Is There a Biological Equivalent?

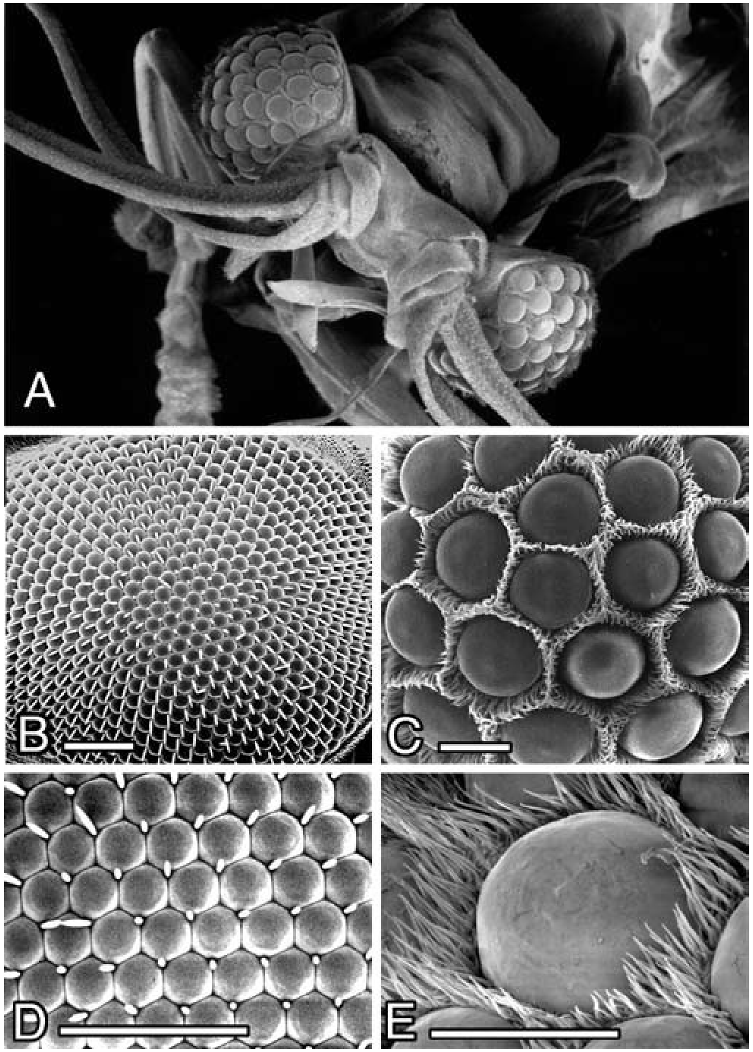
Compound Eye

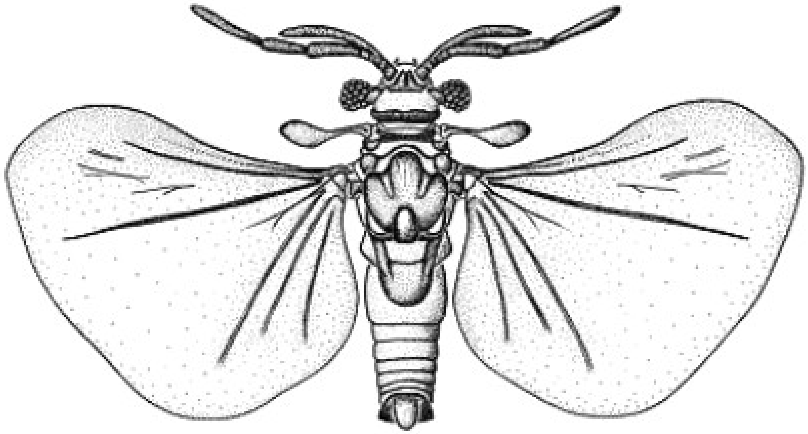


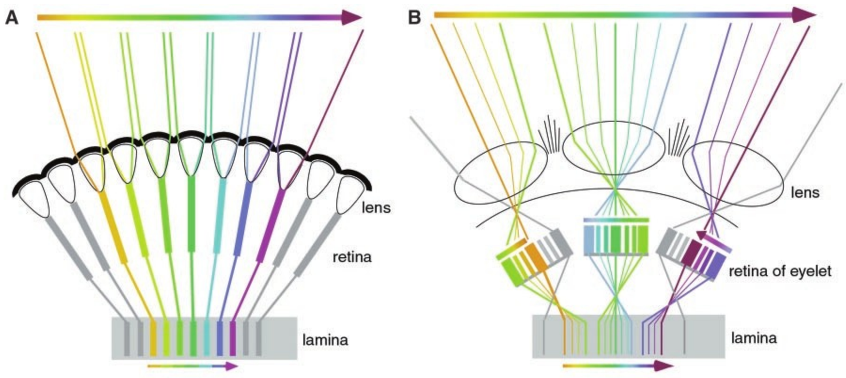
* *Wikipedia, Compound Eye*

* *Buschbeck, 1999*

Eye of the Strepsiptera







** Buschbeck, 1999*