Design and Characterization of Submicron CCDs in CMOS

2009 International Image Sensor Workshop

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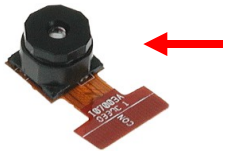
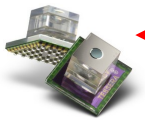
Camera History





- Despite progress, each of these cameras form images in the same way

Image Formation in a Camera

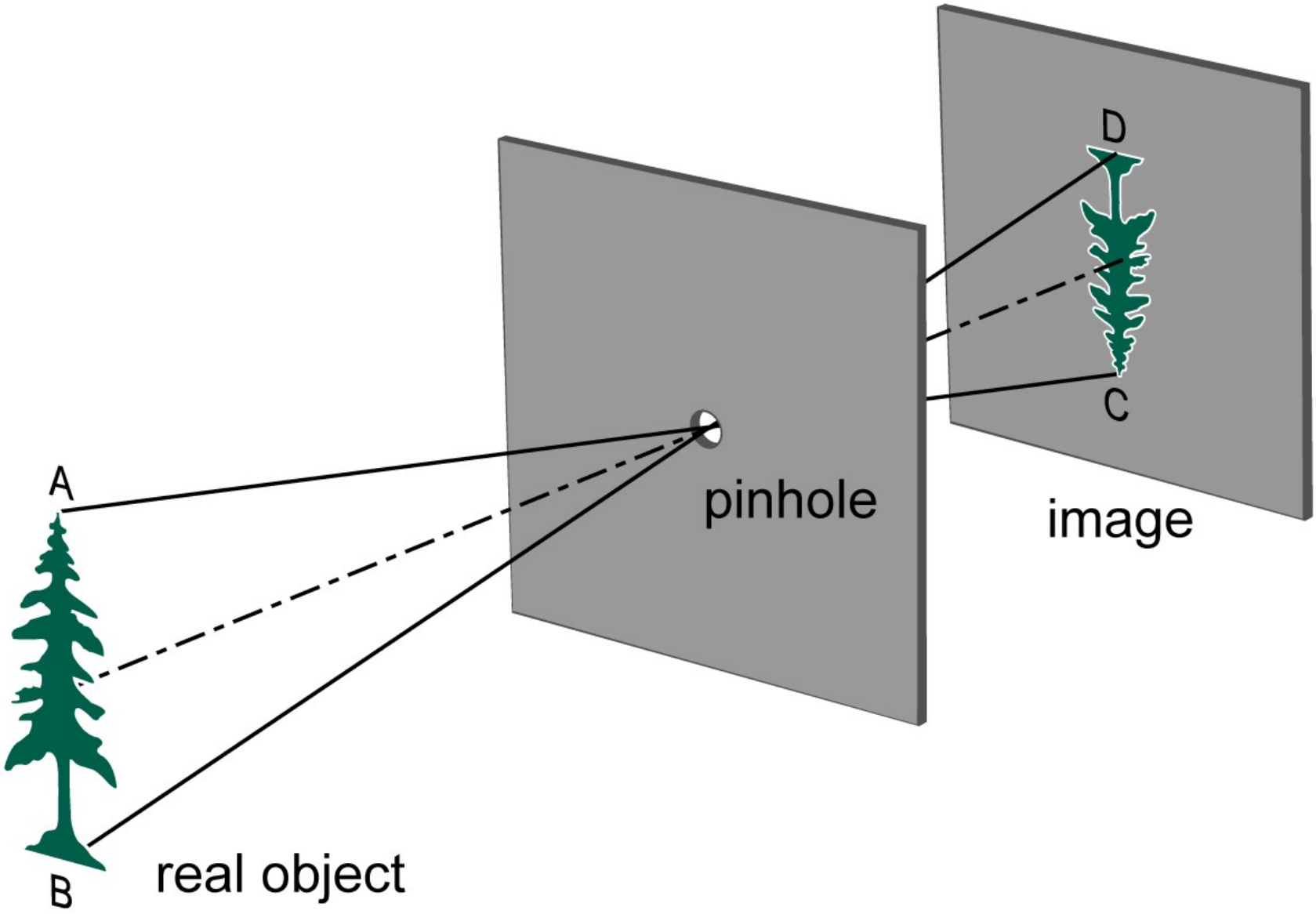


Image Formation in a Camera

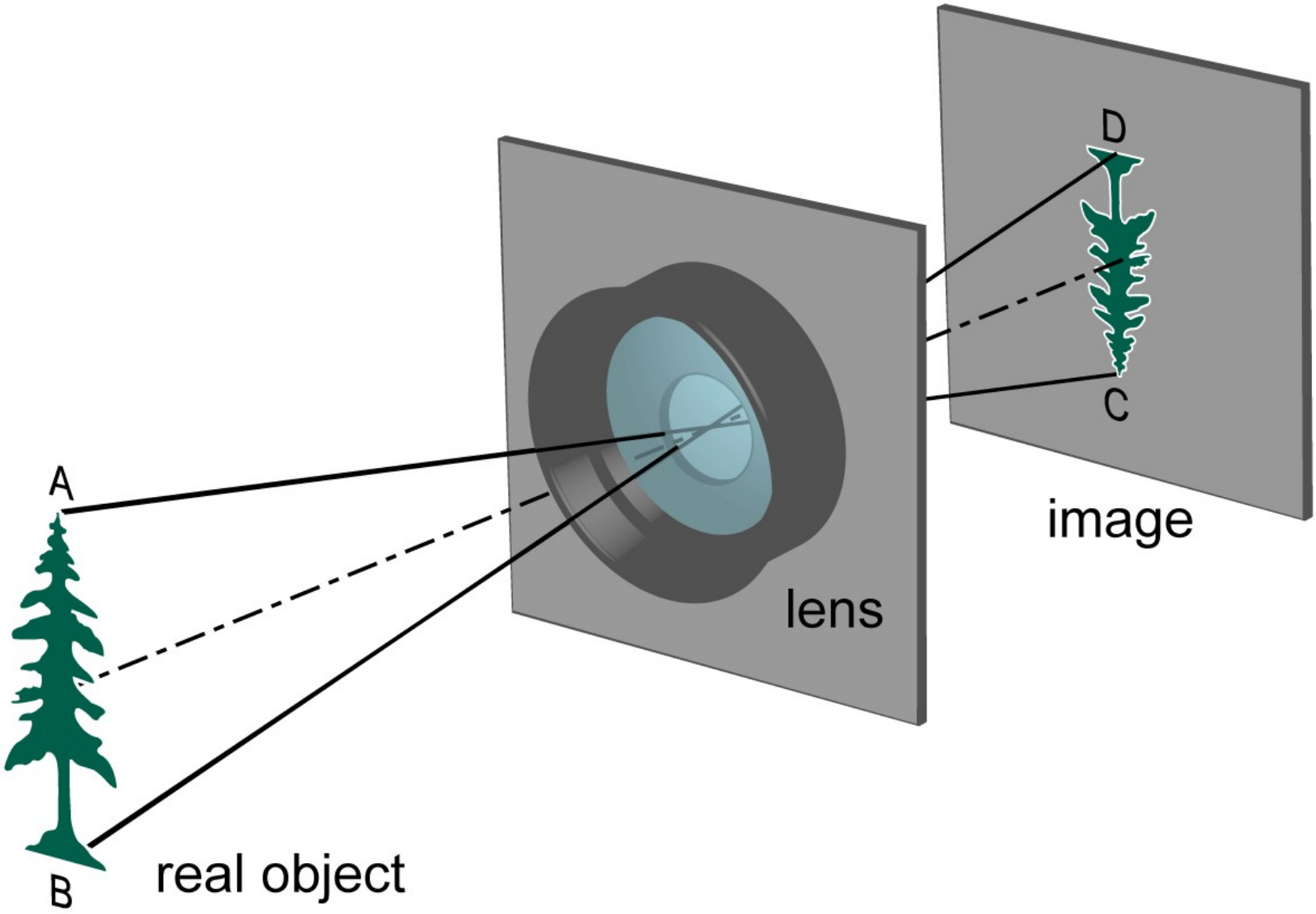
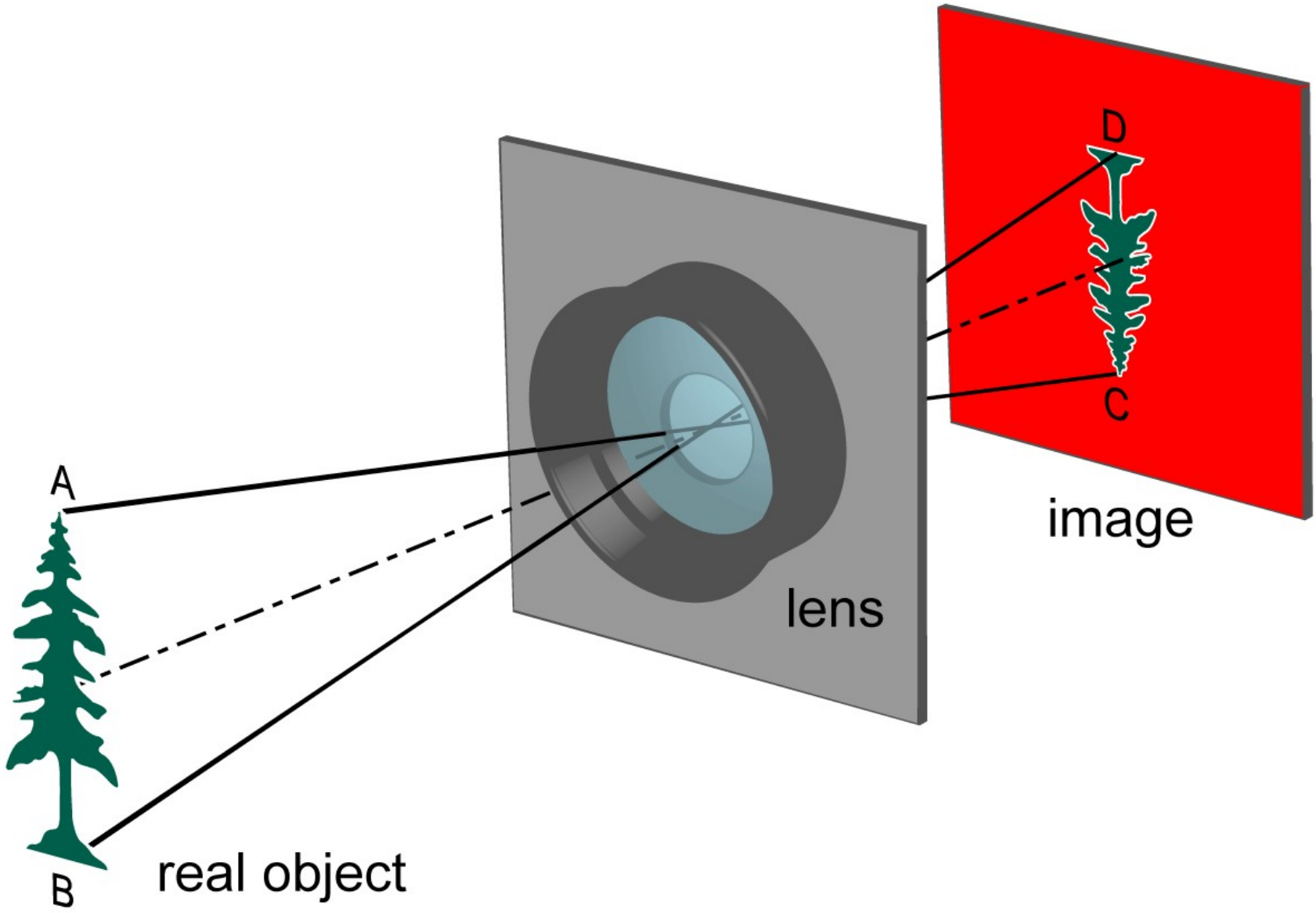


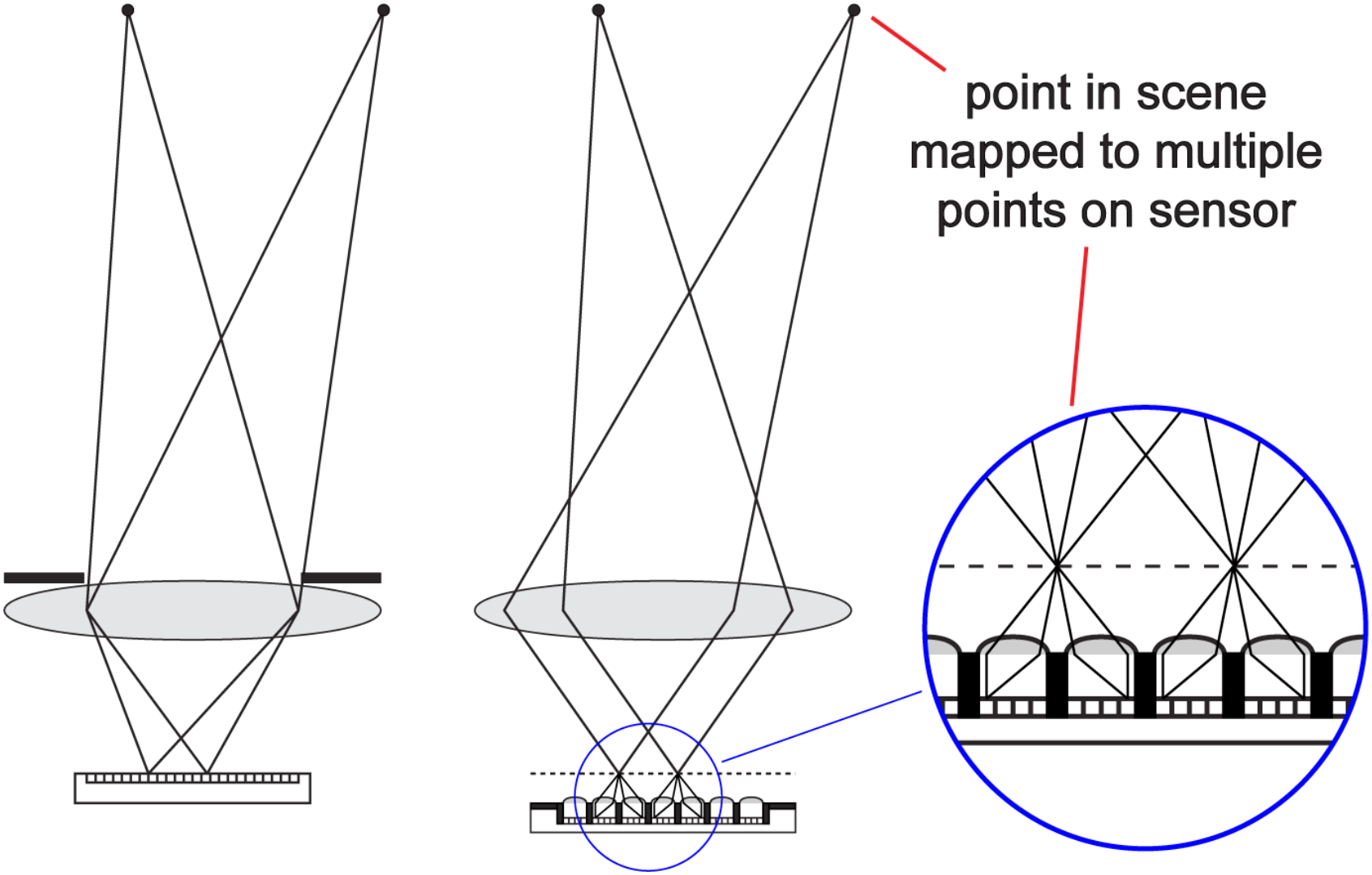
Image Formation in a Camera



Outline

- Multi-Aperture application
- FT-CCD array
  - Surface-channel
  - Buried-channel
  - Pinned phase buried-channel
- Results
- Summary

Conventional vs. Multi-Aperture



Conventional imaging

Multi-Aperture imaging

** K. Fife, A. El Gamal and H.-S. P. Wong, CICC 2006, p281-284*

Multi-Aperture Imaging

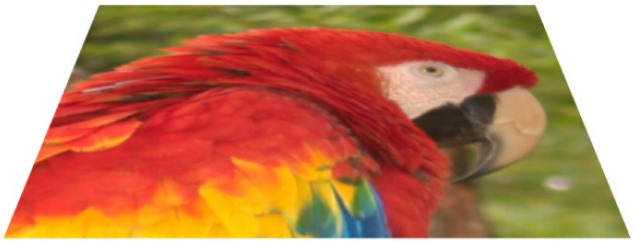


Image in focal Plane

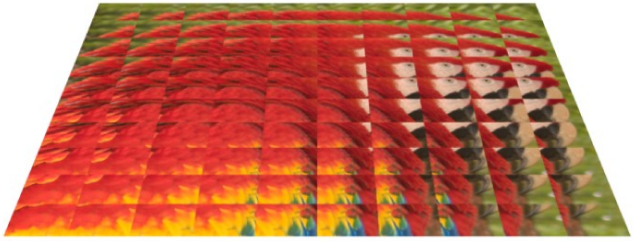
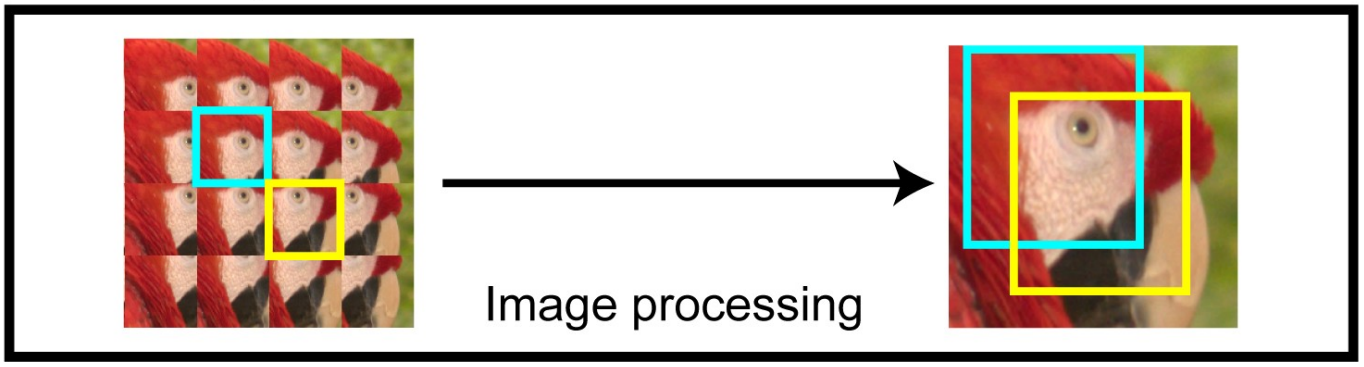


Image captured at MA-imager

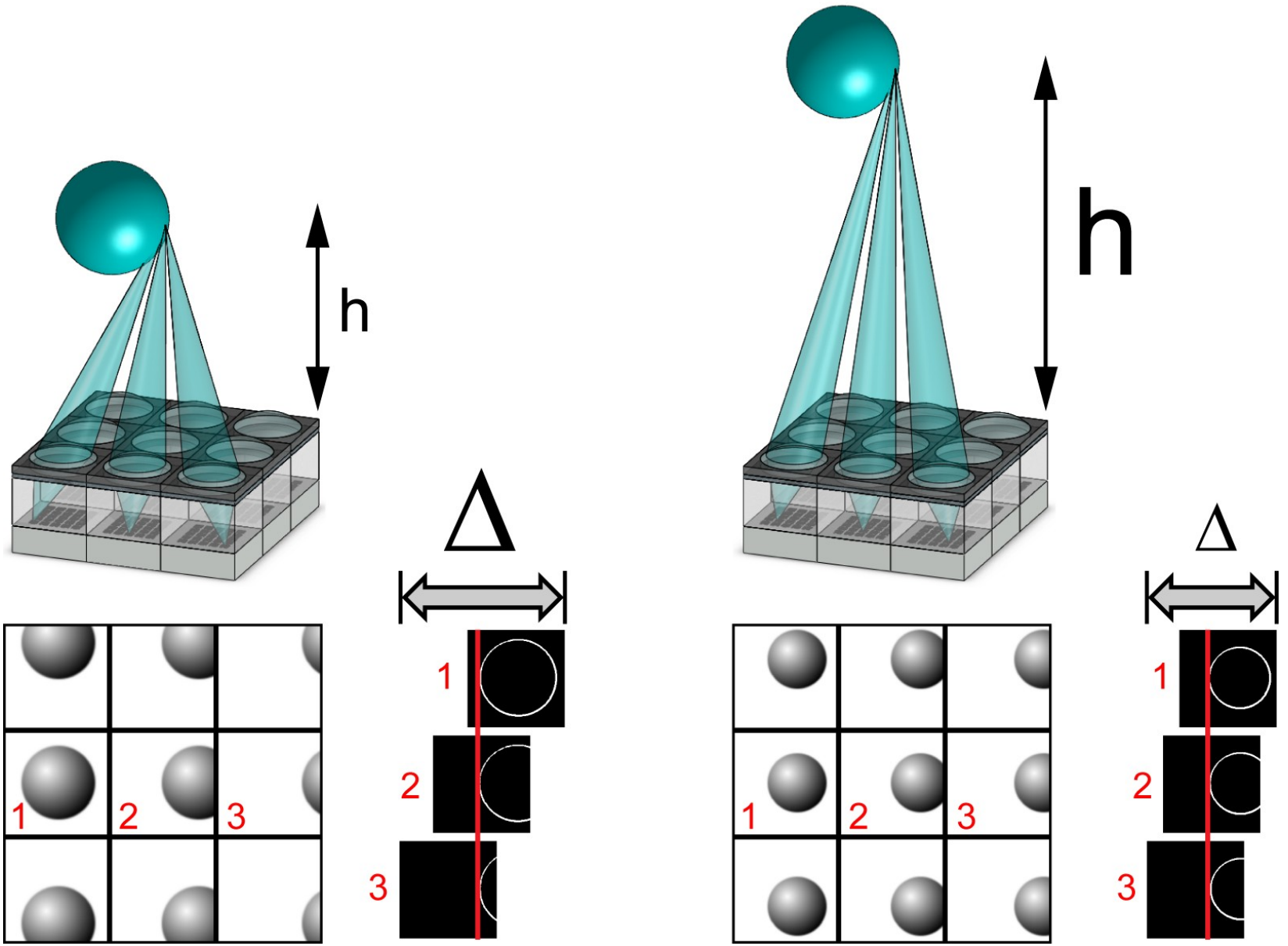
Final reconstructed image



Benefits of Multi-Aperture Imaging

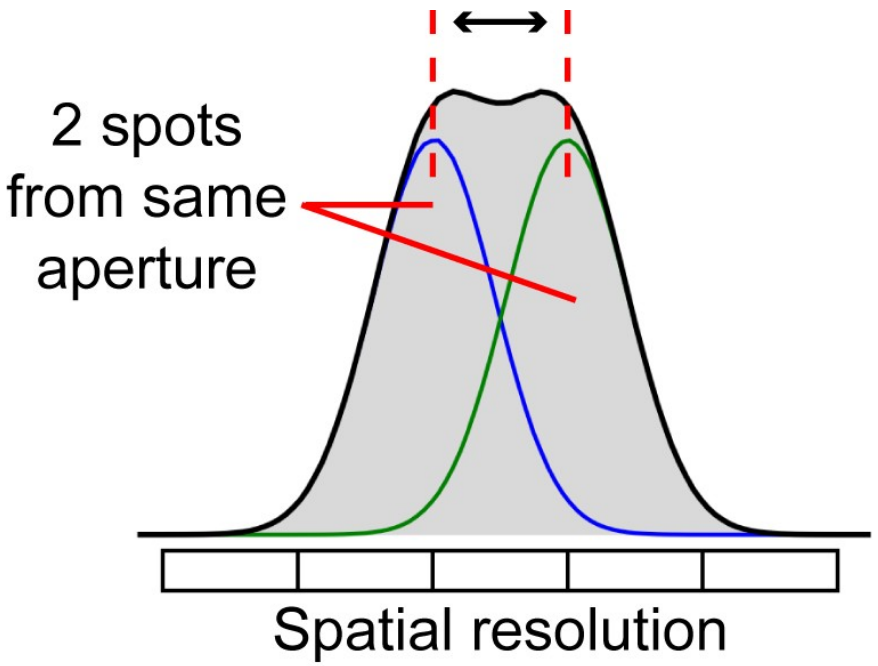
- Capture depth information
- Close proximity imaging
- Achieve better color separation
- Reduce requirements of objective lens
- Increase tolerance to defective pixels
- Increase scalability

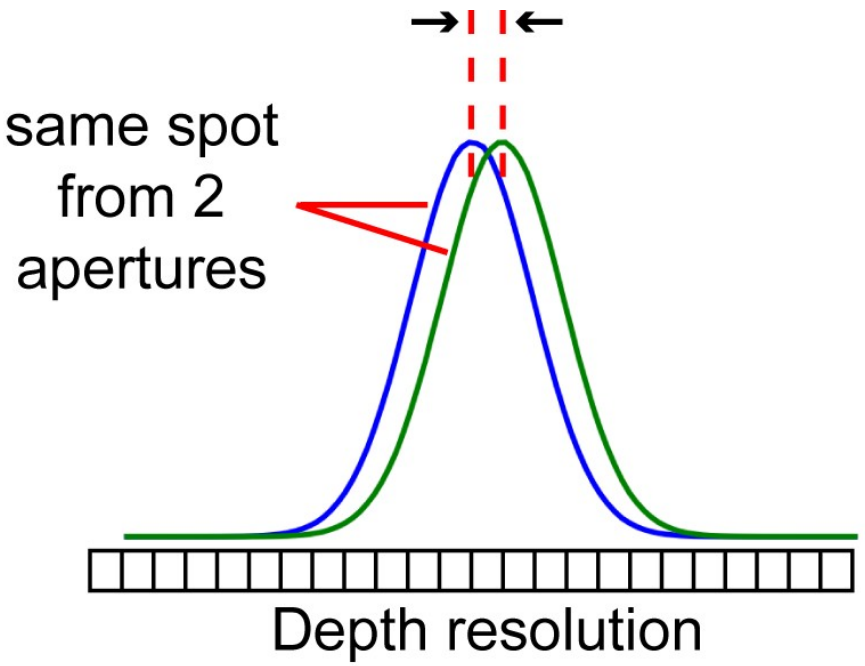
Depth from Multi-Aperture



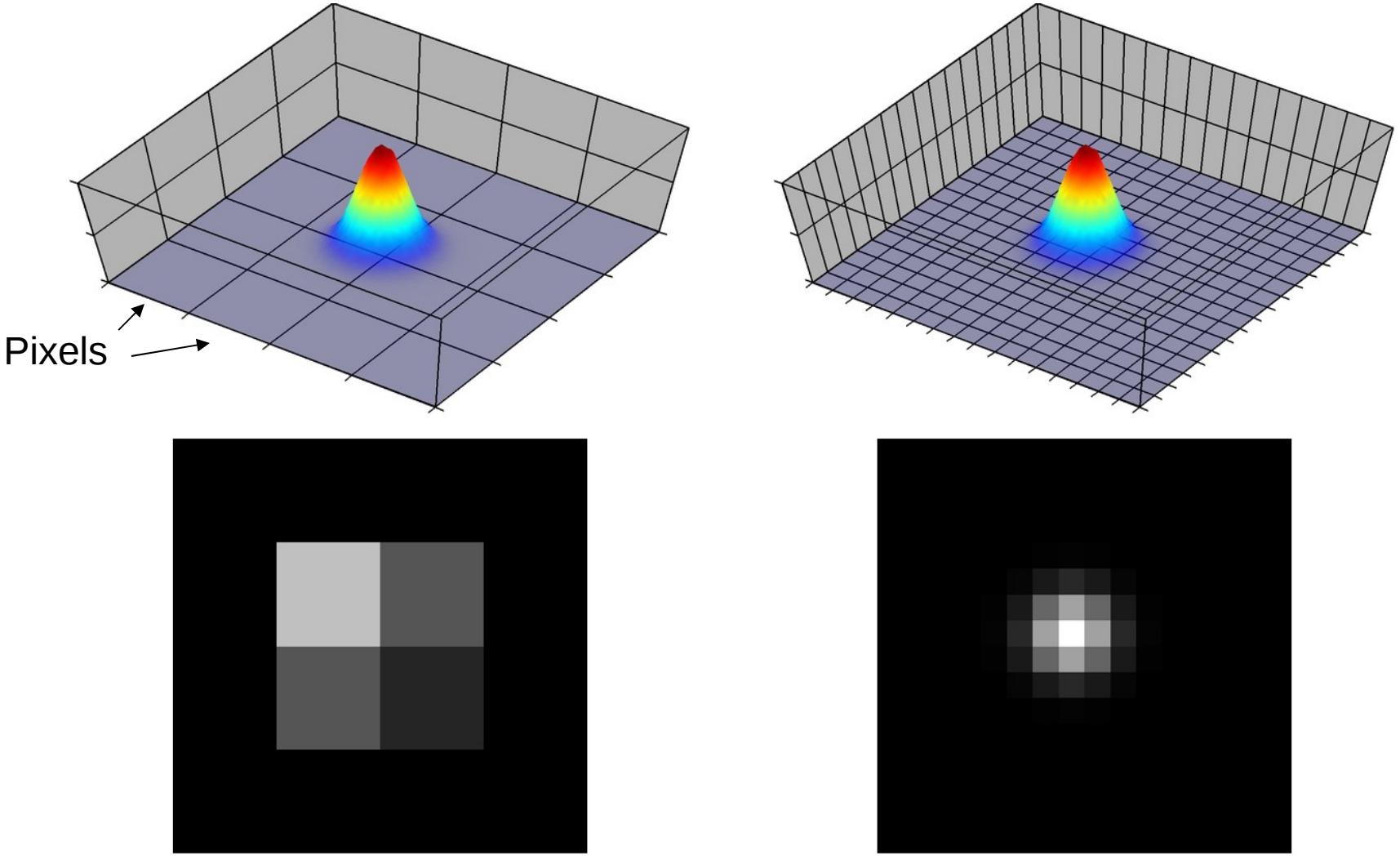
Why Use Small Pixels?

- Depth resolution improves with pixels smaller than the spot size
- Spatial resolution is limited by the spot size
- Depth resolution is limited by accuracy in localization of the spot





Feature Localization vs. Pixel Size



Poor location accuracy

High location accuracy

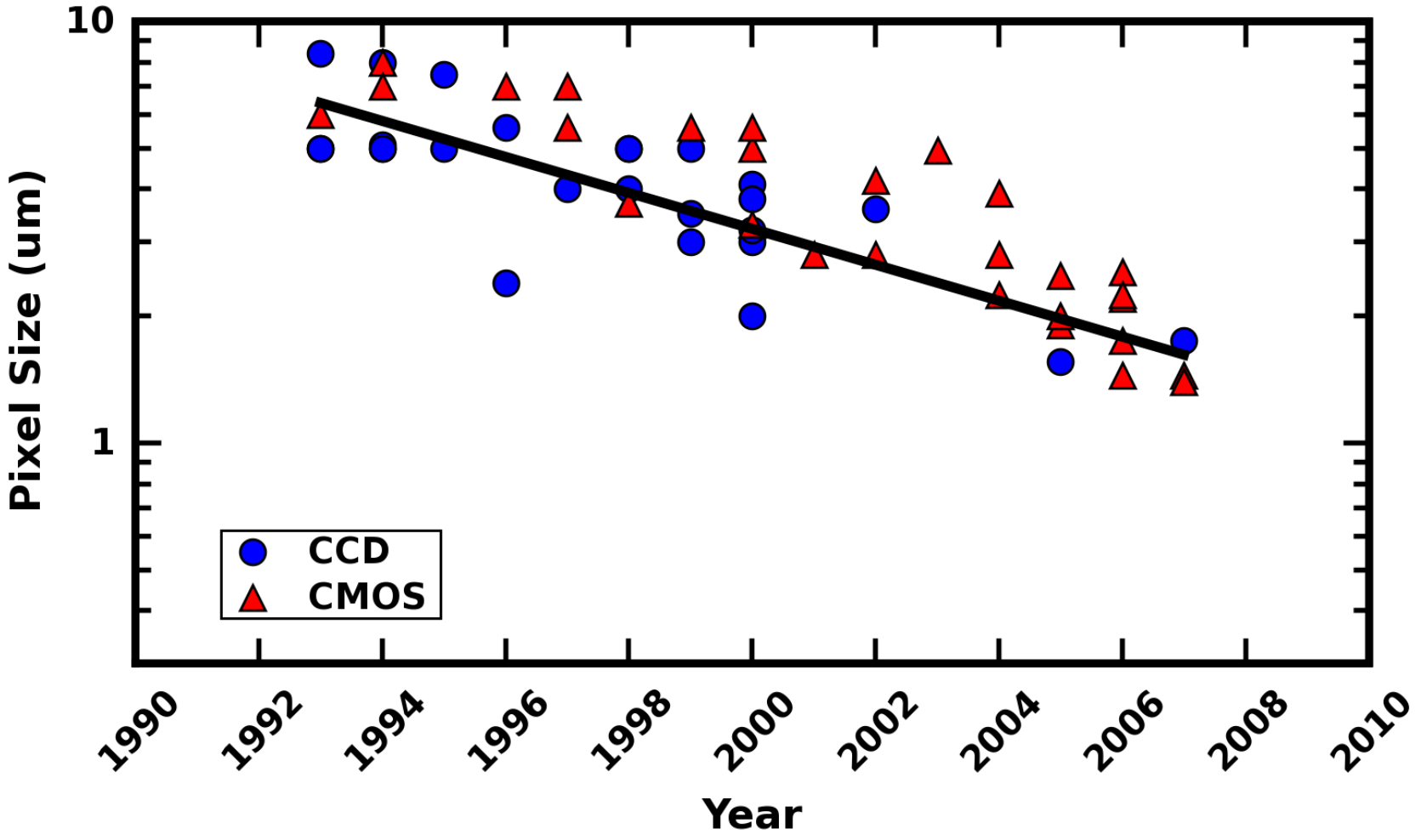
Implementation

- Submicron pixels are difficult to build
- Small, disjoint arrays of pixels (clusters) are needed for MA architecture
  - Easier to implement pixels as clusters
  - Several performance advantages
- We selected a hybrid CCD/CMOS image sensor architecture

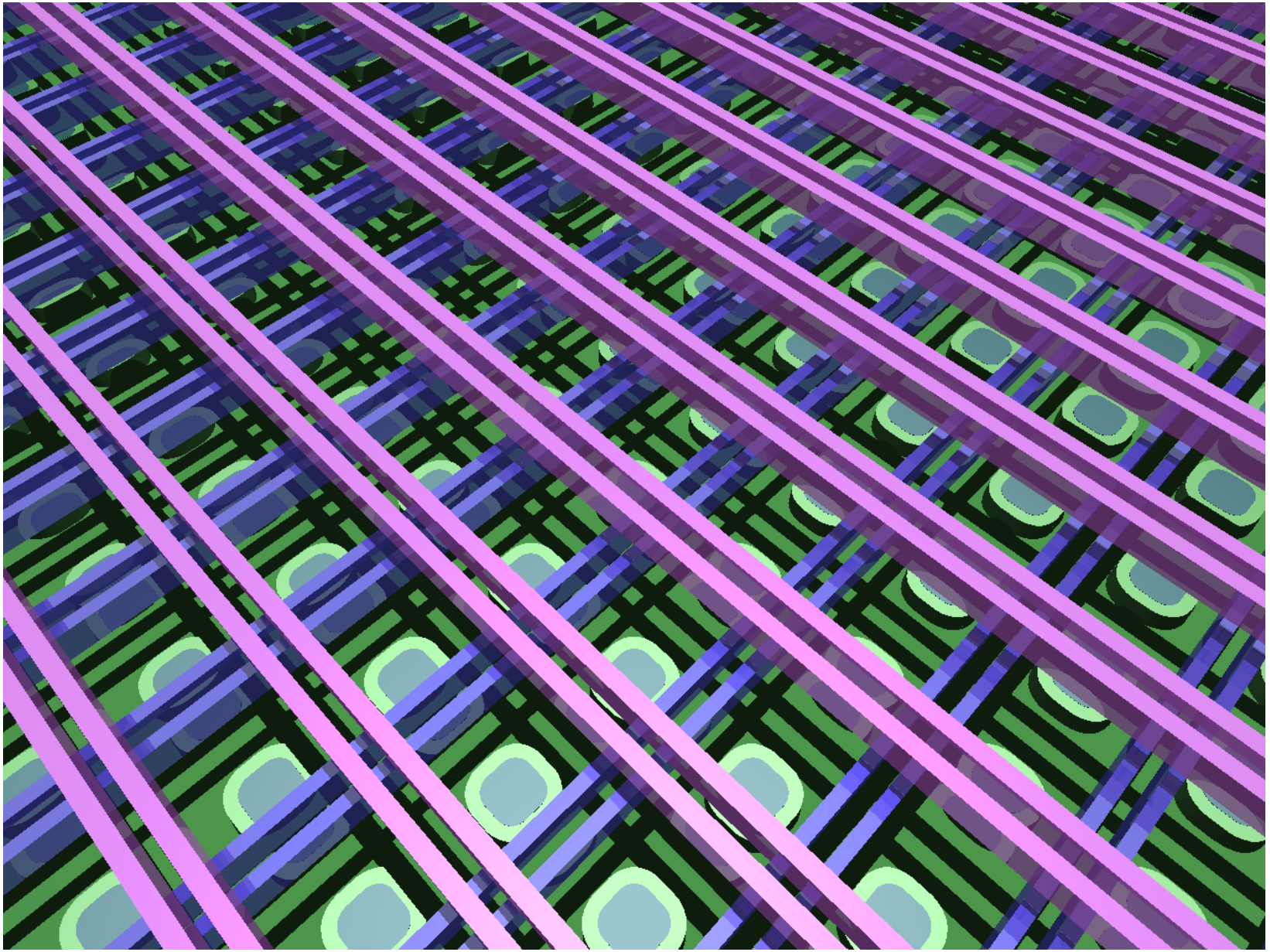
Recent Pixel Scaling

- Increase spatial resolution
- Decrease format size

Pixel Sizes reported at IEDM, ISSCC, IISW

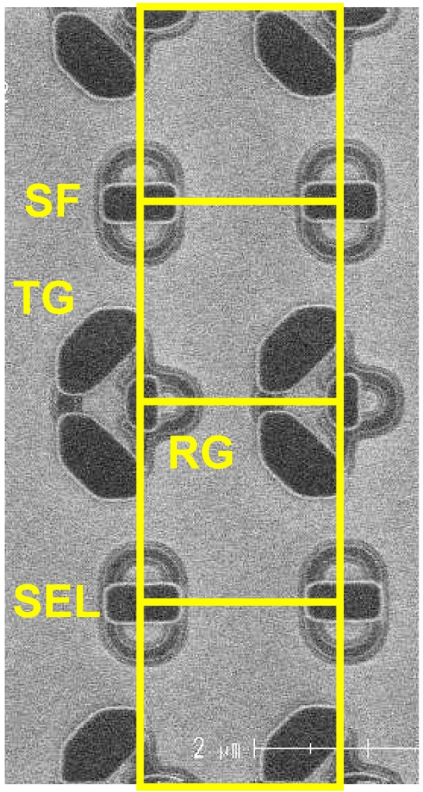


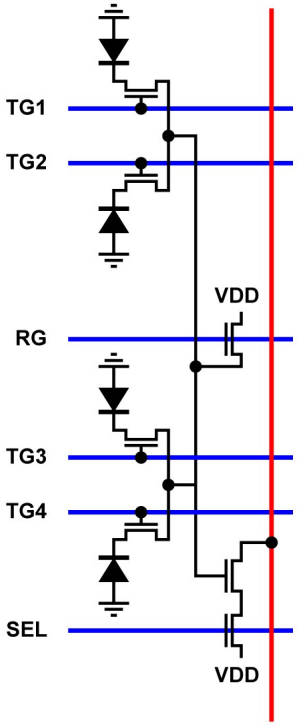
Ex:1.75um Pixel in 0.11um CMOS



Recent Pixel Scaling Technology

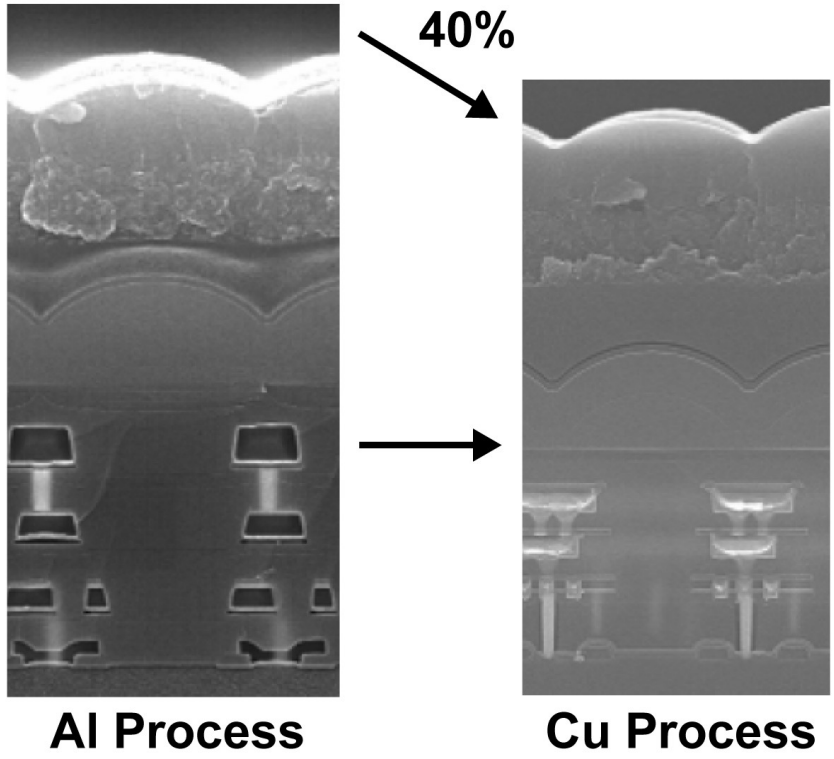
4T sharing





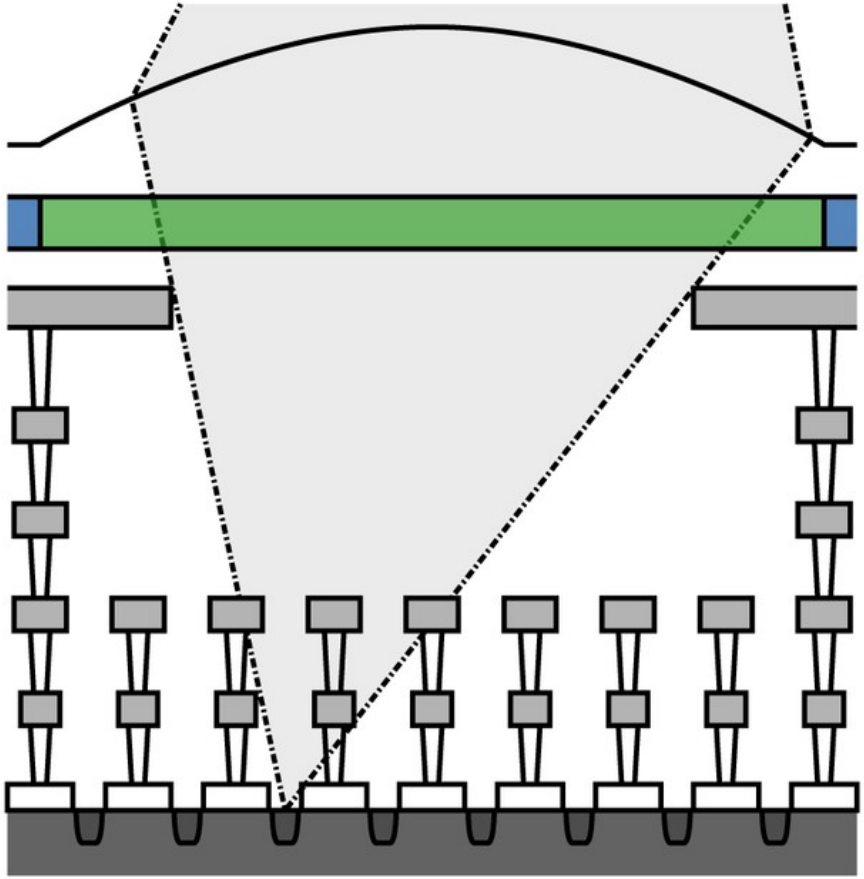
** J. Kim, J. Shin, C.R. Moon, et. al., IEDM 2006, p123-126*

Stack height reduction

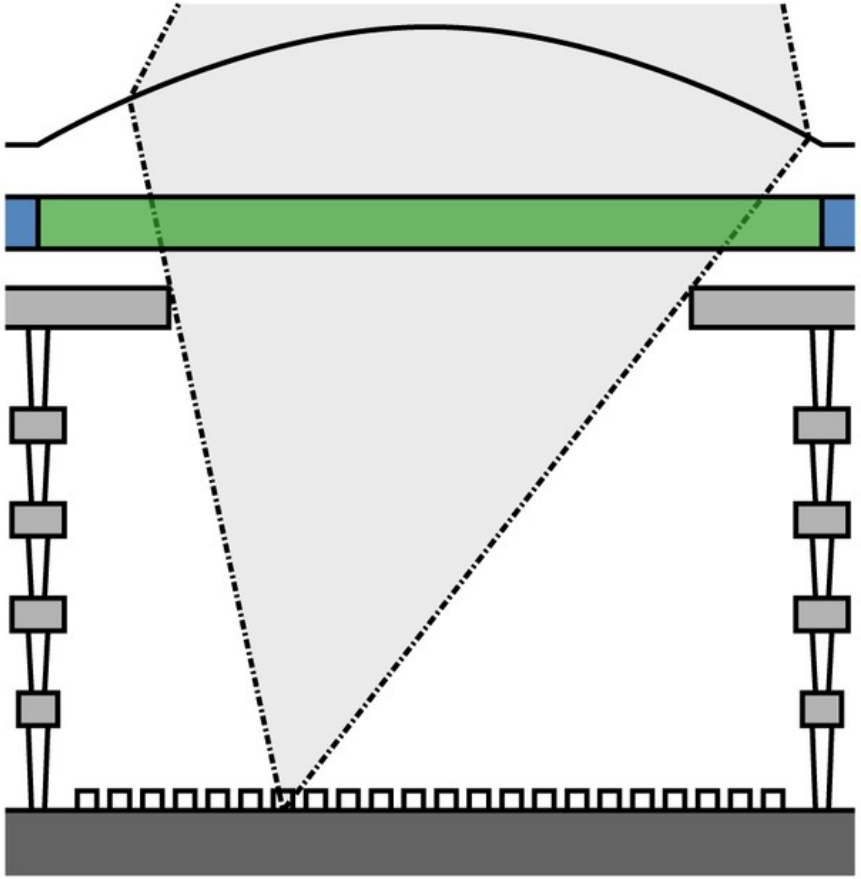


** H. Sumi, IEDM 2006, p119-122*

A Reason for using CCD Pixels

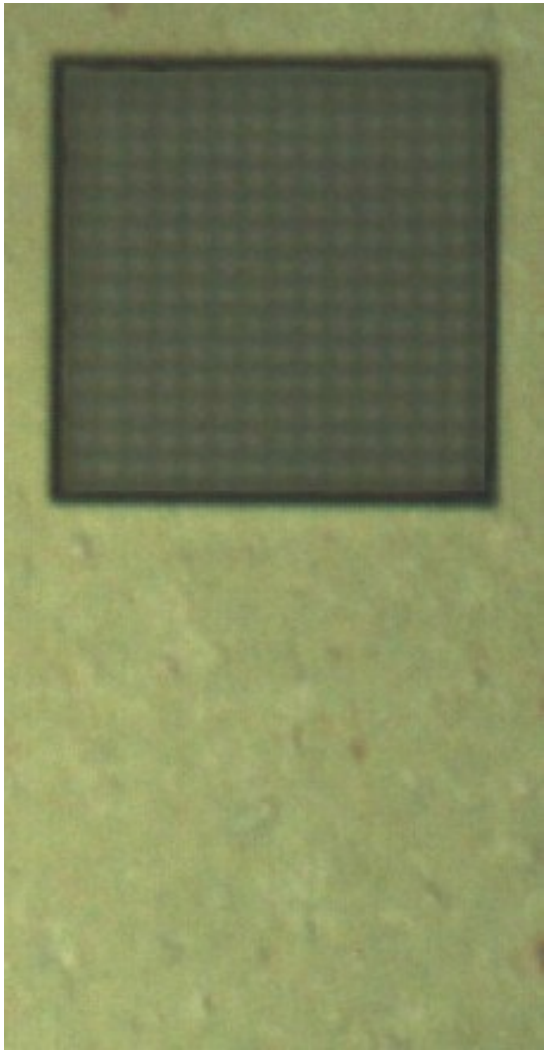


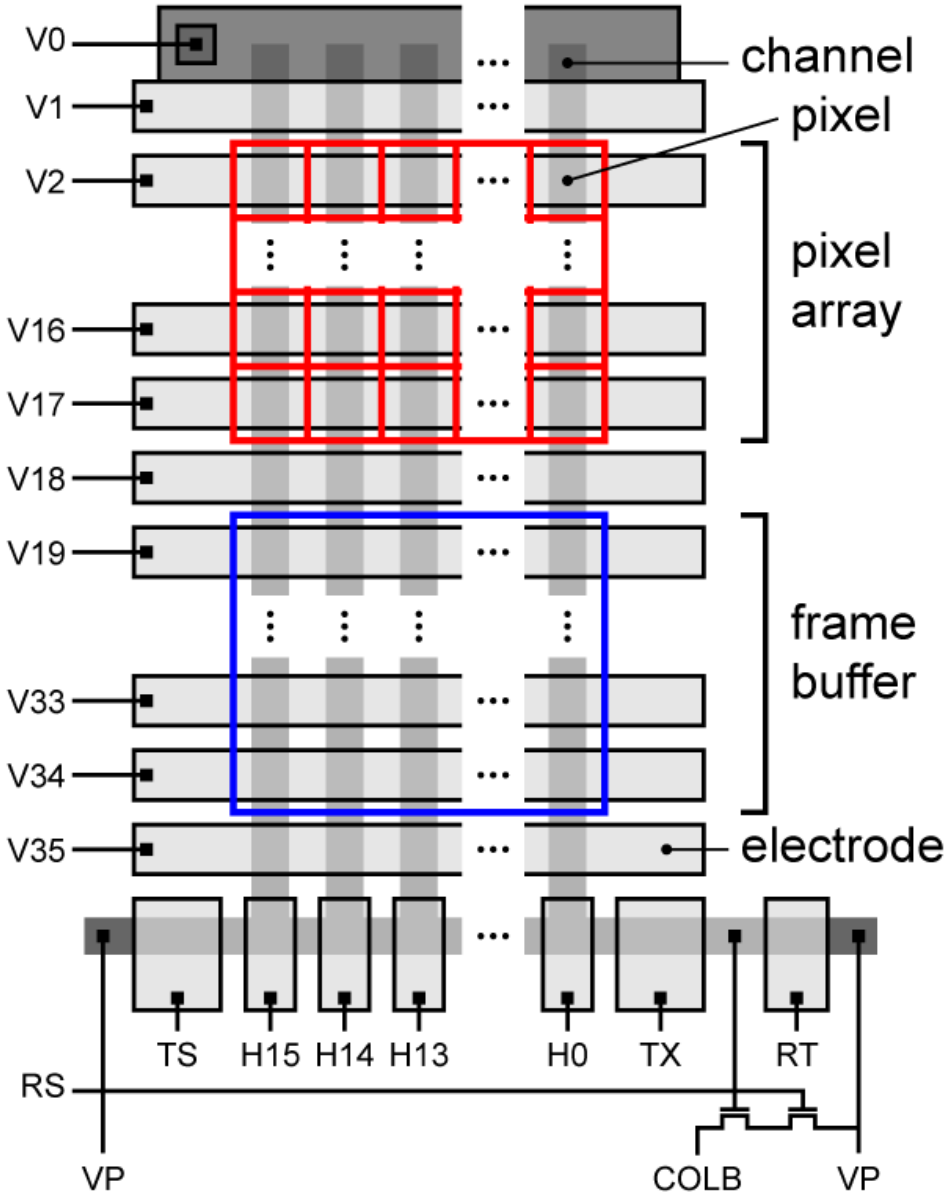
Using CMOS active pixels



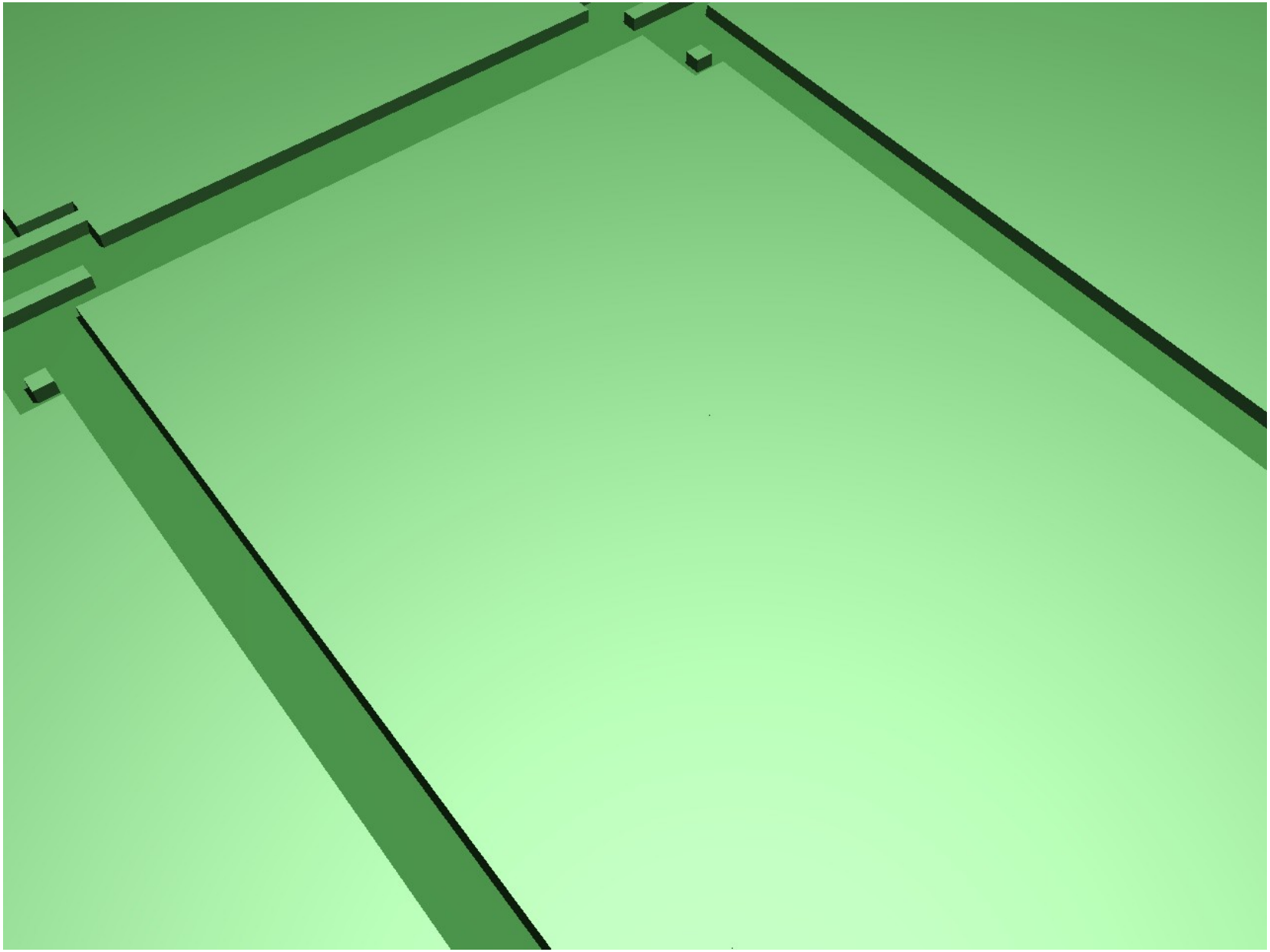
Using FT-CCD pixels

16 x 16 FT-CCD schematic

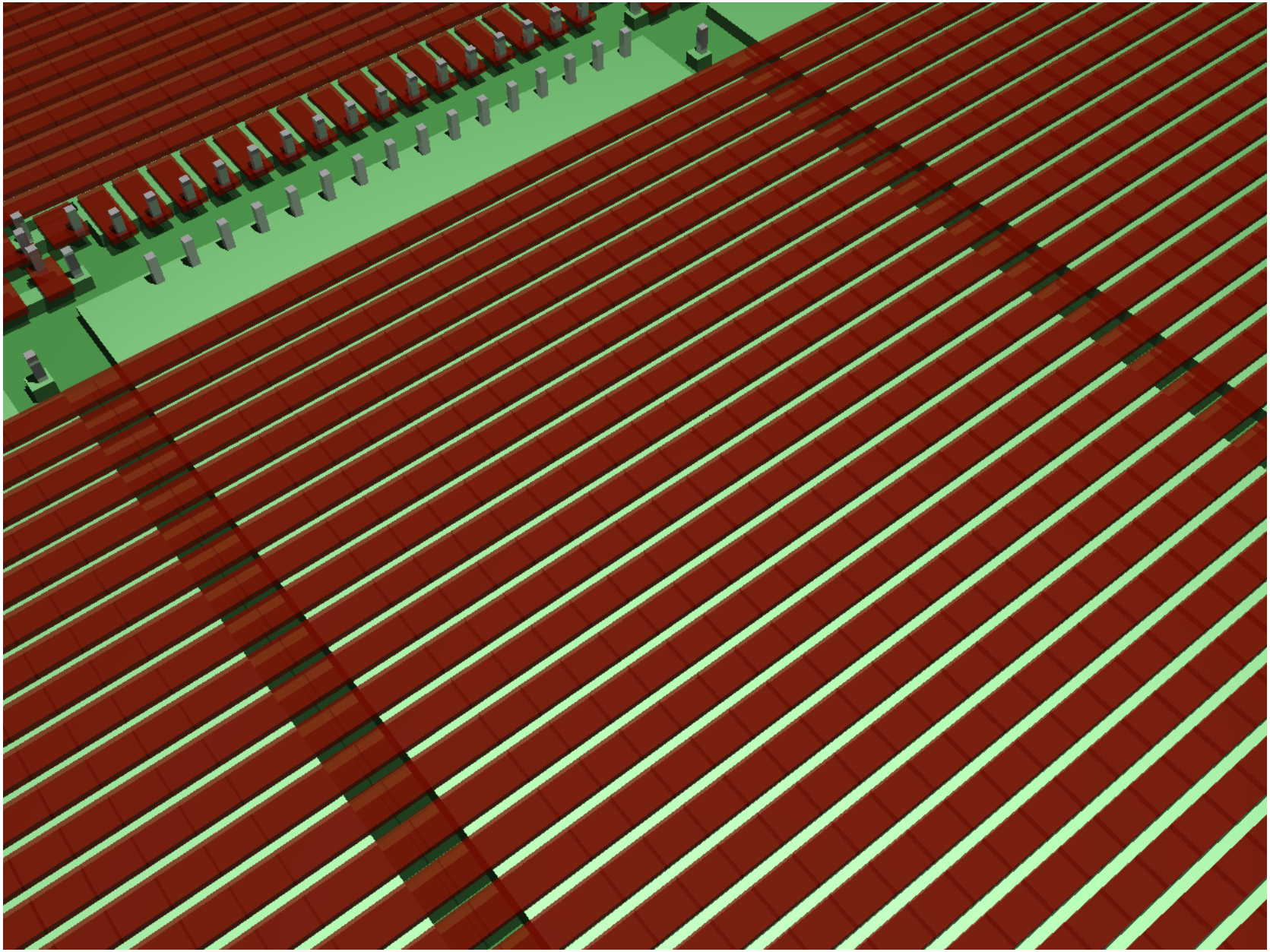




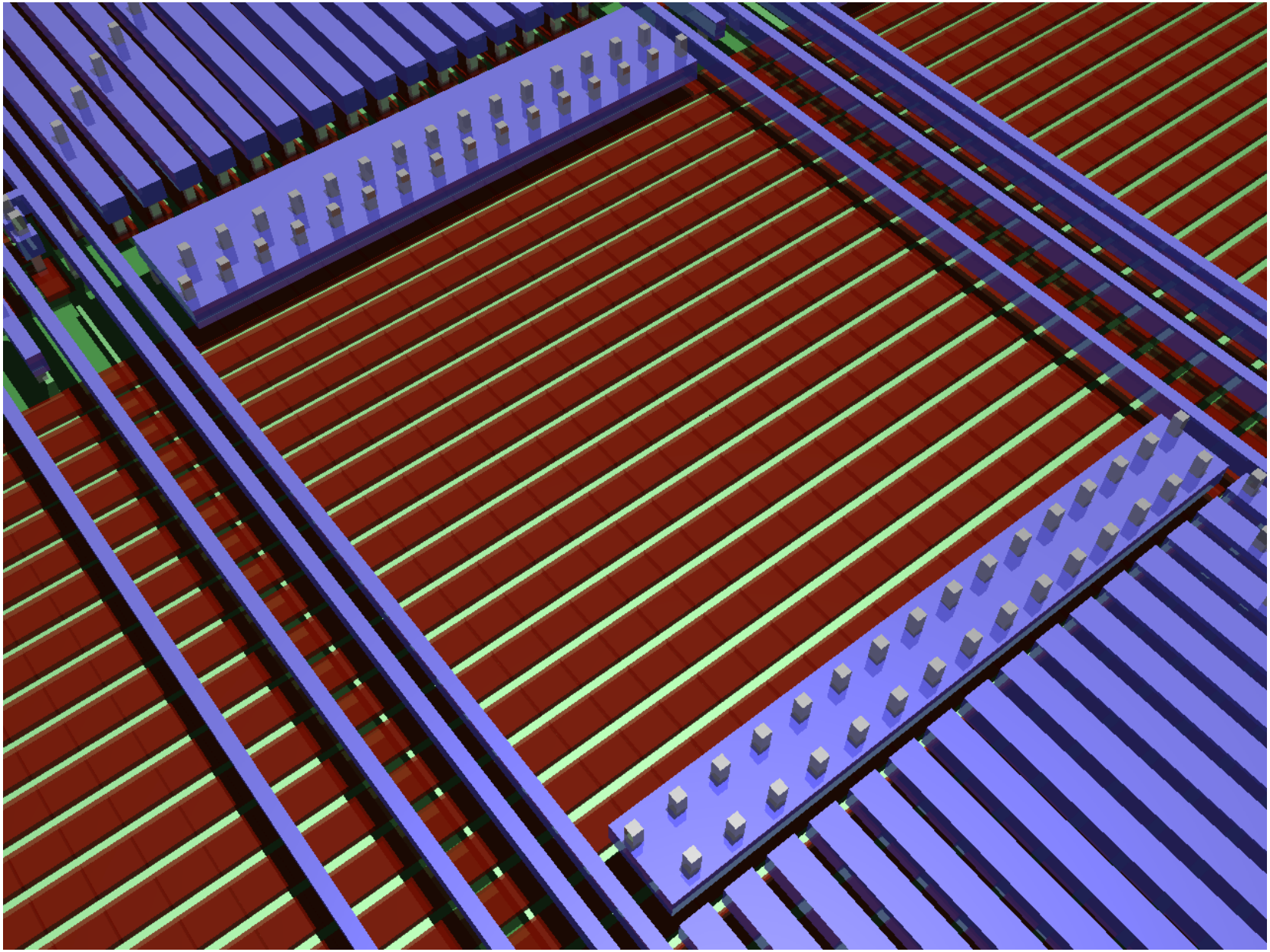
Thin Oxide



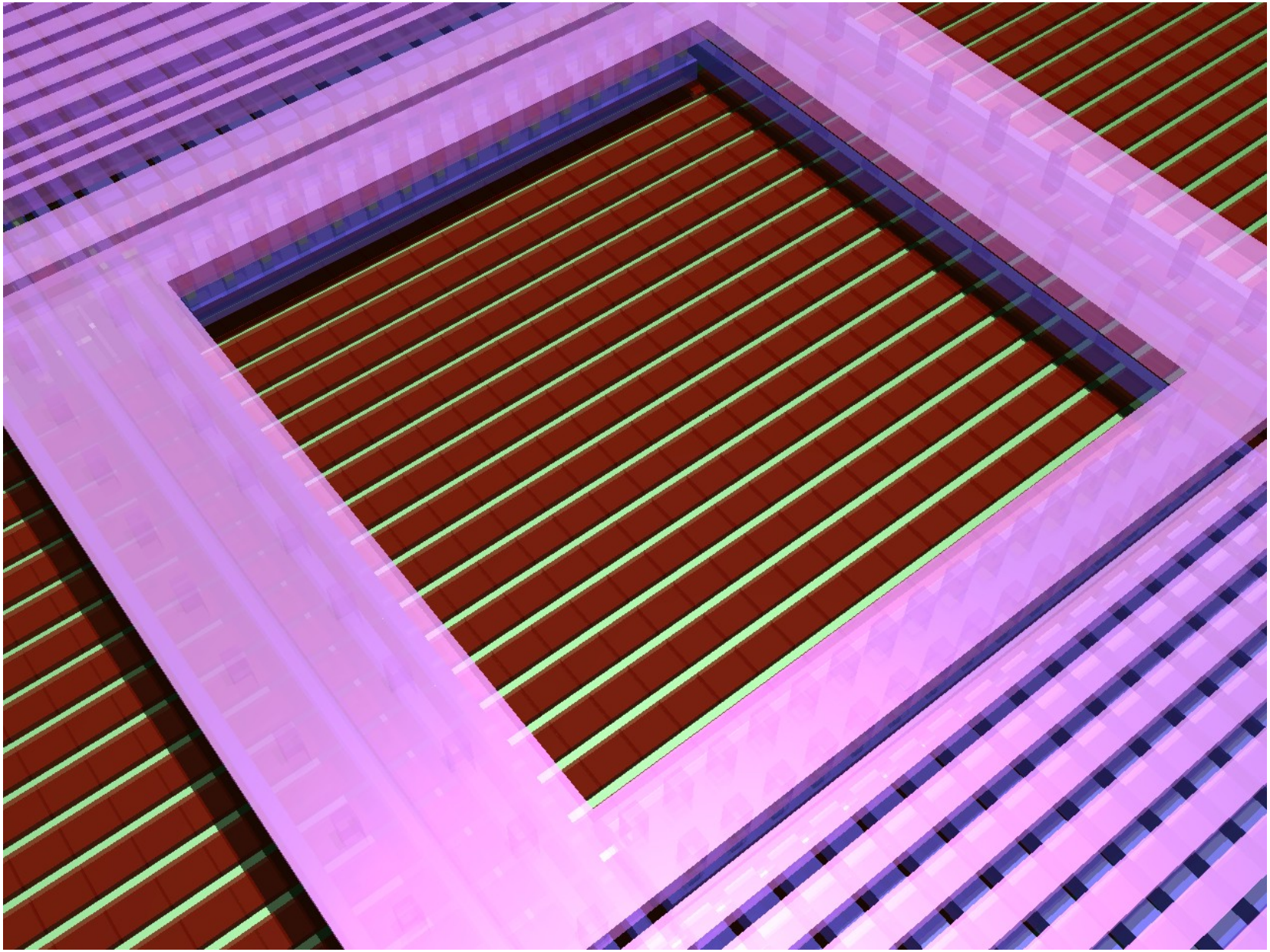
Poly and Contact



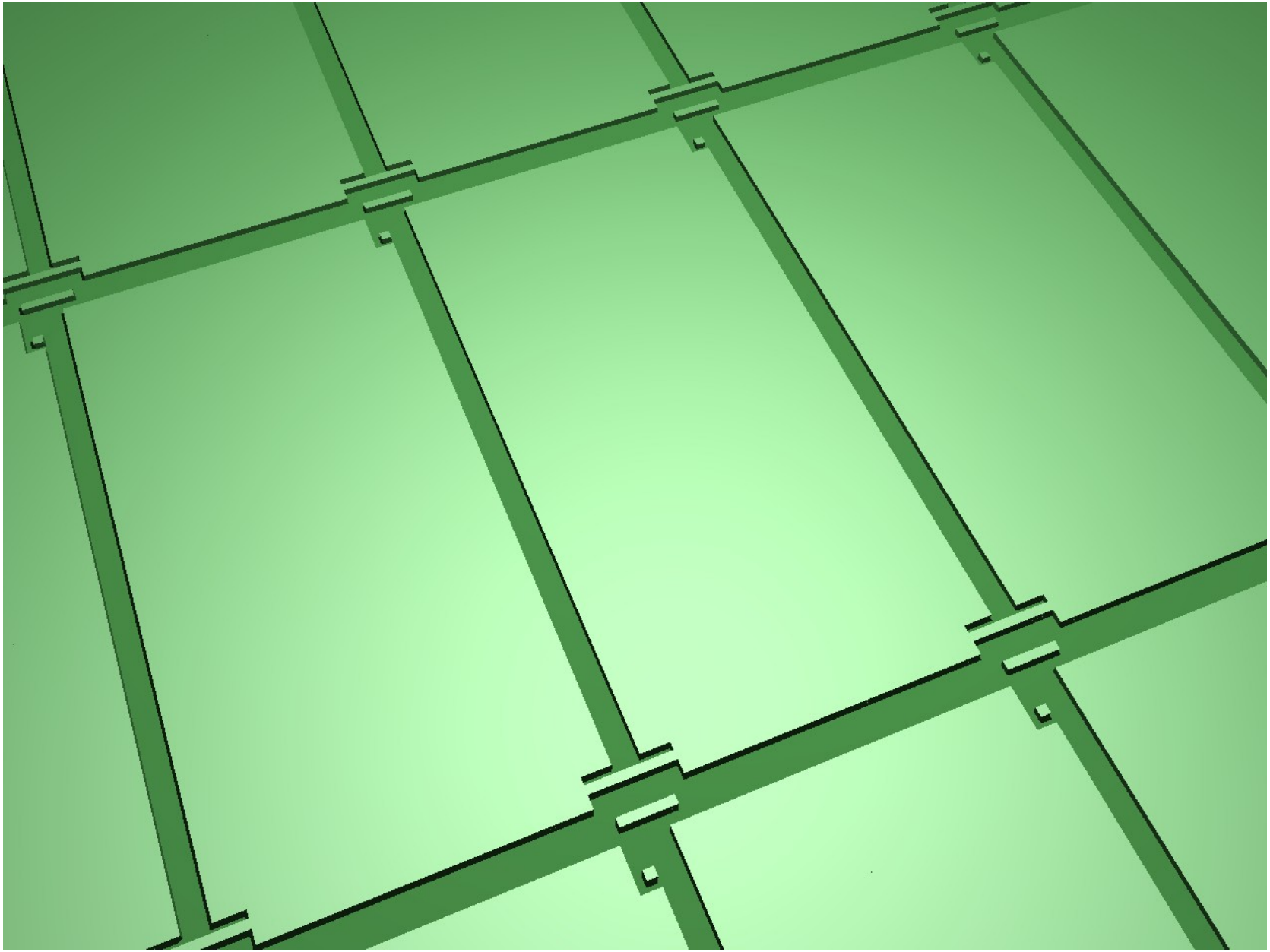
Metal1 and Via12



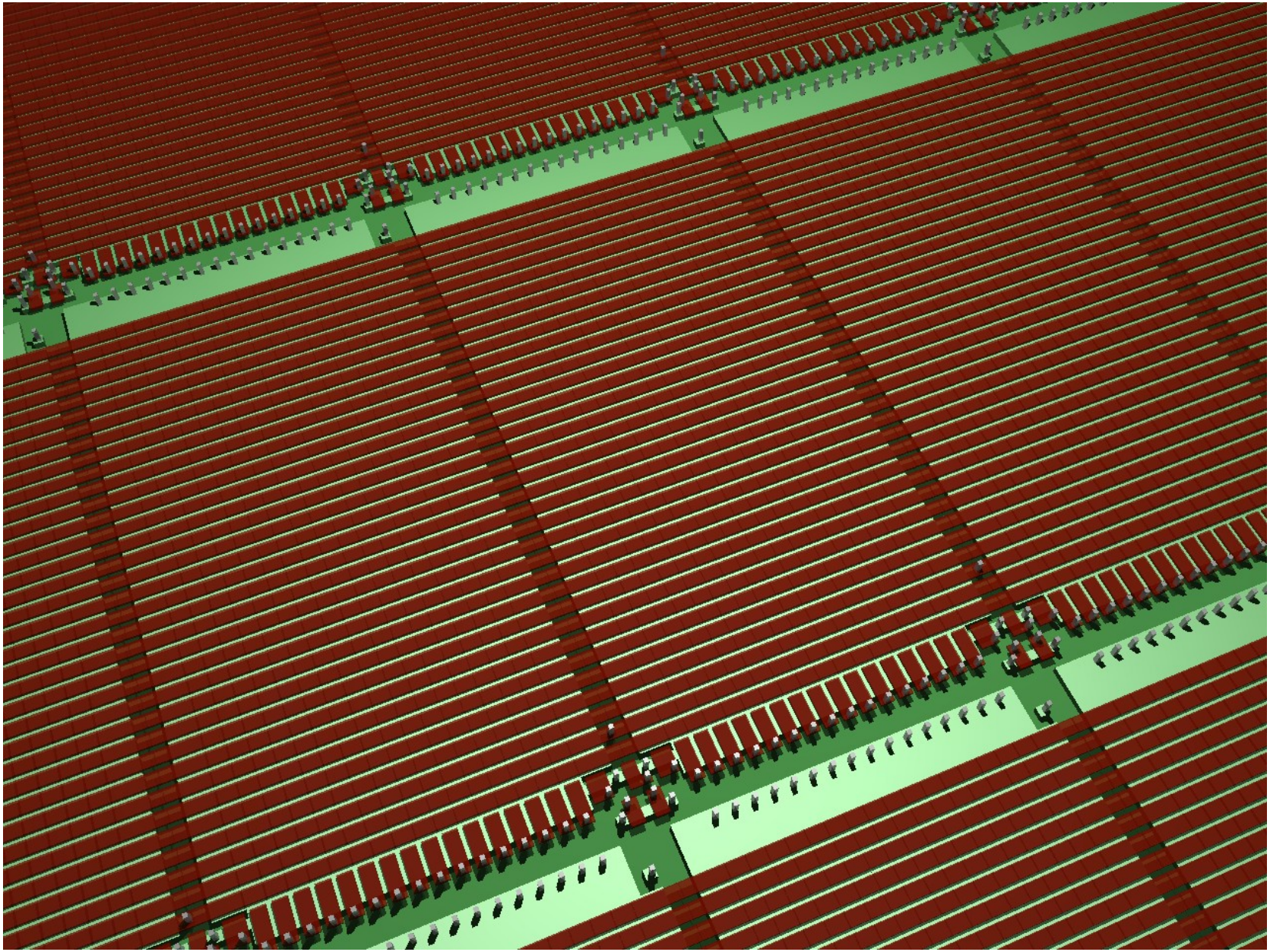
Metal2



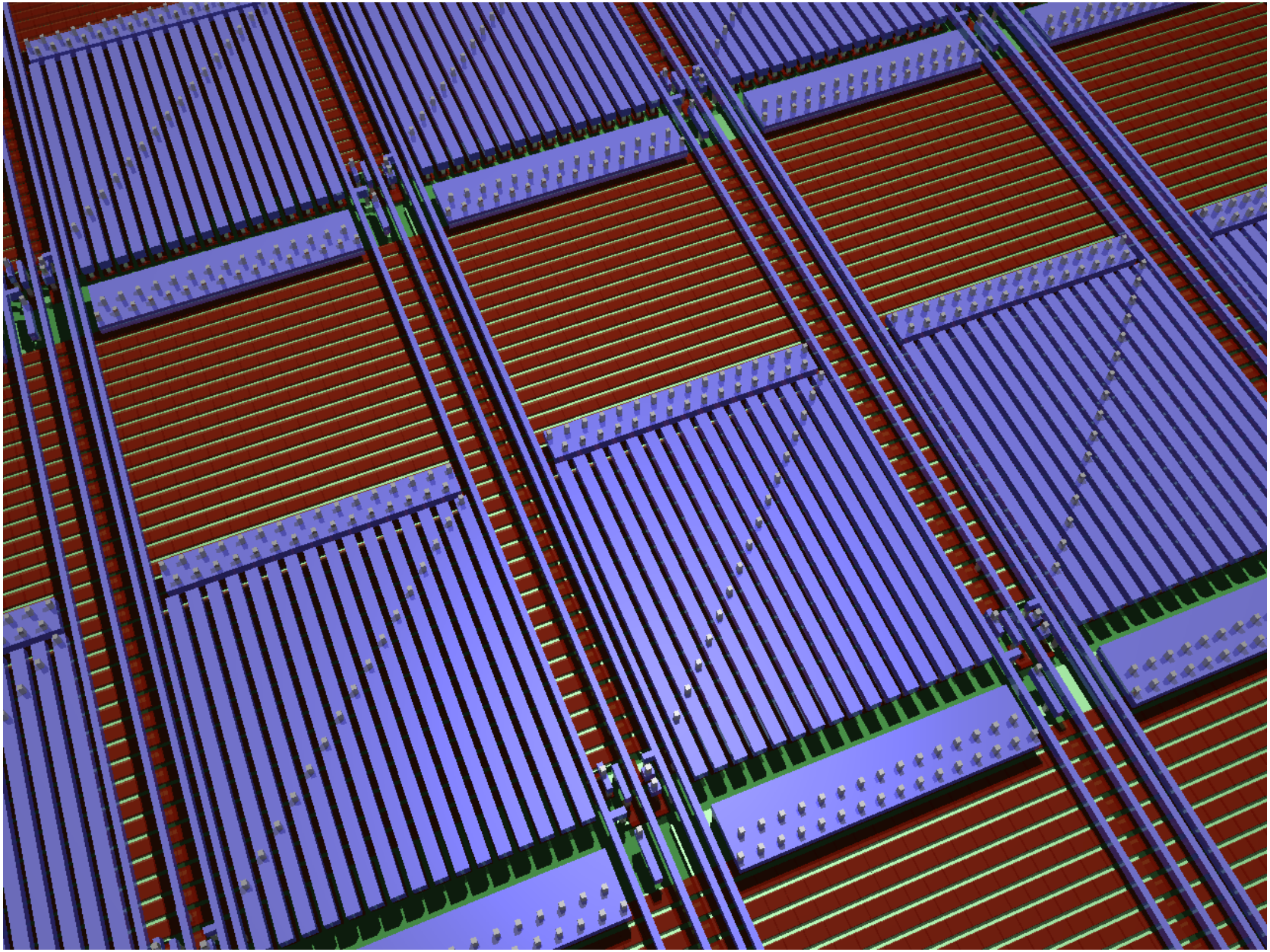
Thin Oxide



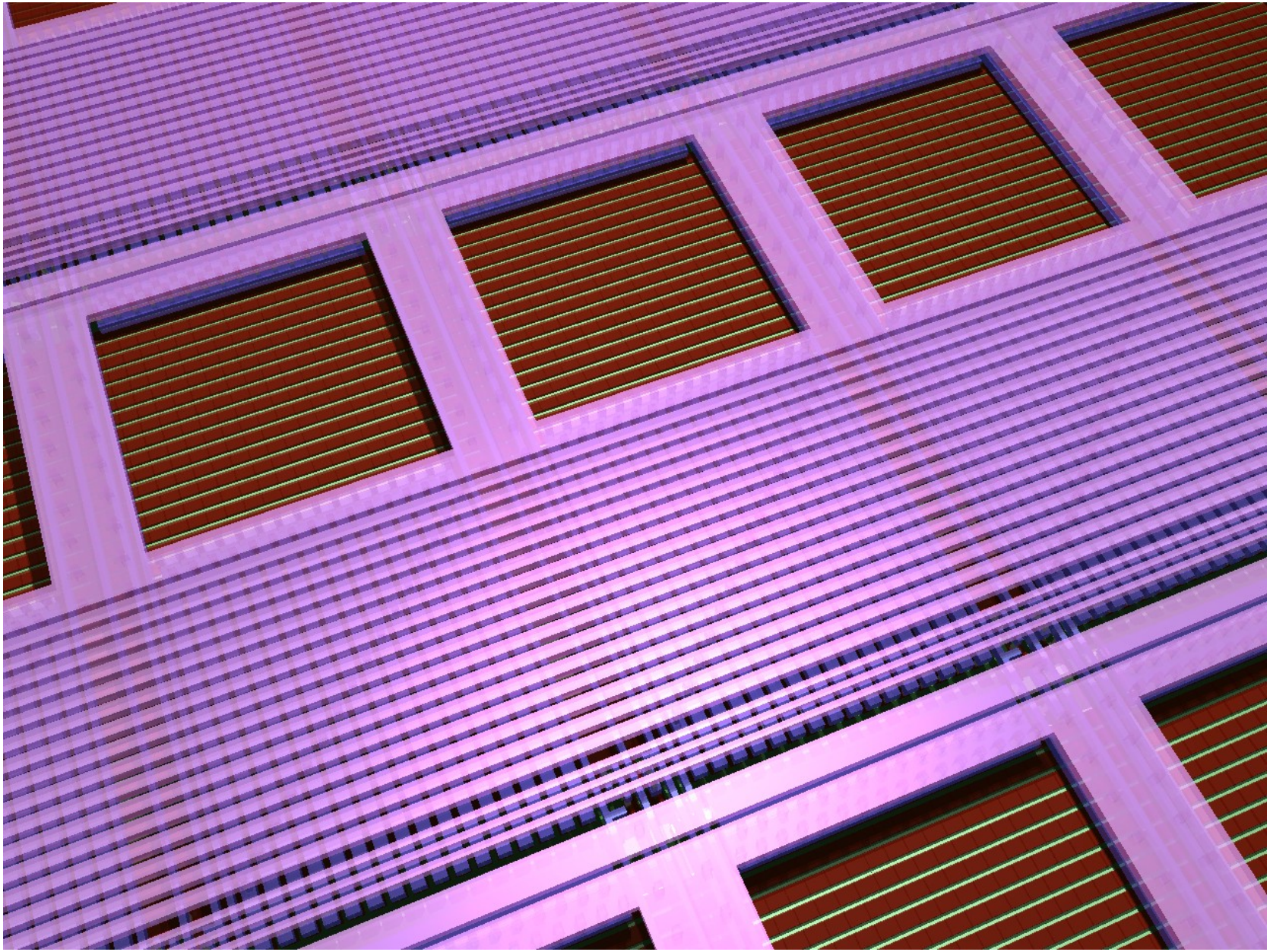
Poly and Contact



Metal and Via12



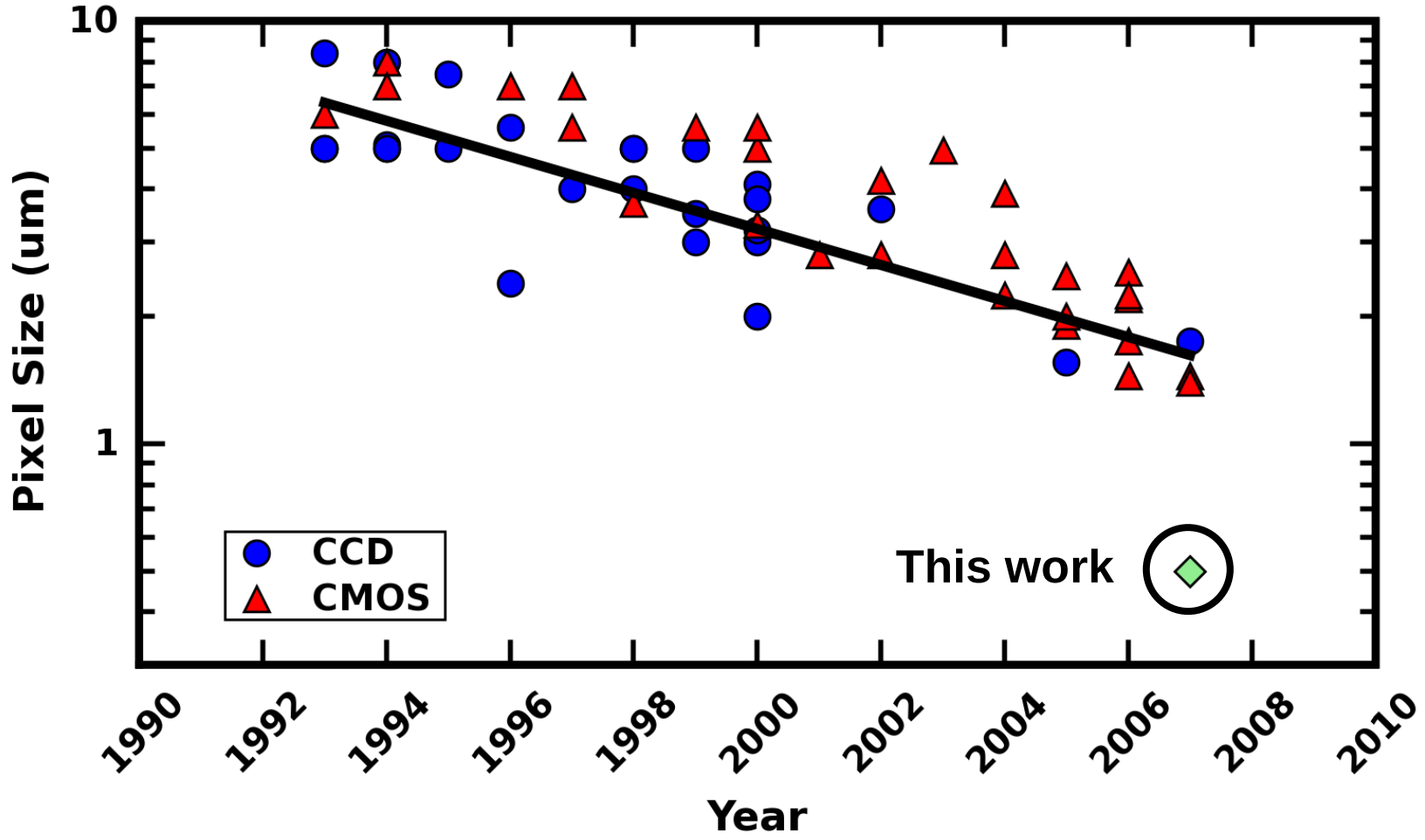
Metal2



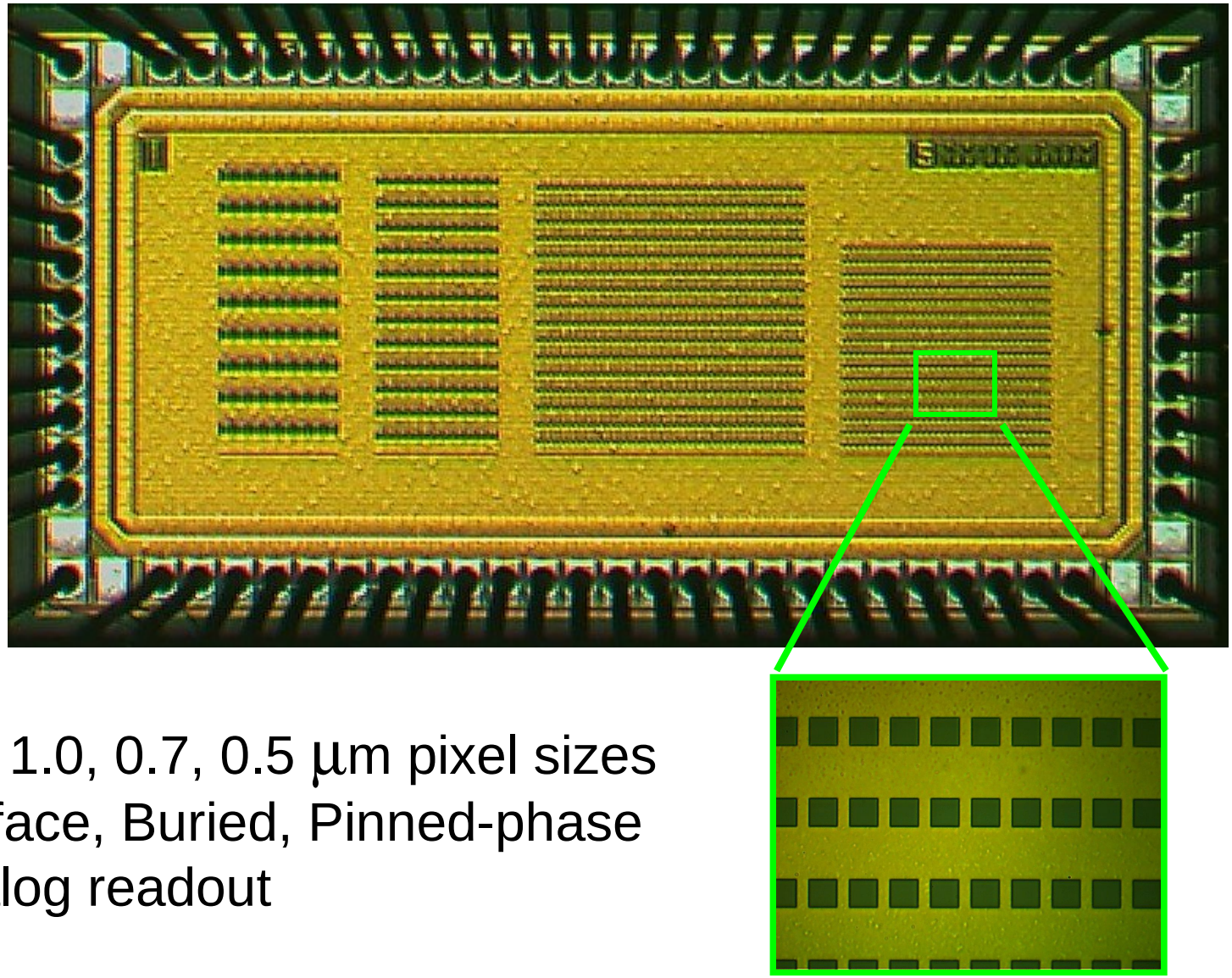
Relative Pixel Size for This Work

- Increase spatial resolution
- Decrease format size

Pixel Sizes reported at IEDM, ISSCC, IISW



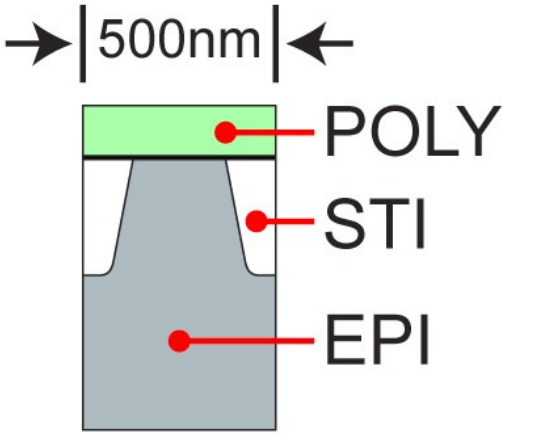
FT-CCD Test Chip



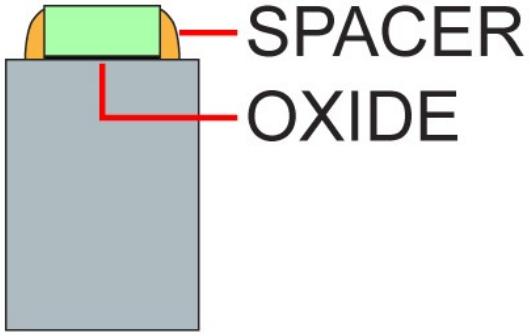
- 1.4, 1.0, 0.7, 0.5 µm pixel sizes
- Surface, Buried, Pinned-phase
- Analog readout

** K. Fife, A. El Gamal and H.-S. P. Wong, IEDM 2007, p1003-1006*

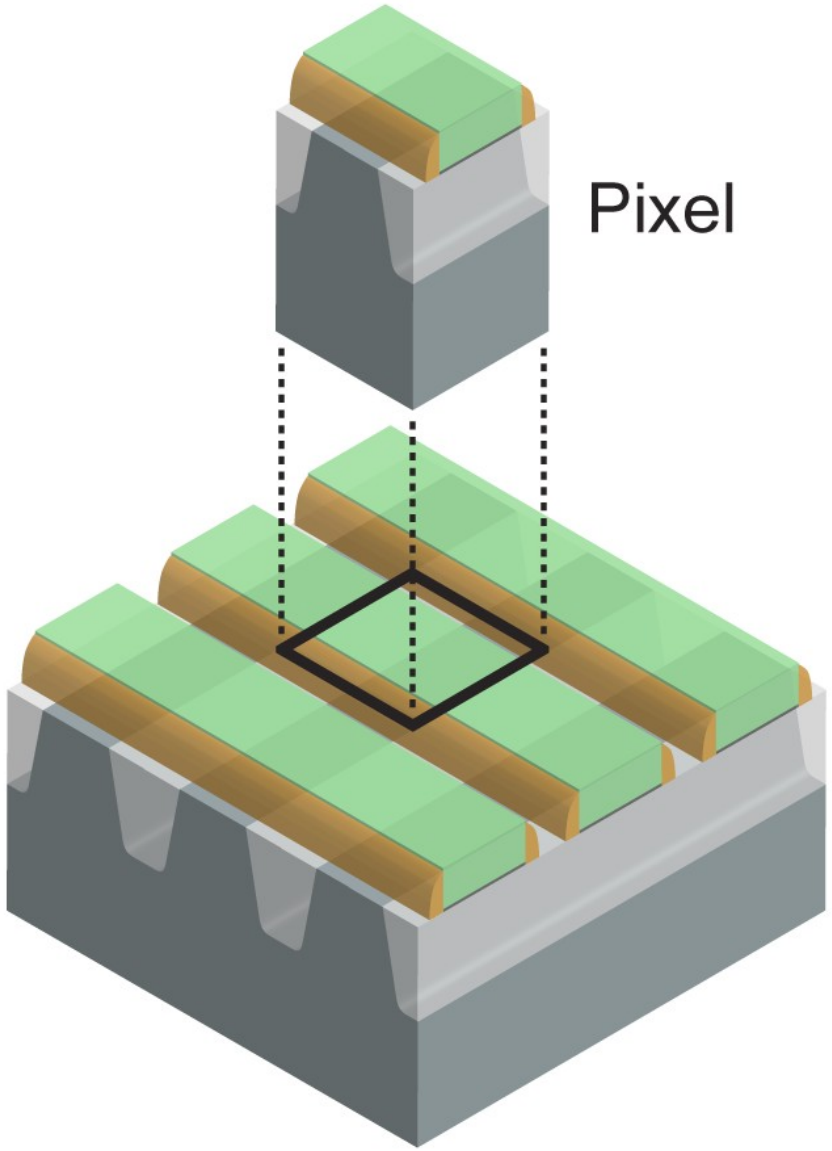
The 0.5µm Pixel



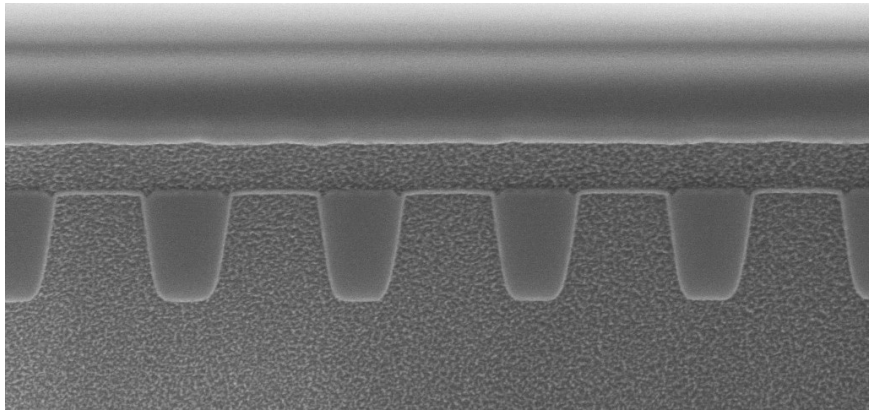
Across Channel



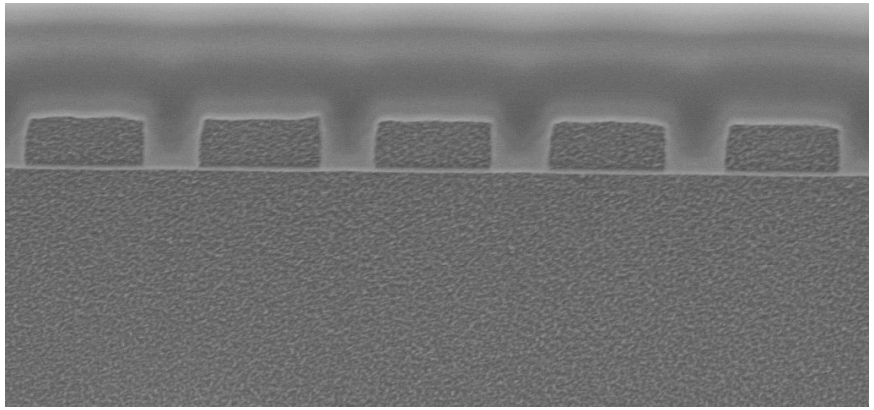
Along Channel



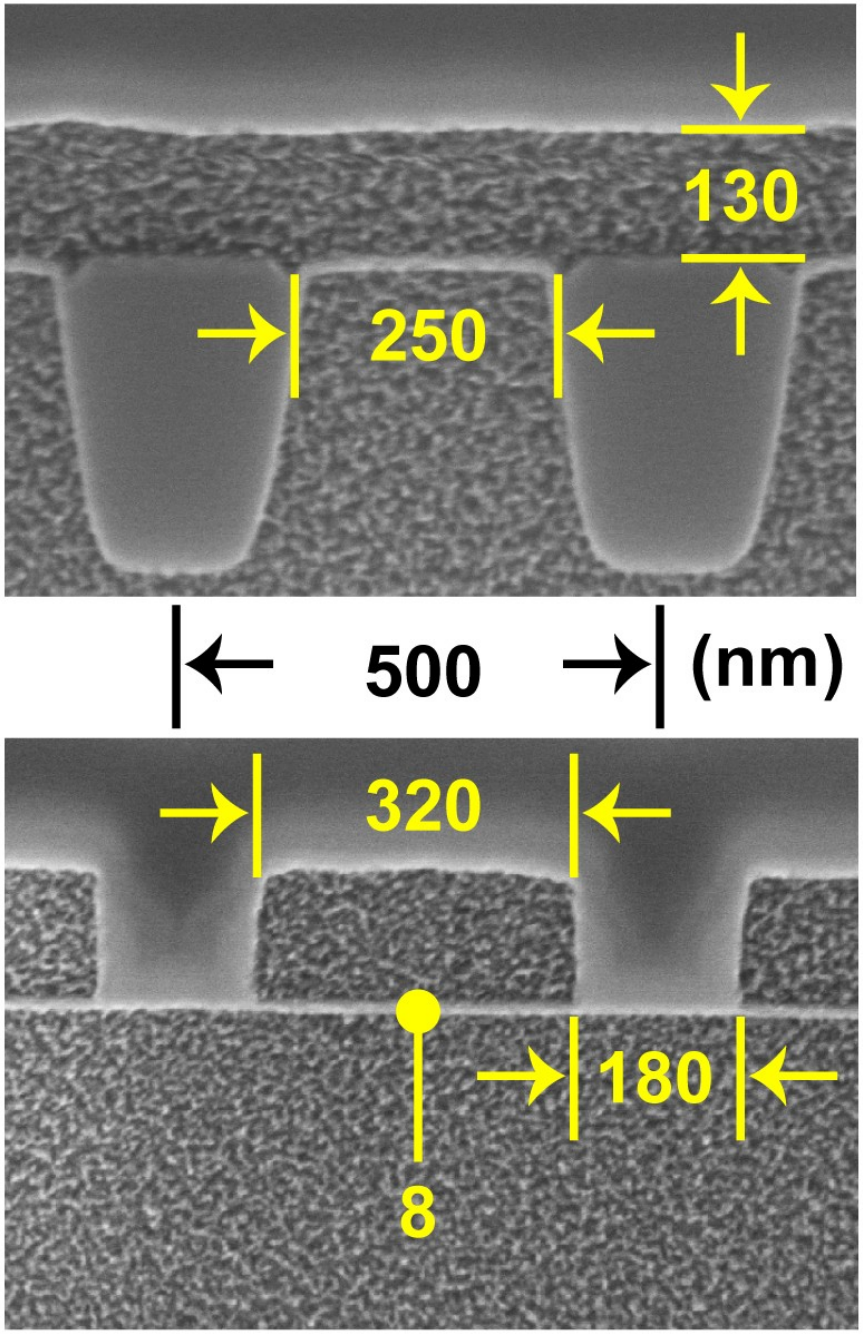
CCD Structure



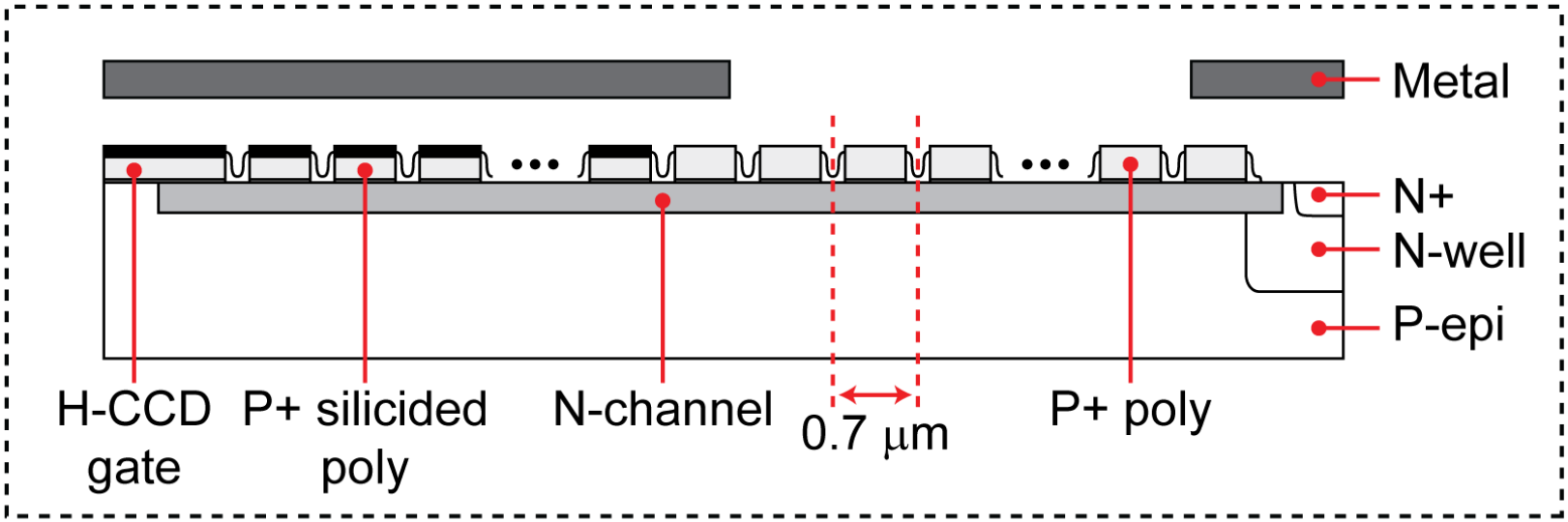
STI forms the channel stop



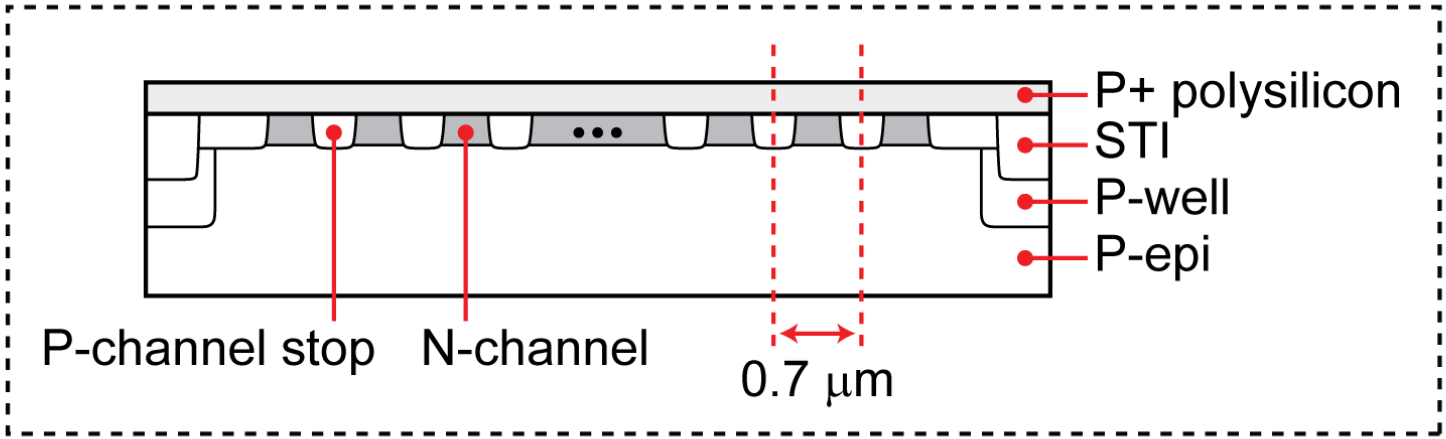
Single-level poly electrodes



The 0.7µm Buried Channel Pixel

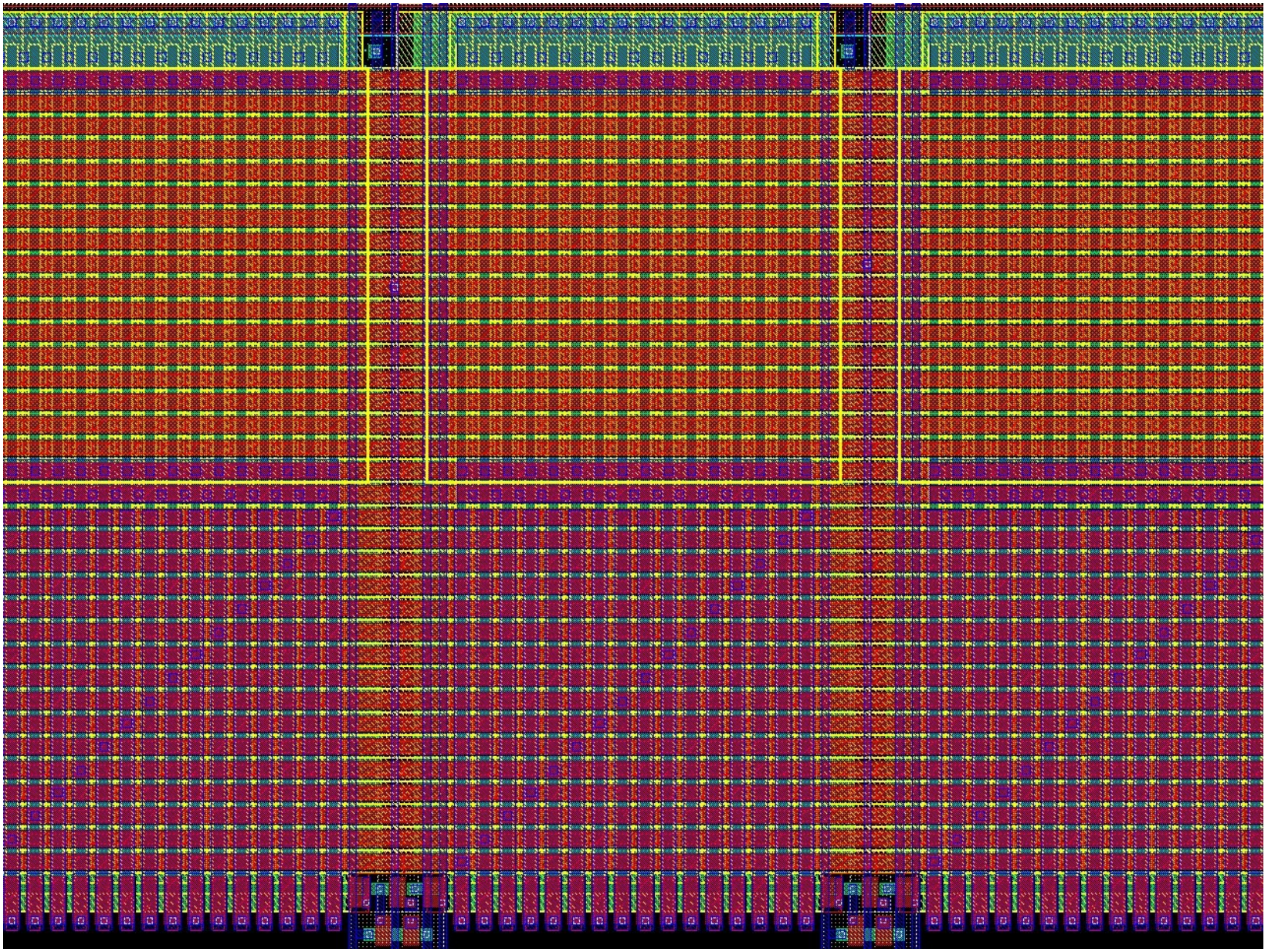


cross section along channel



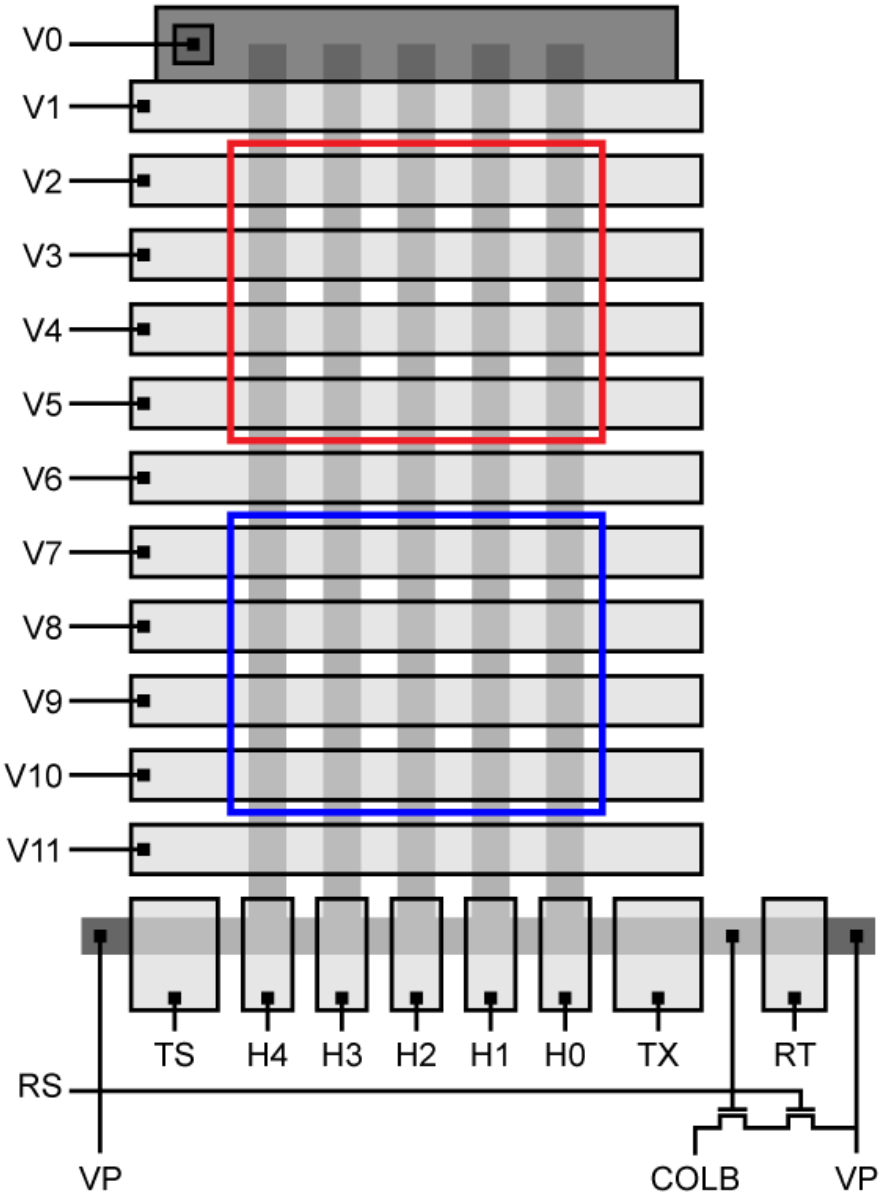
cross section against channel

Layout Masks for Buried Channel CCD

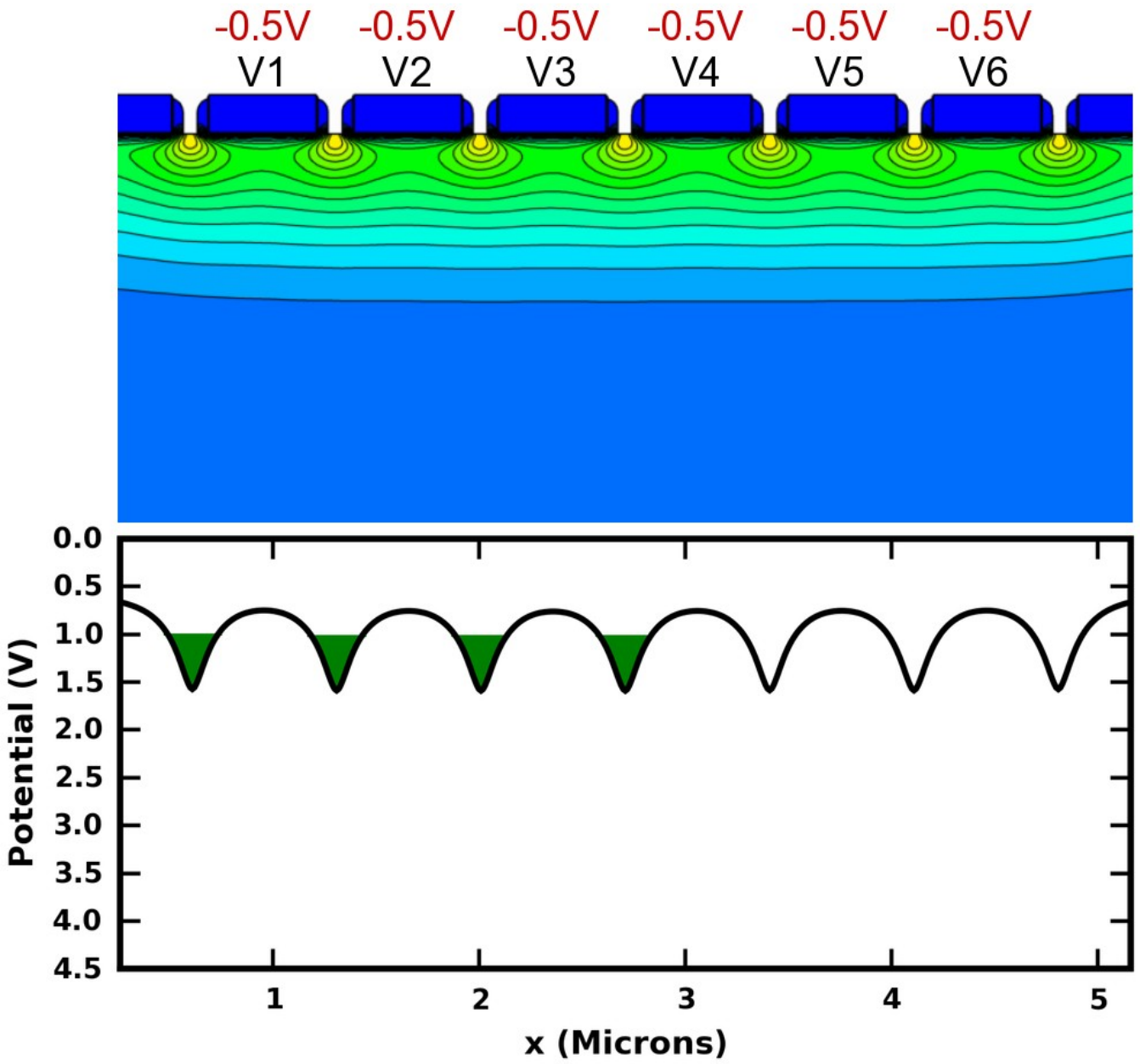


Operation

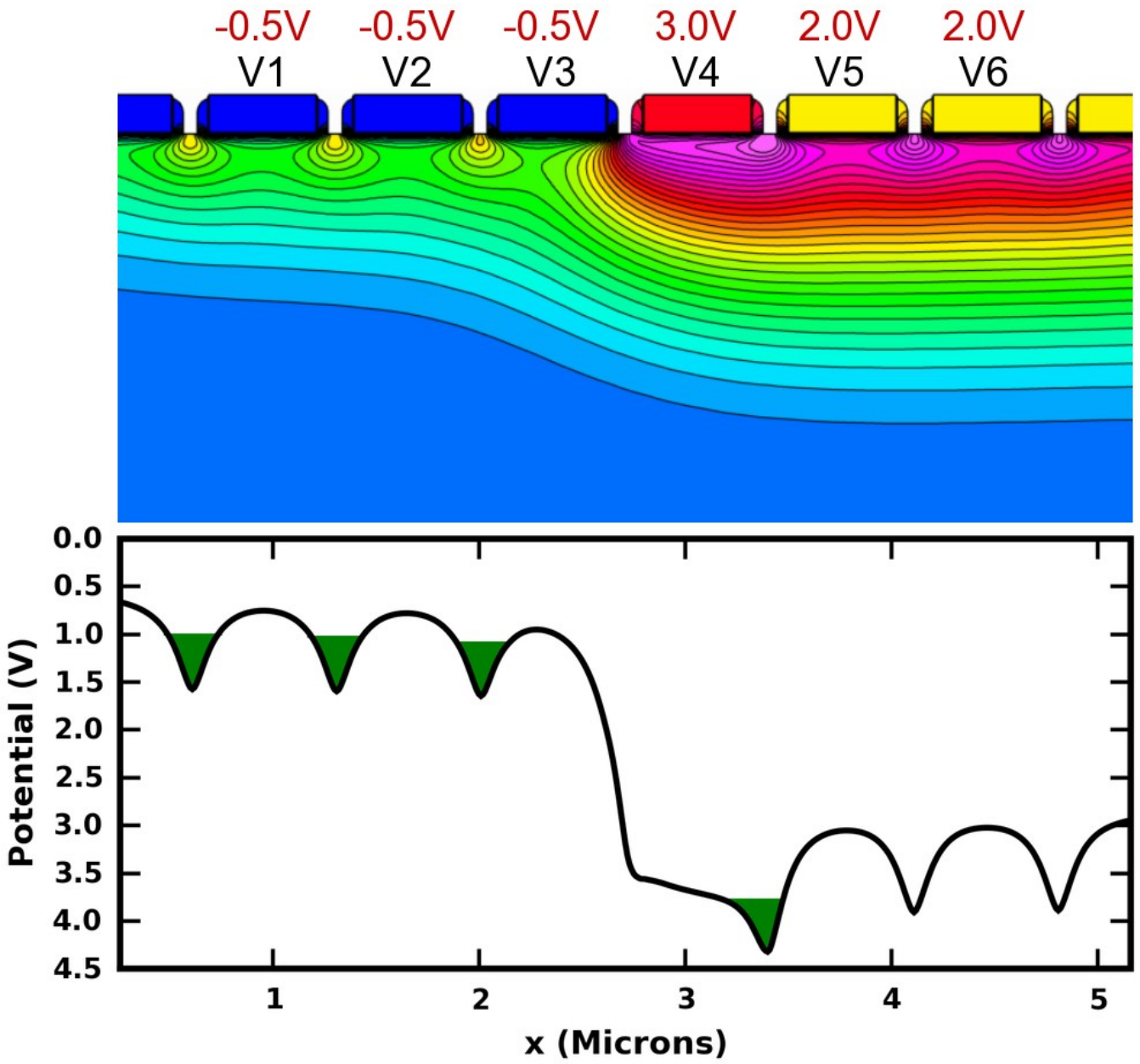
- Flush
- Integrate
- Frame Transfer
- Horizontal Readout



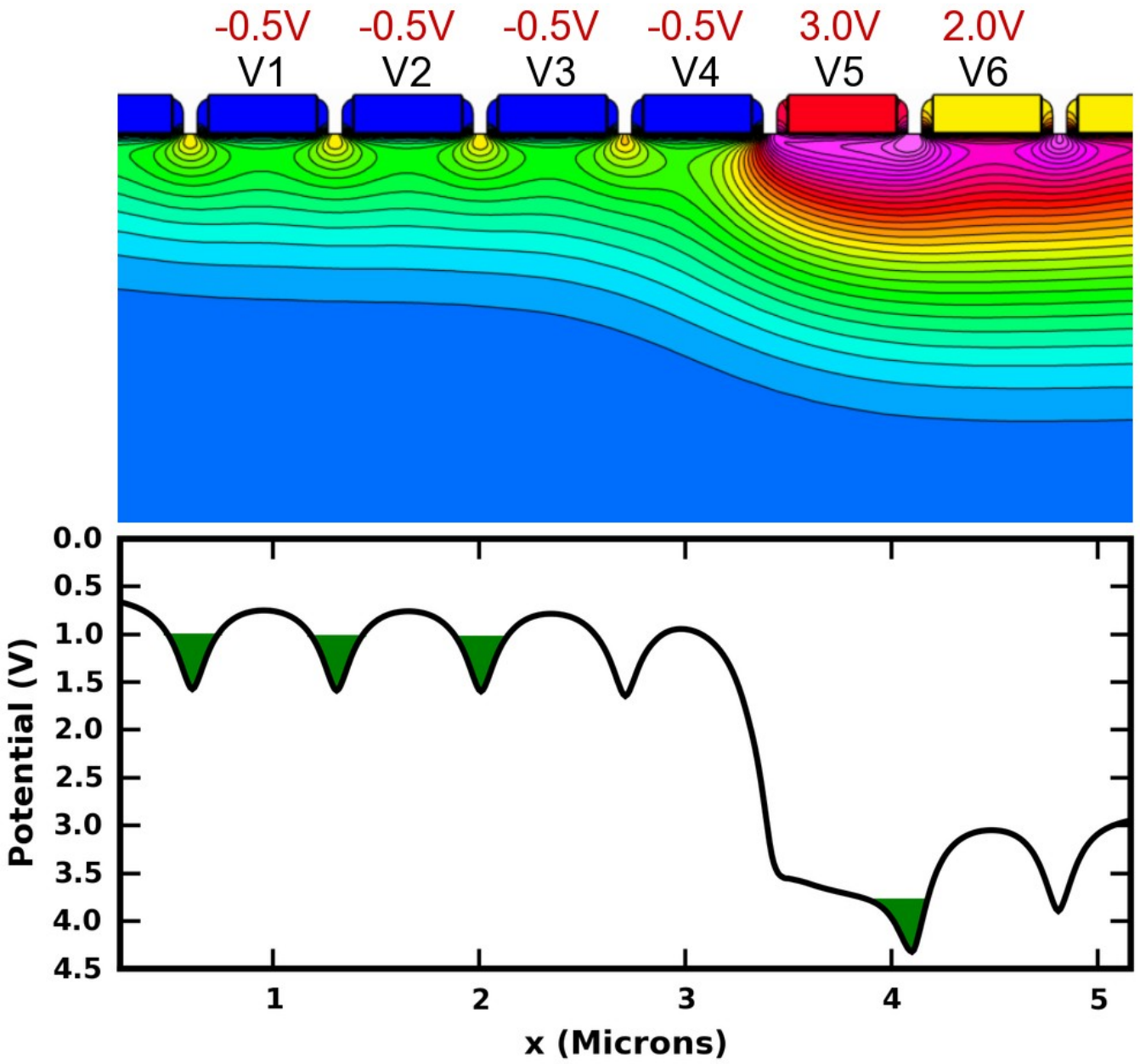
Potential Profile Along Channel



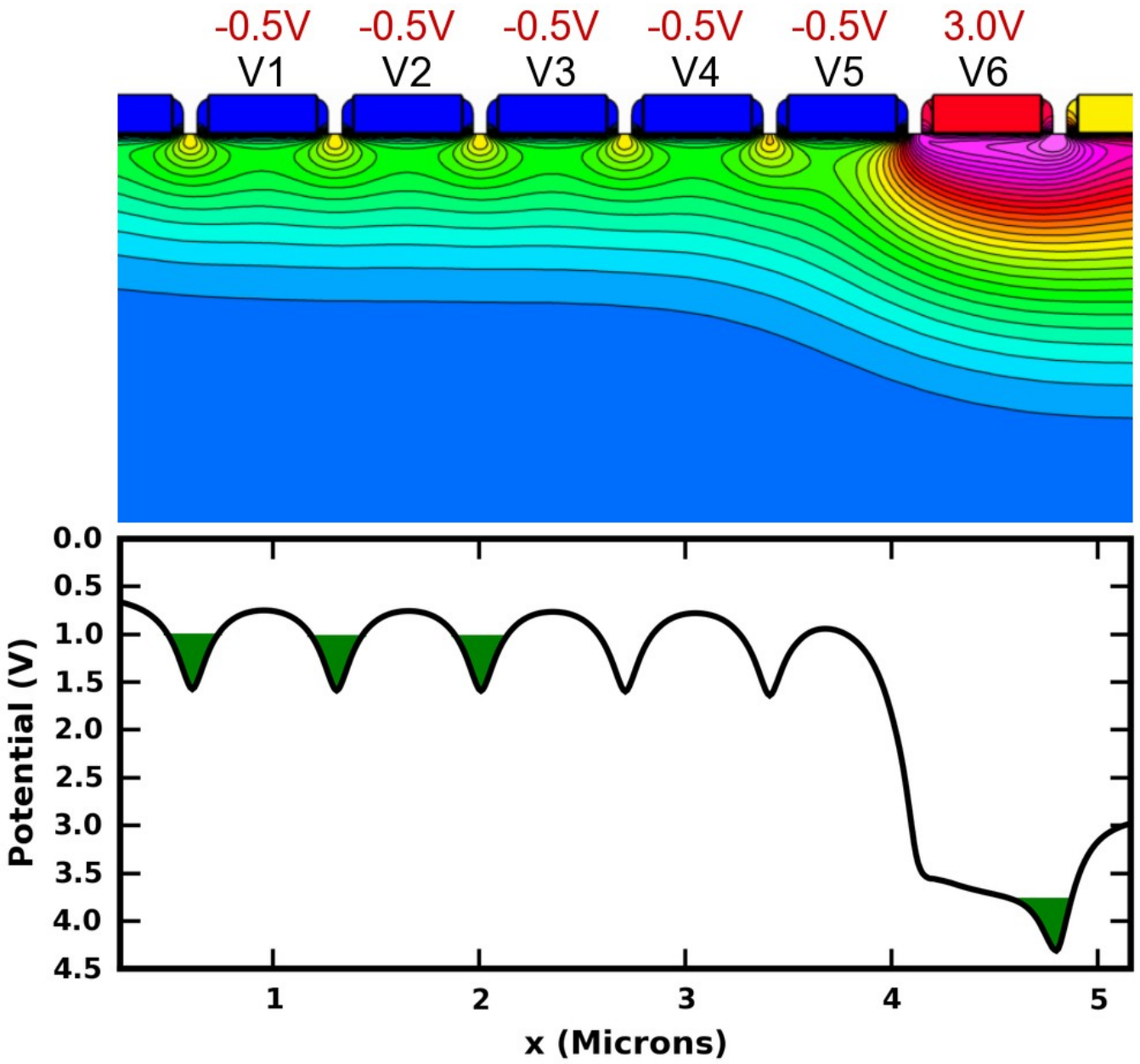
Potential Profile Along Channel



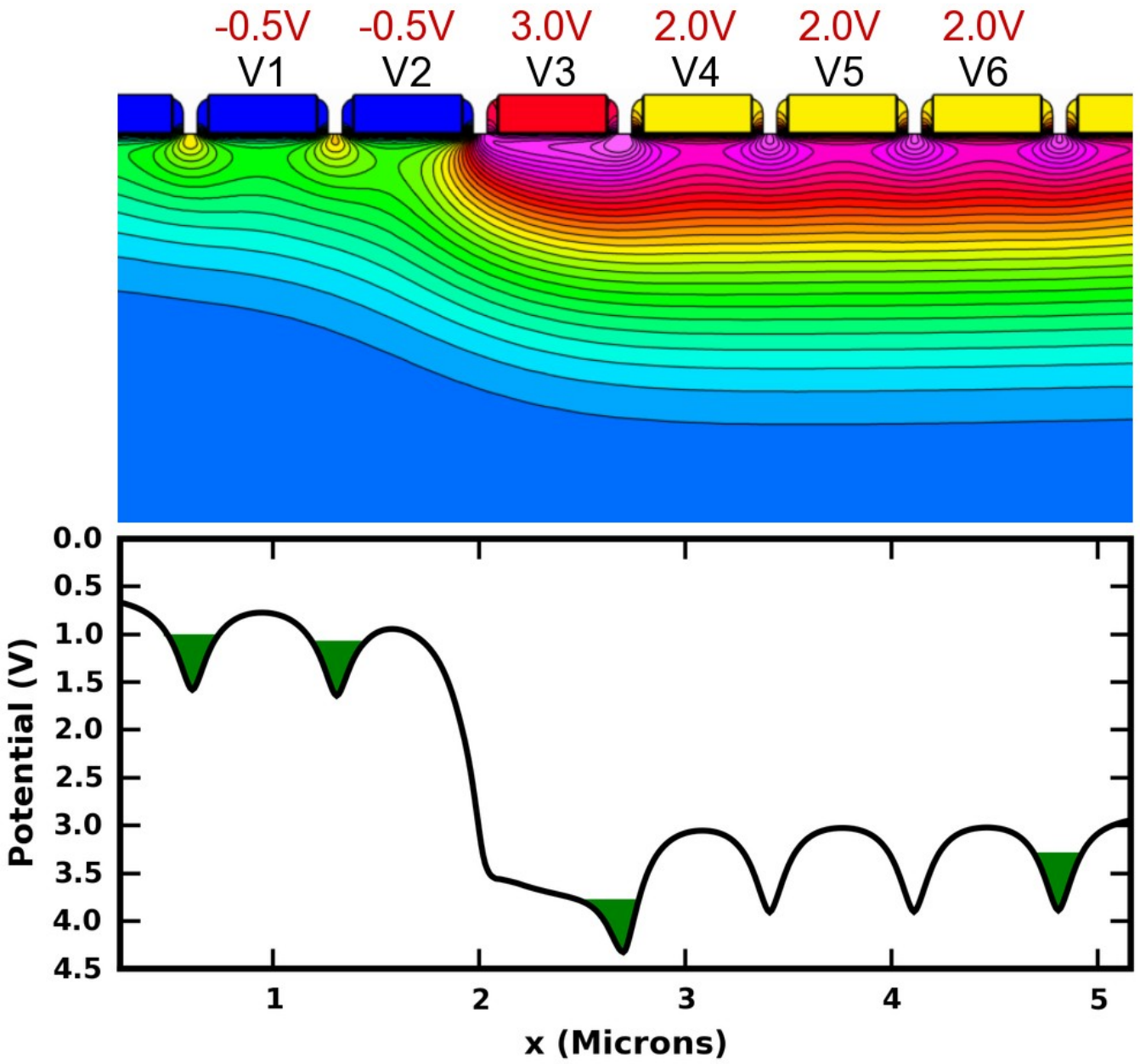
Potential Profile Along Channel



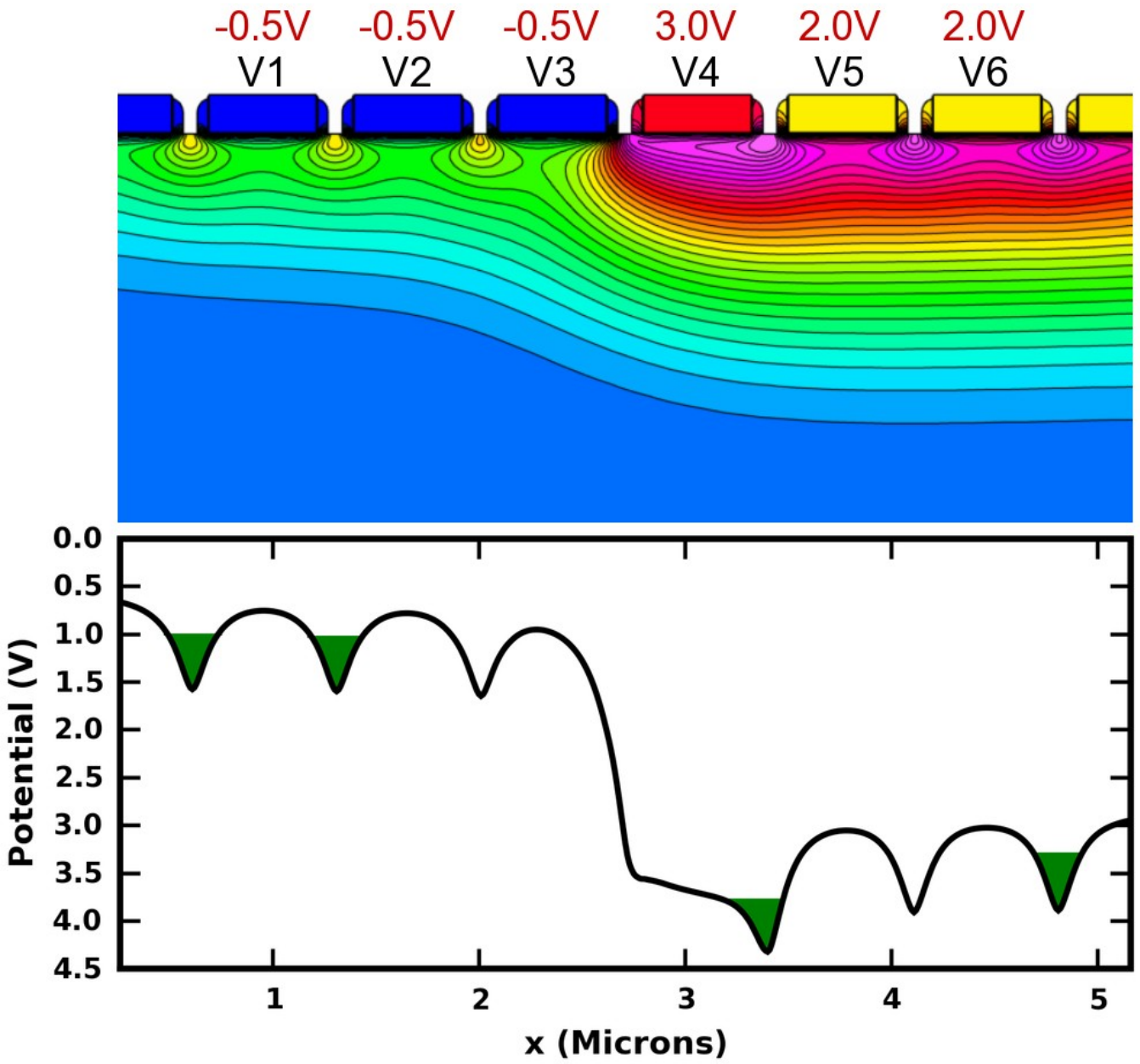
Potential Profile Along Channel



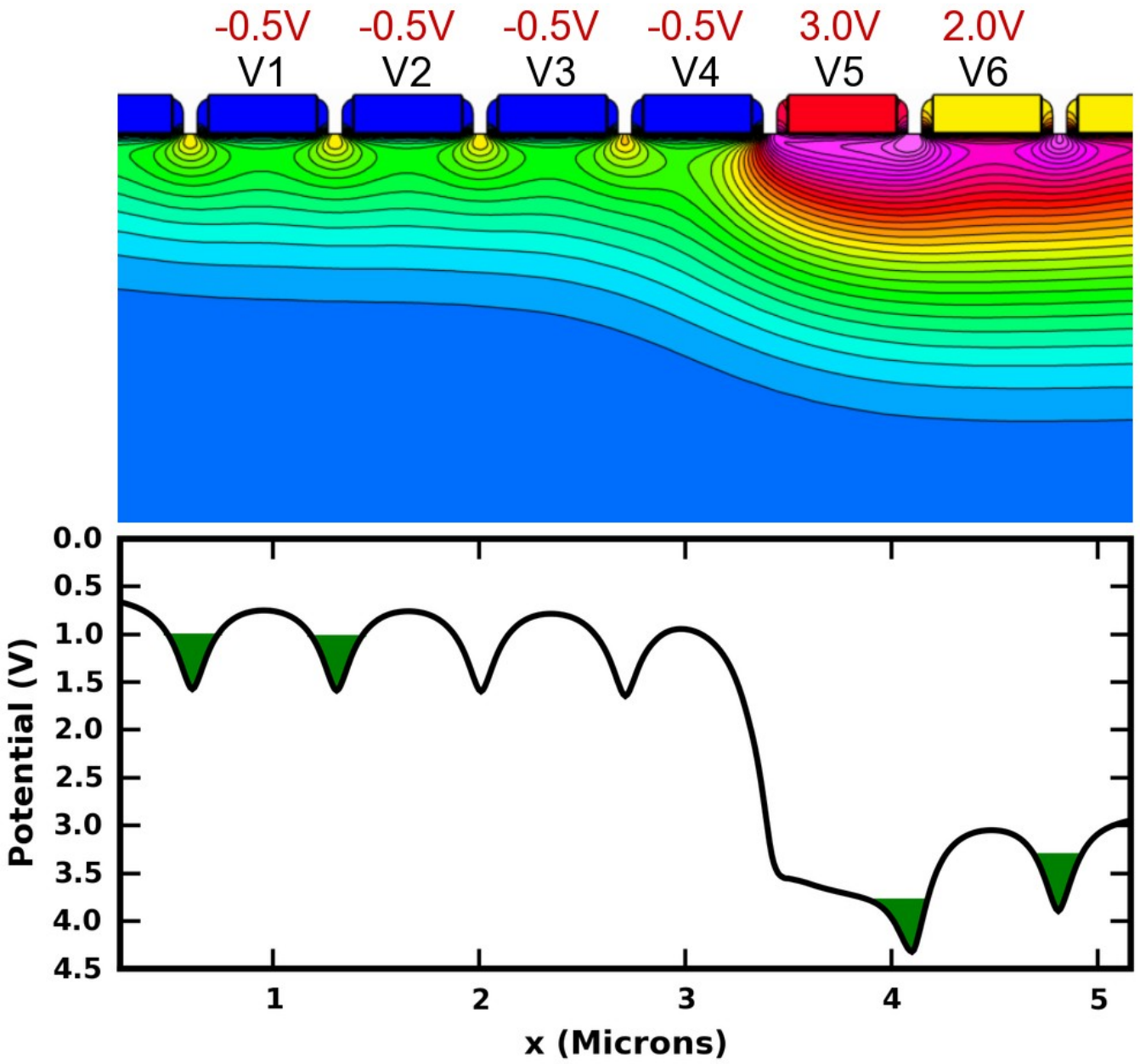
Potential Profile Along Channel



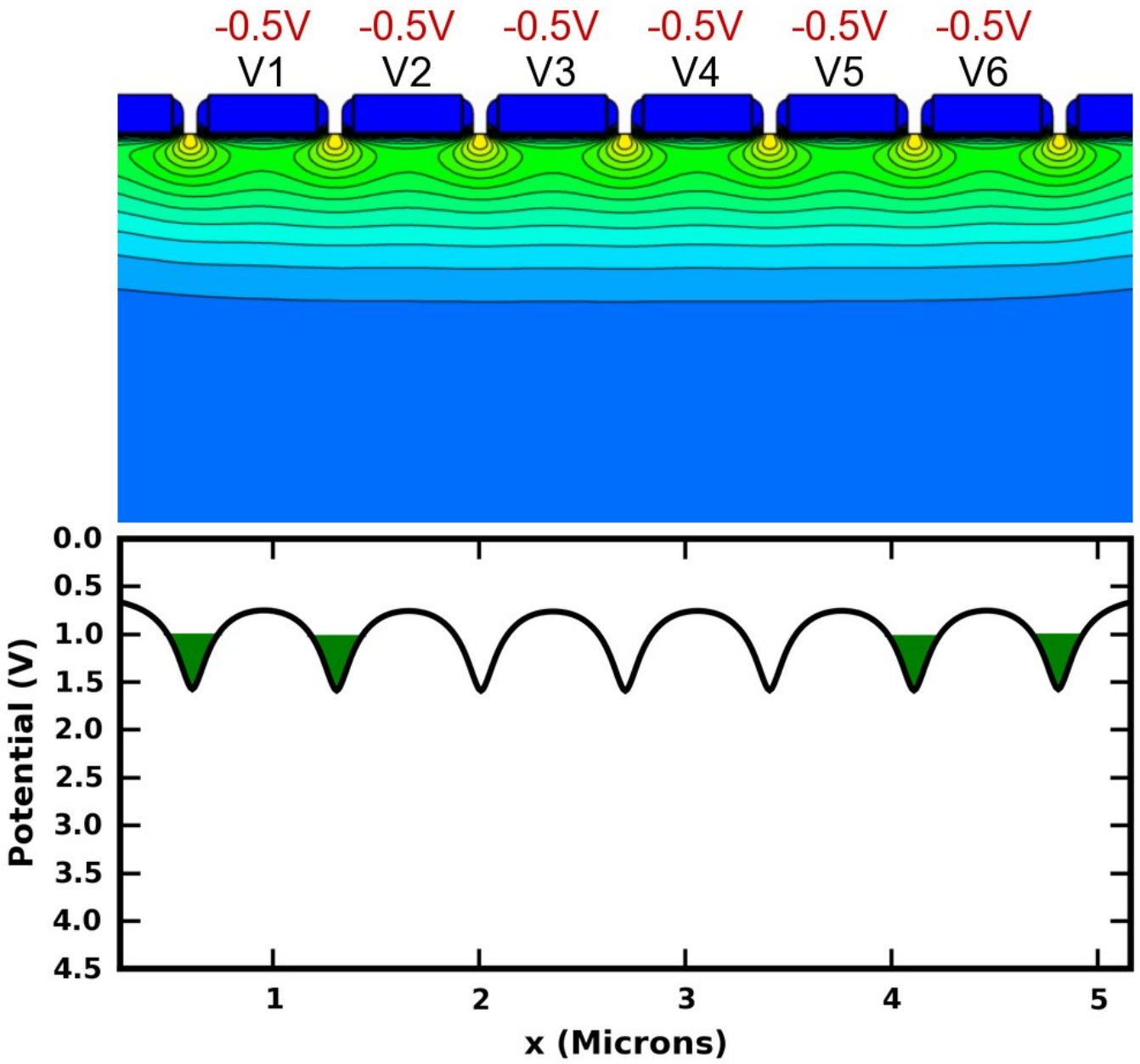
Potential Profile Along Channel



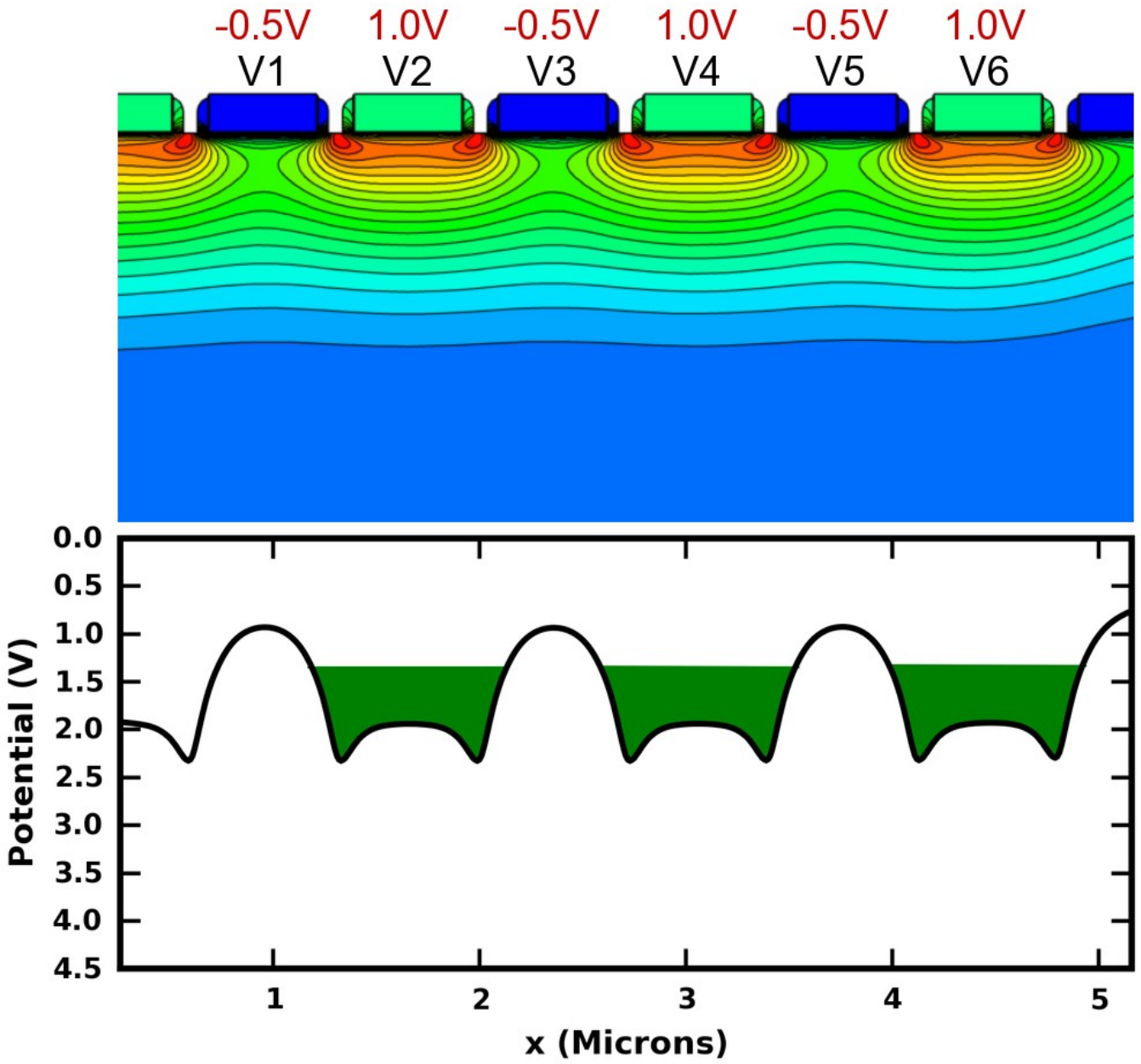
Potential Profile Along Channel



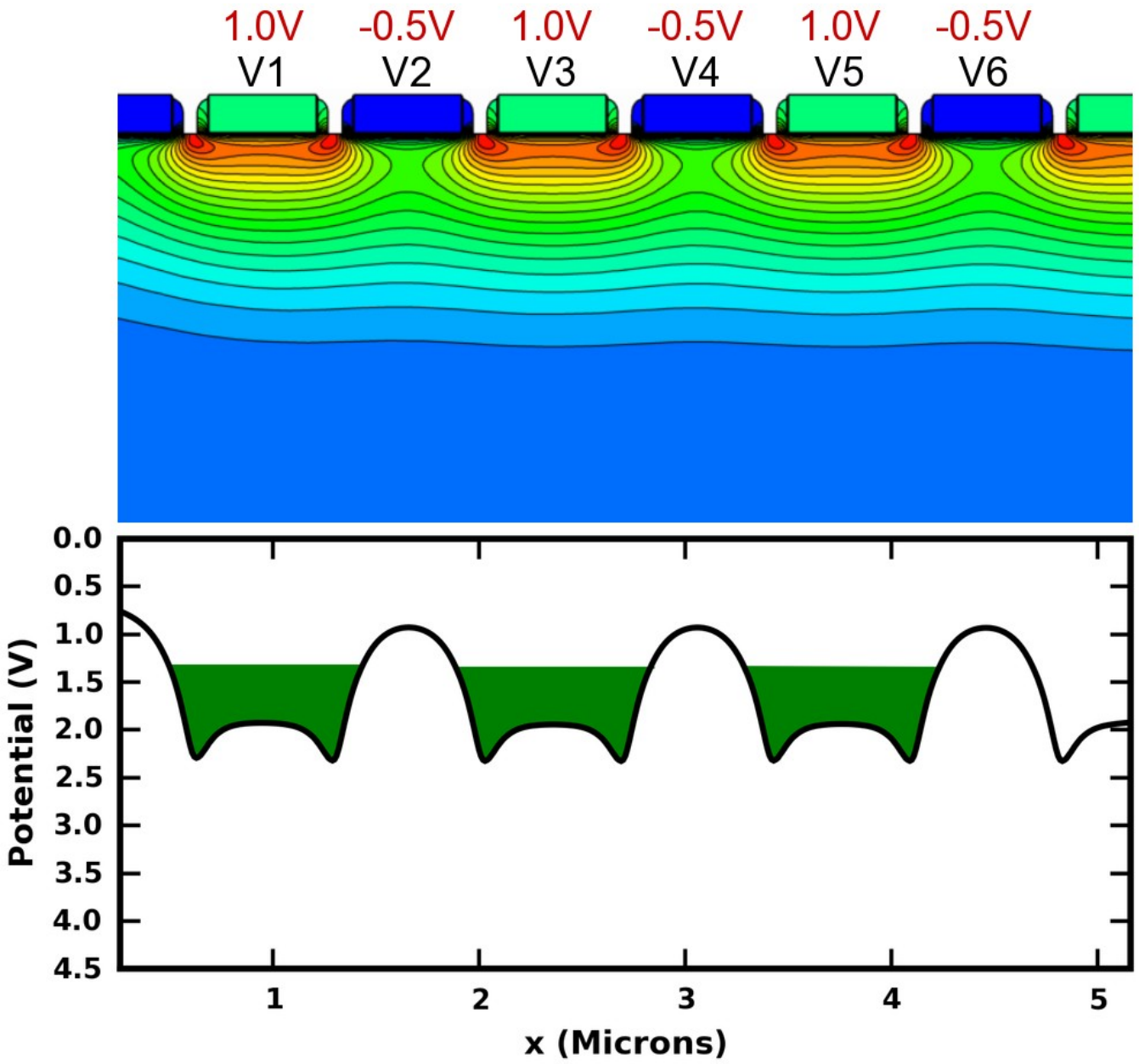
Potential Profile Along Channel



Interlaced Mode (Even Field)

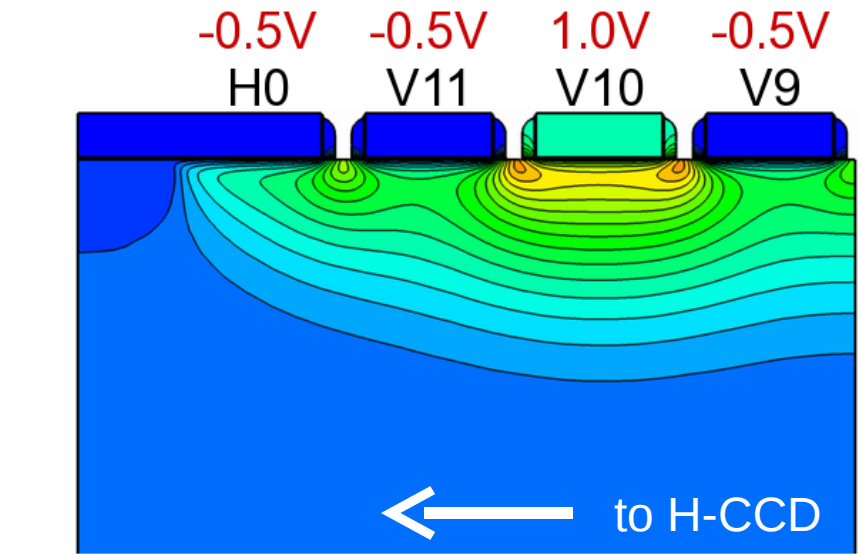


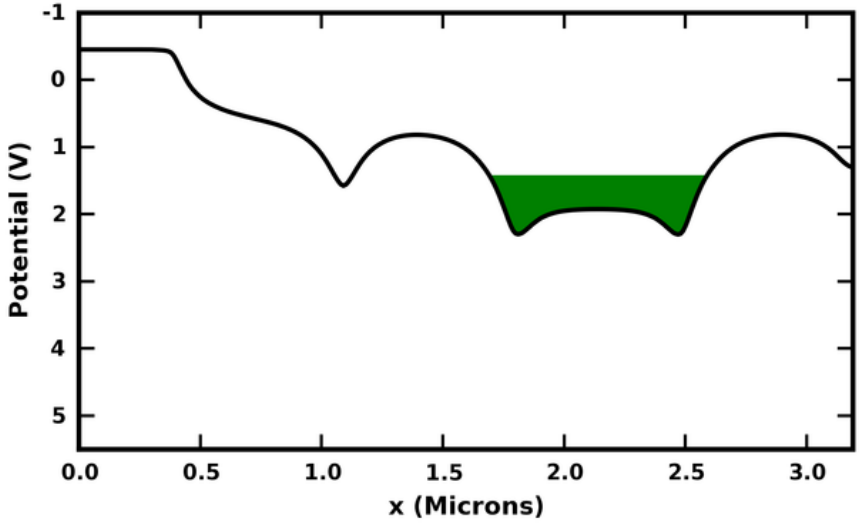
Interlaced Mode (Odd Field)



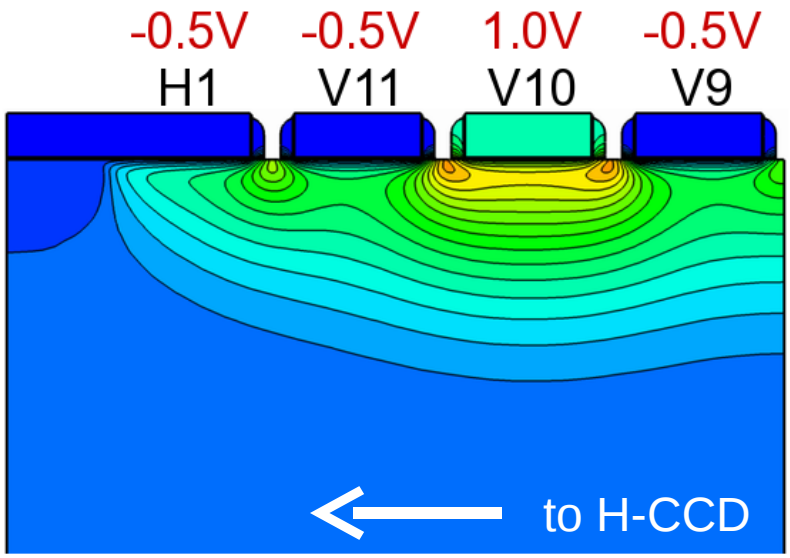
Vertical to Horizontal Transfer

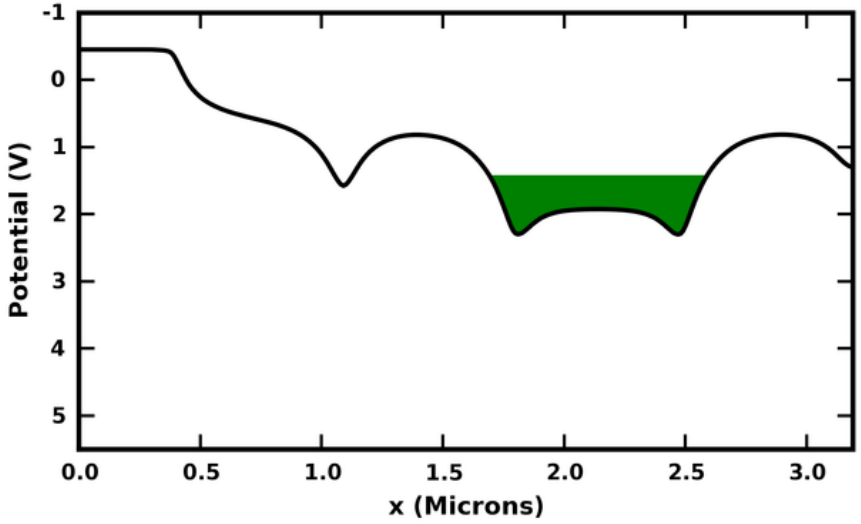
Even column





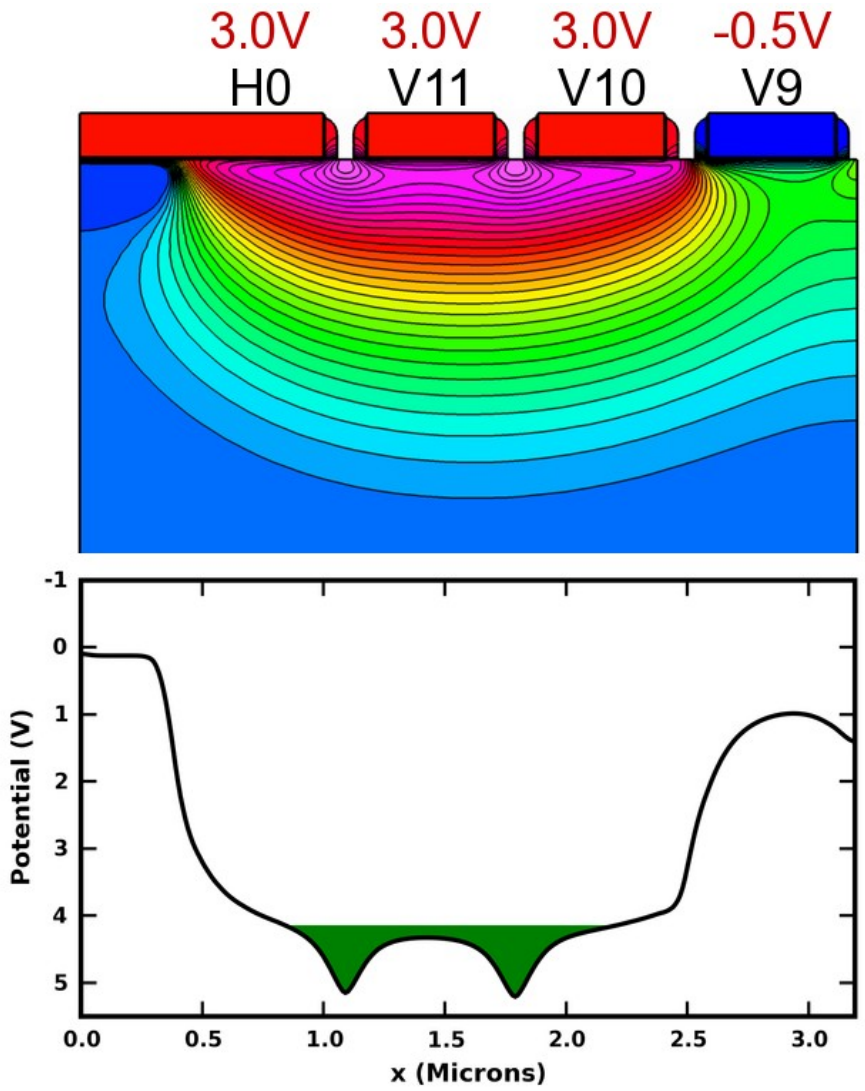
Odd column



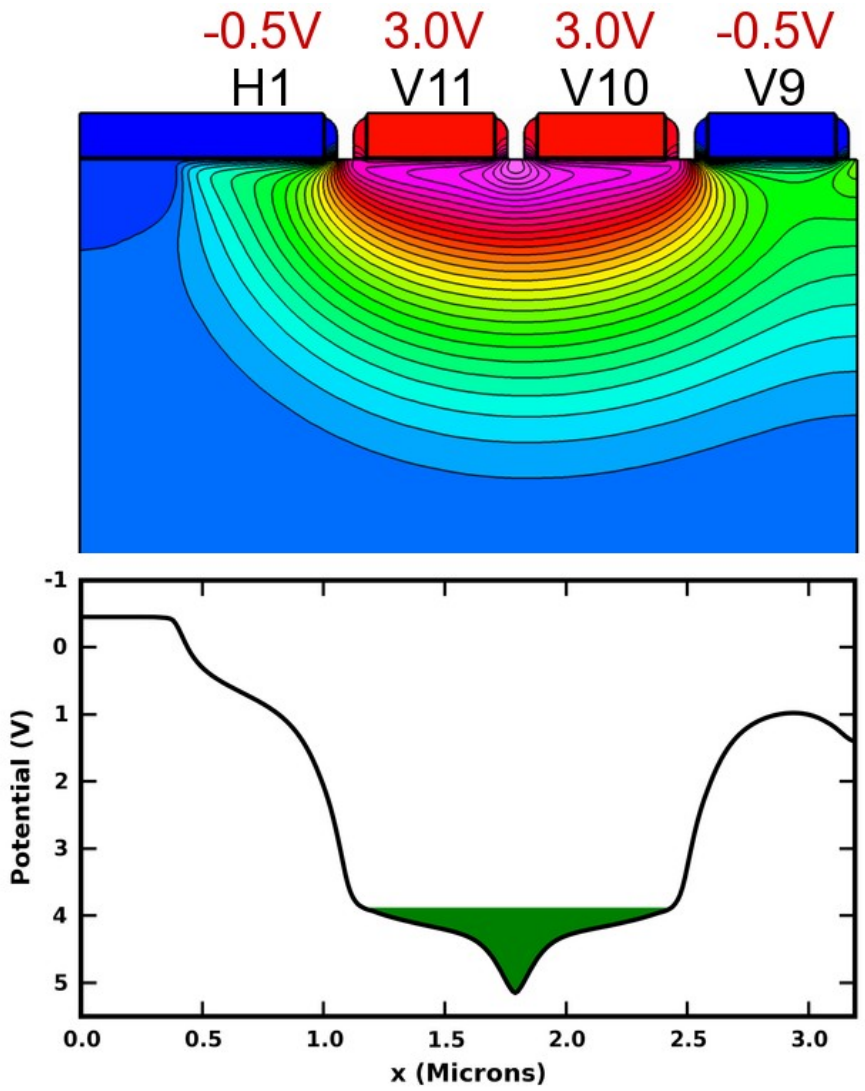


Vertical to Horizontal Transfer

Even column

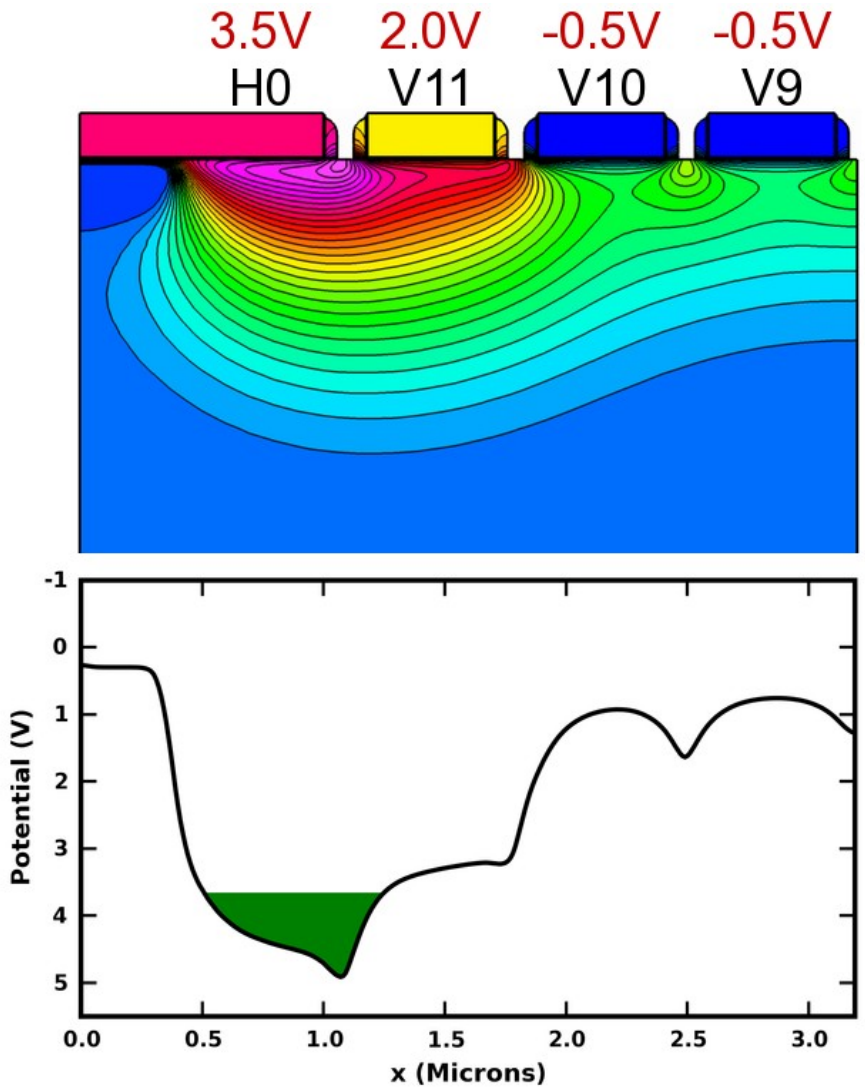


Odd column

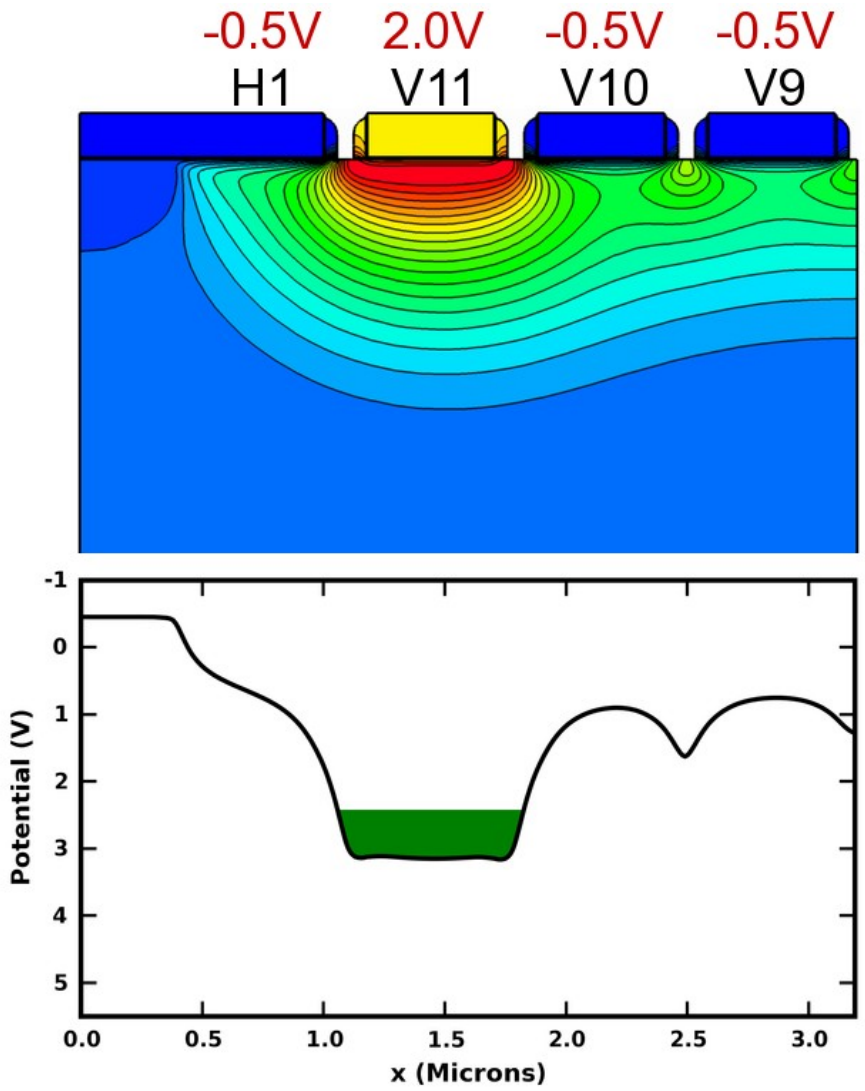


Vertical to Horizontal Transfer

Even column

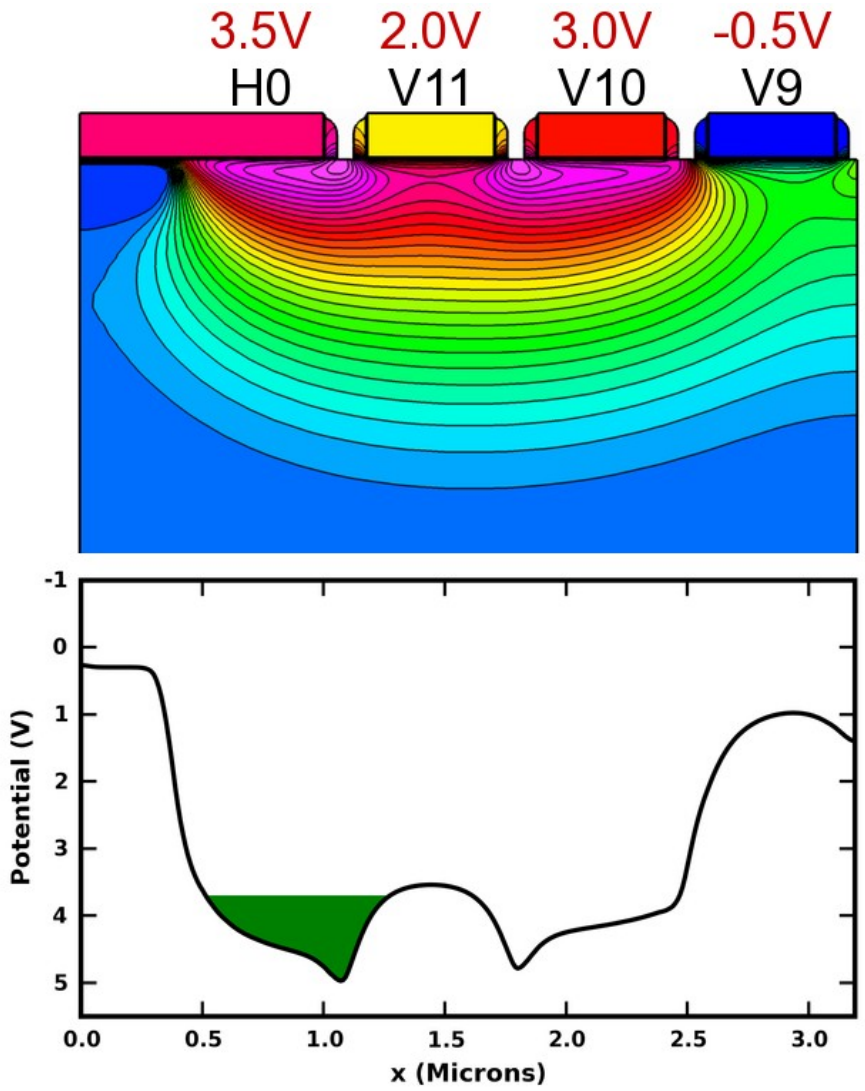


Odd column

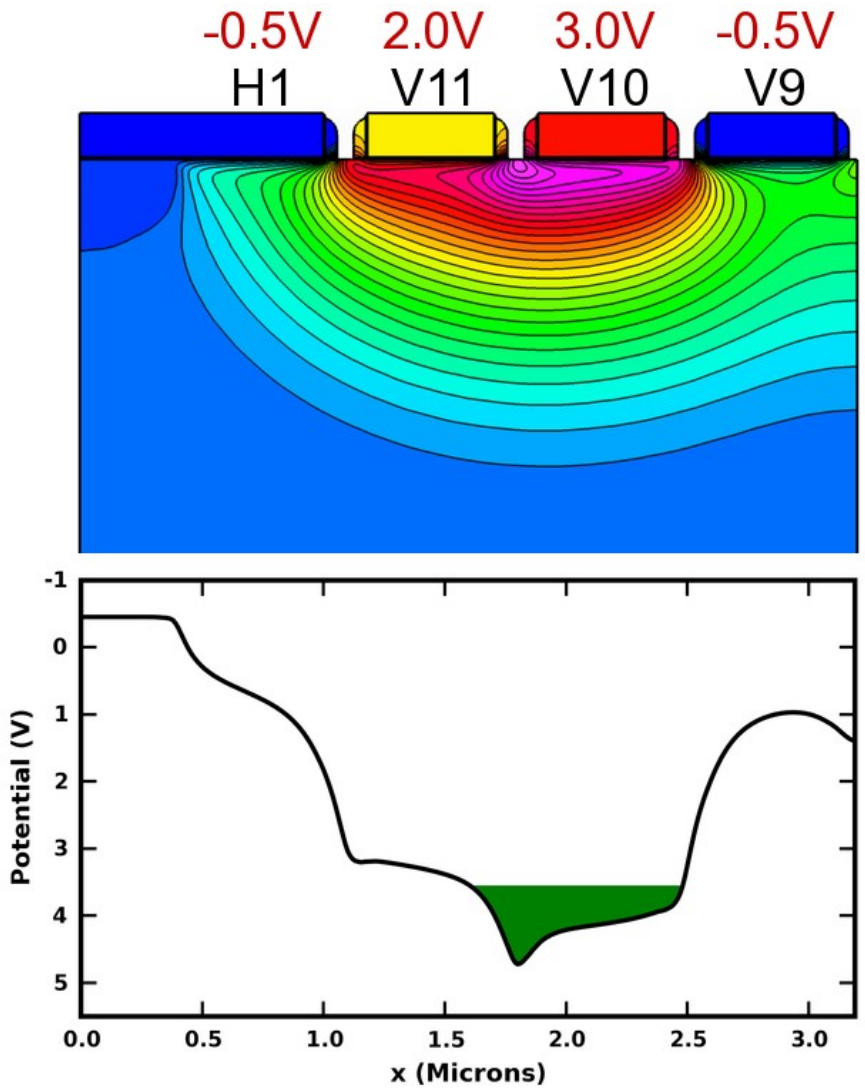


Vertical to Horizontal Transfer

Even column

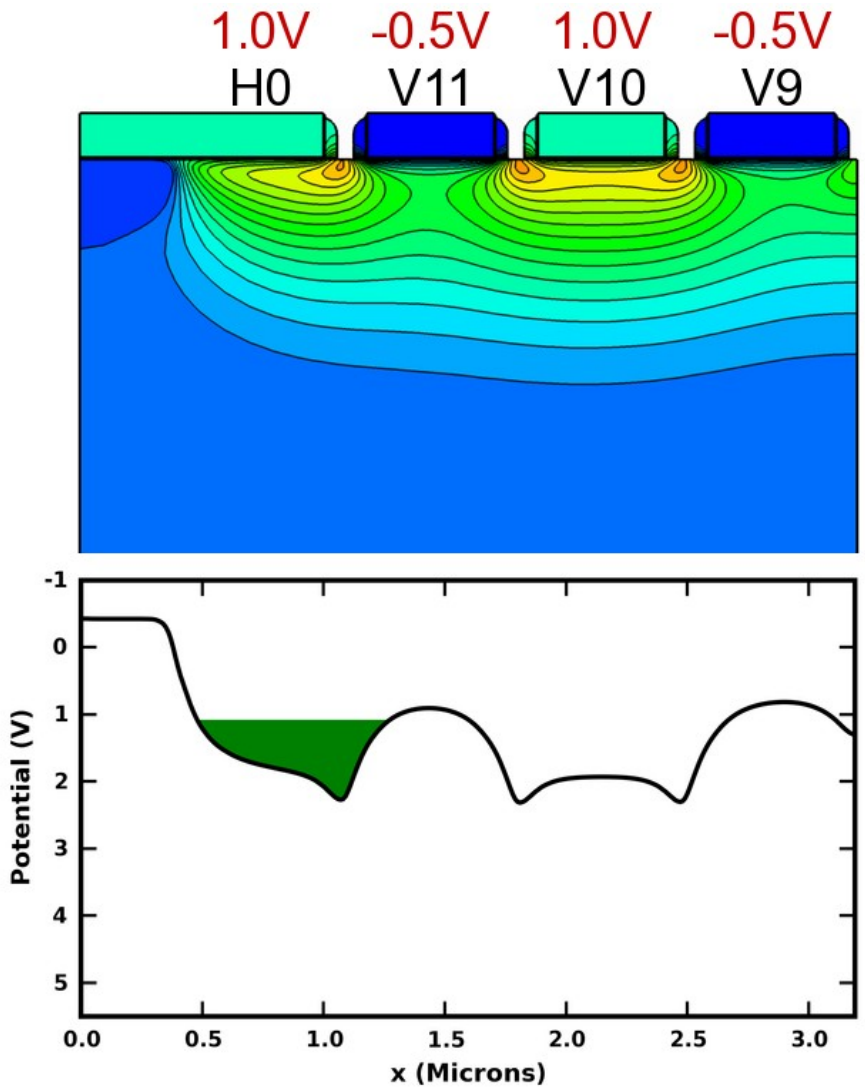


Odd column

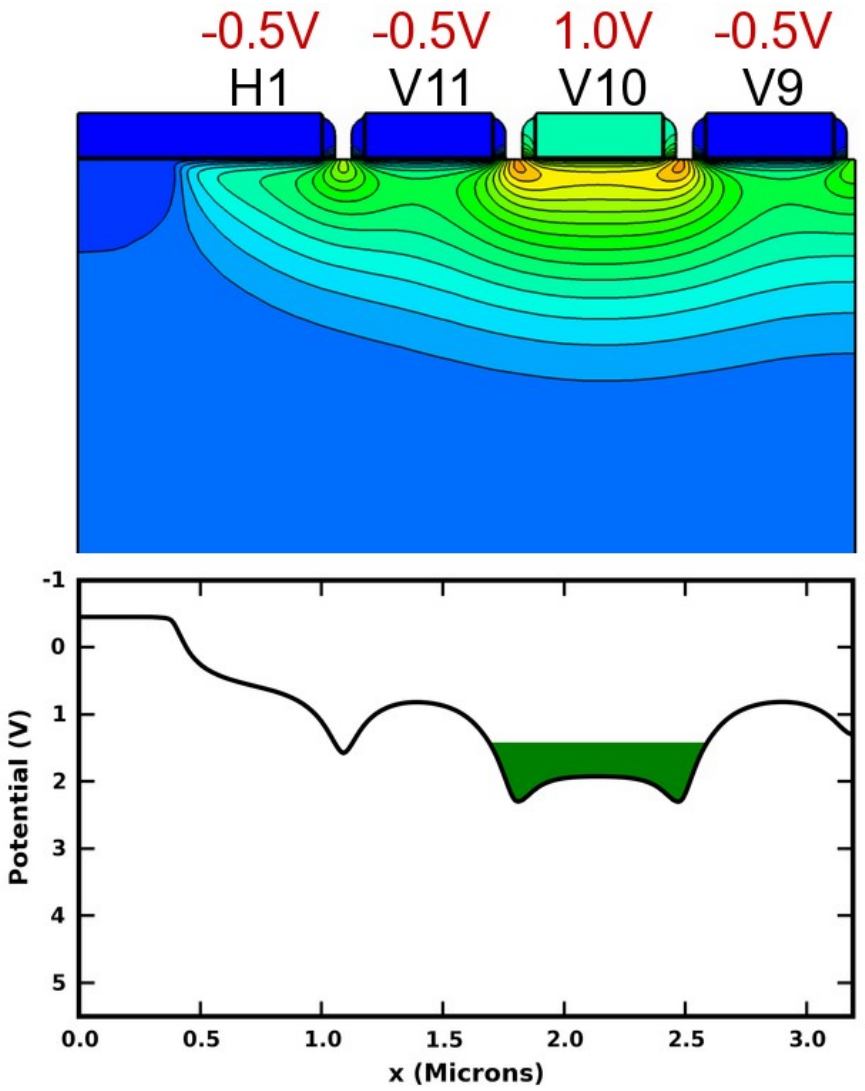


Vertical to Horizontal Transfer

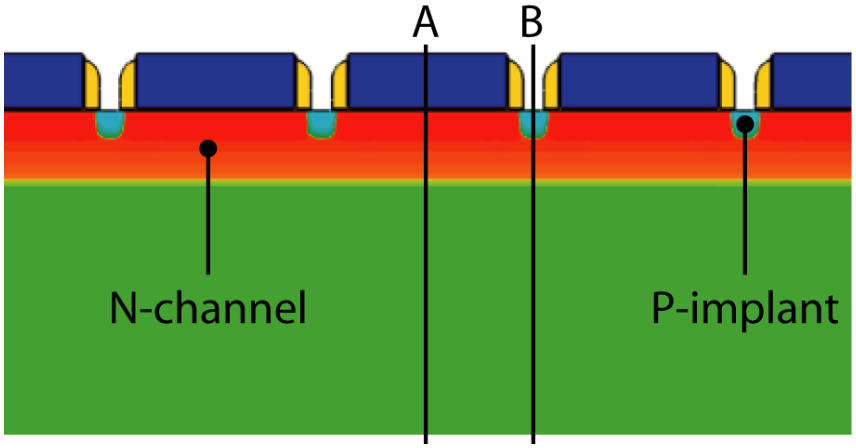
Even column

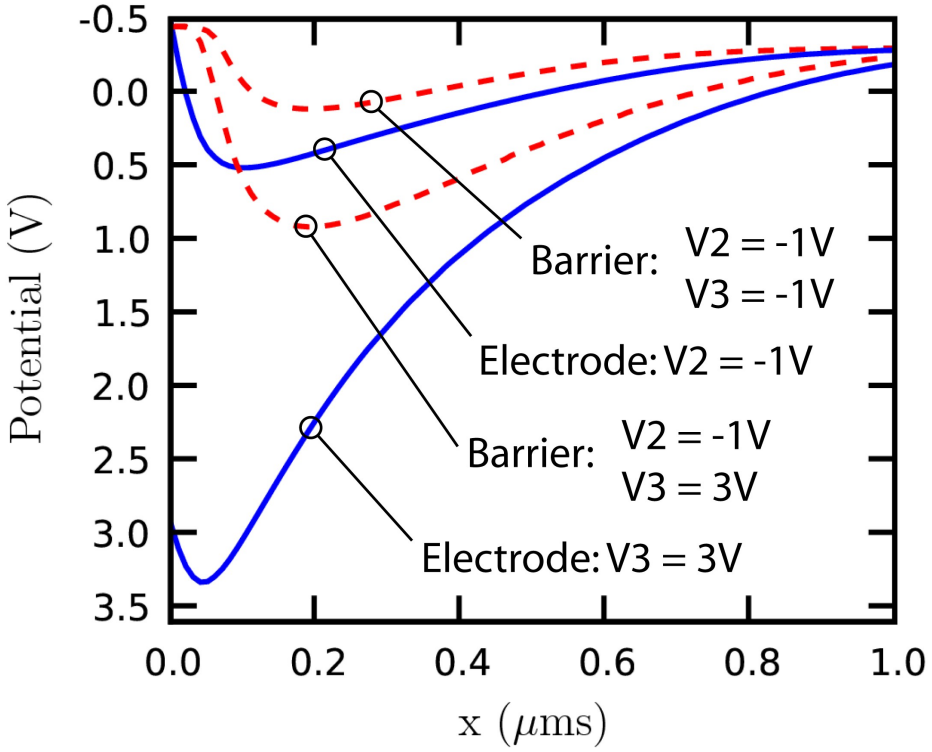


Odd column



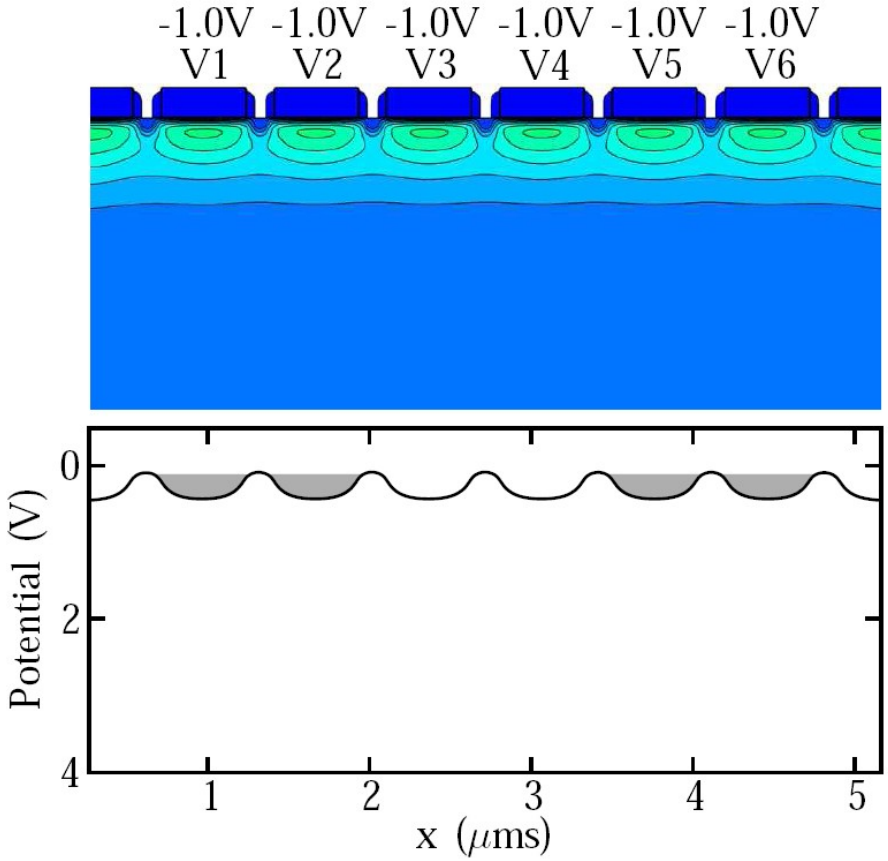
Pinned-Phase Buried Channel

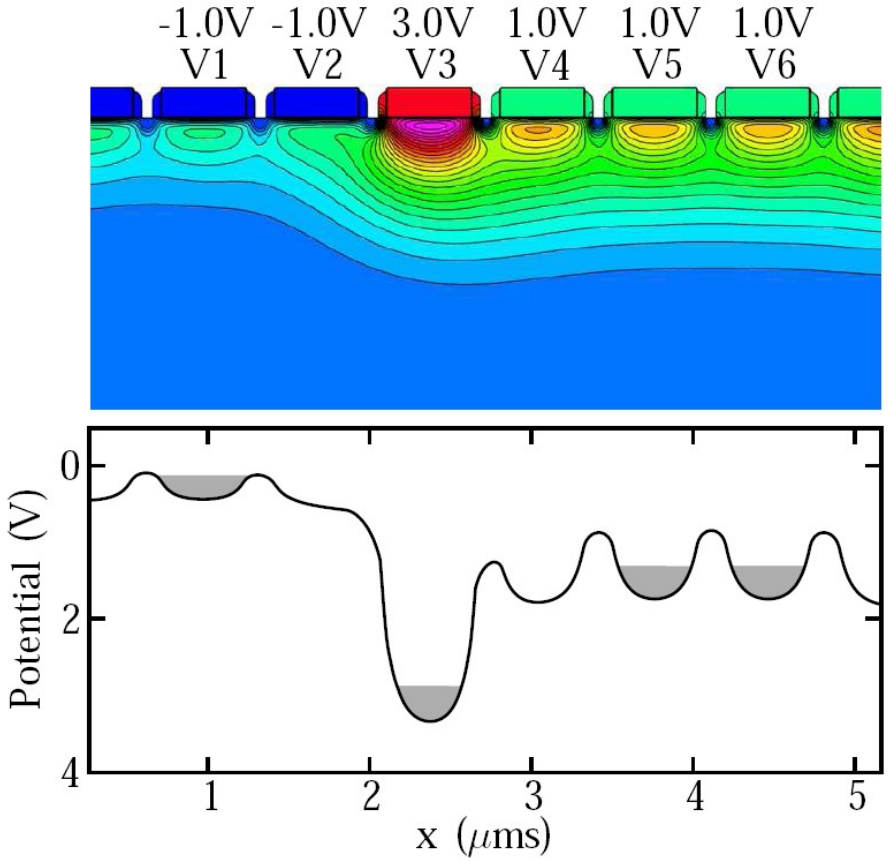




Pinned-Phase Buried Channel

- Charge confinement achieved while surface is inverted during integration time
- Charge transfer achieved with application of high electrode voltages to overcome barriers

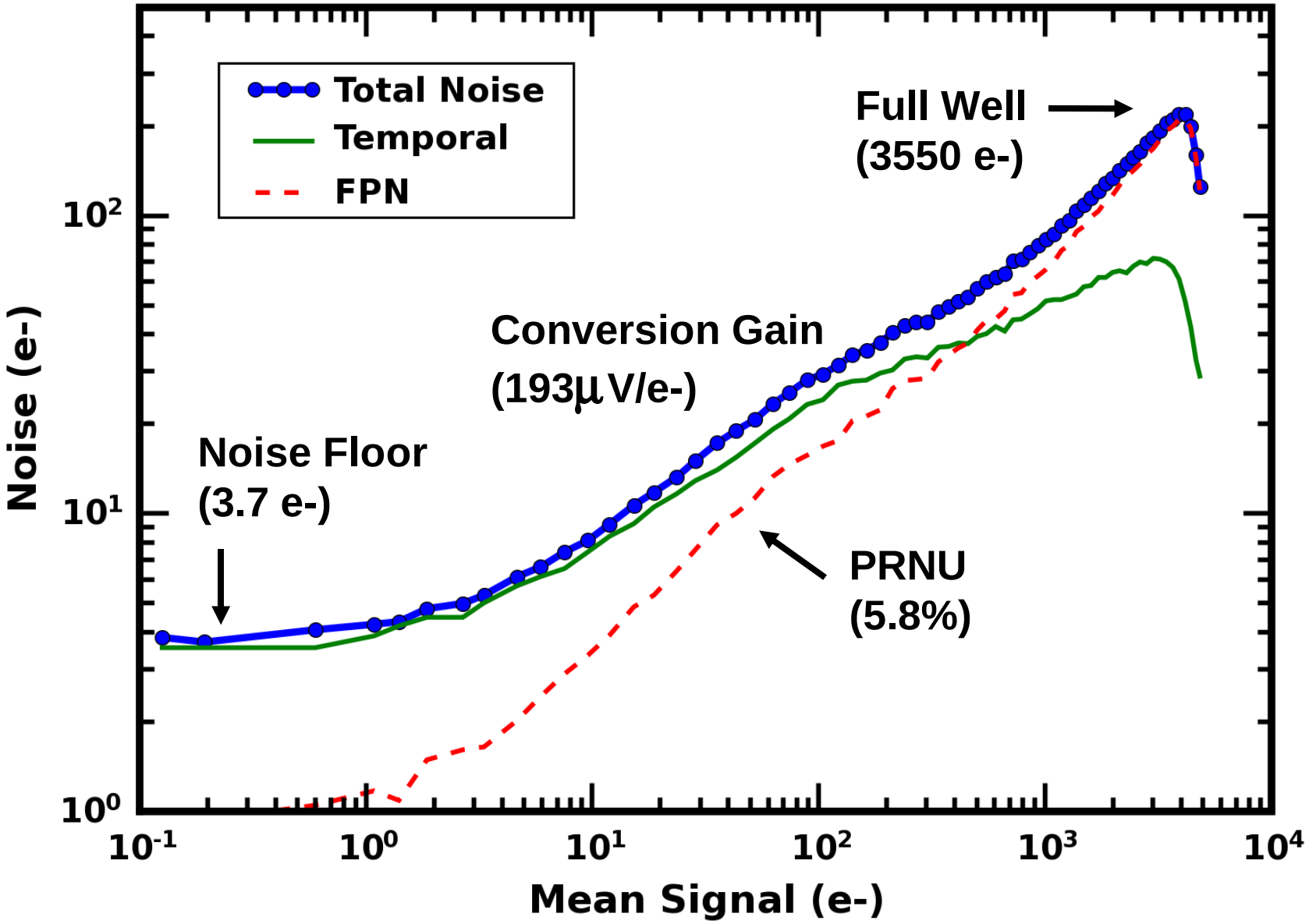




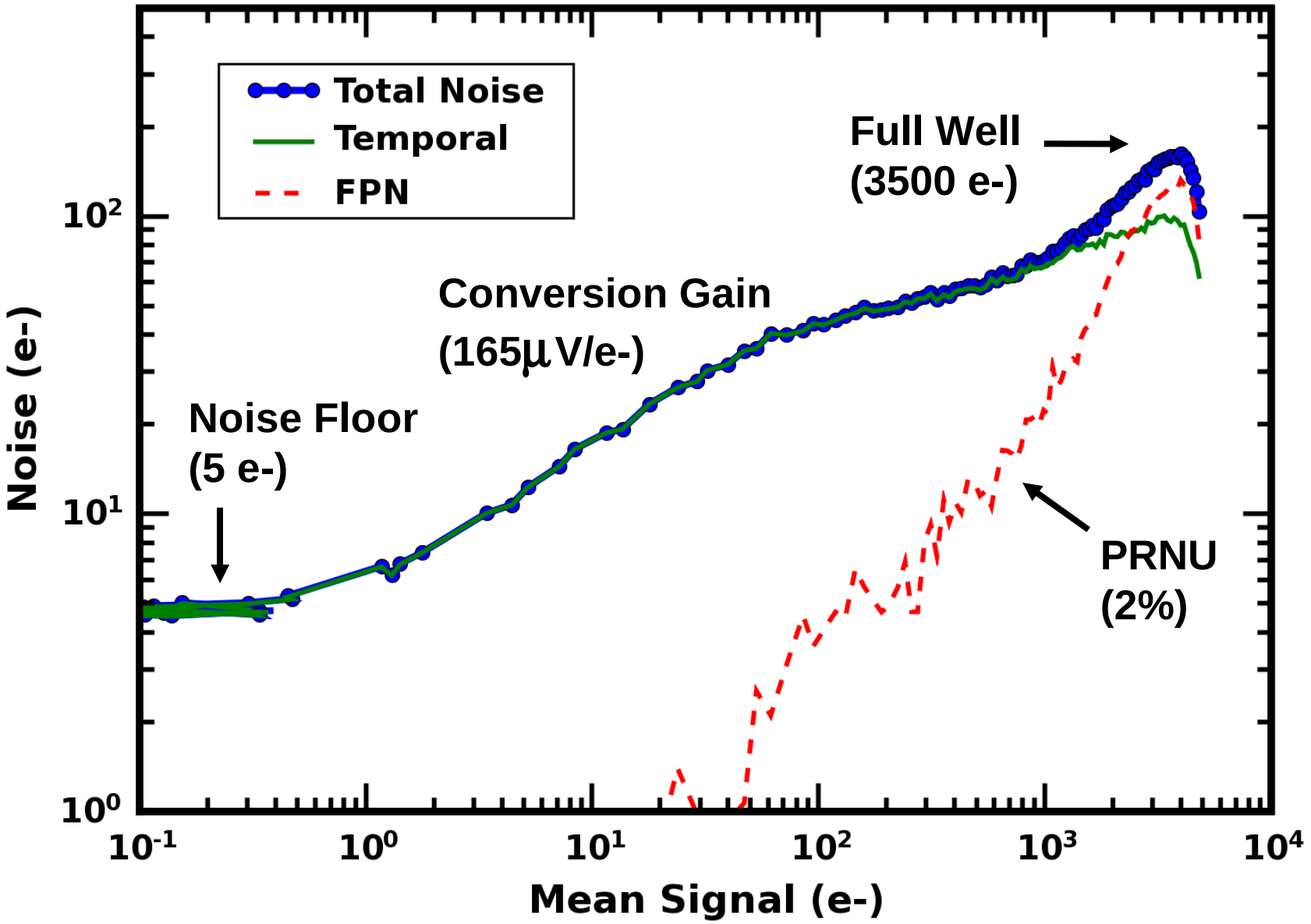
Pinned-Phase Buried Channel

- Dark current decreases by factor of 15 over buried channel device.
- Detailed characterization of the device is in progress.
  - Difficult to measure charge transfer efficiency using fill/spill circuit.
  - Well capacity is lower than 500 electrons.

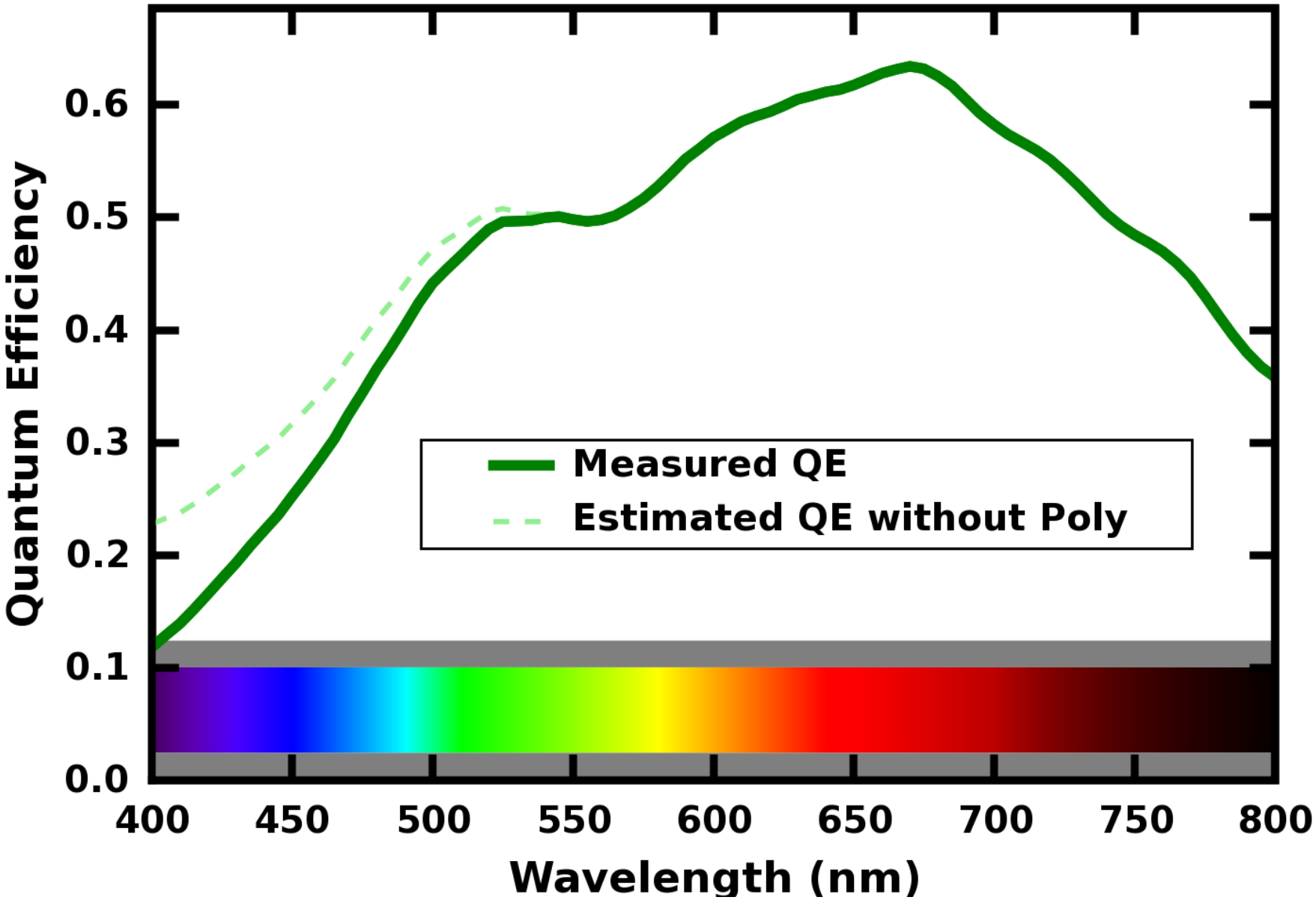
PTC (Surface-channel, 0.5µm Pixel)



PTC (Buried-channel, 0.7µm Pixel)

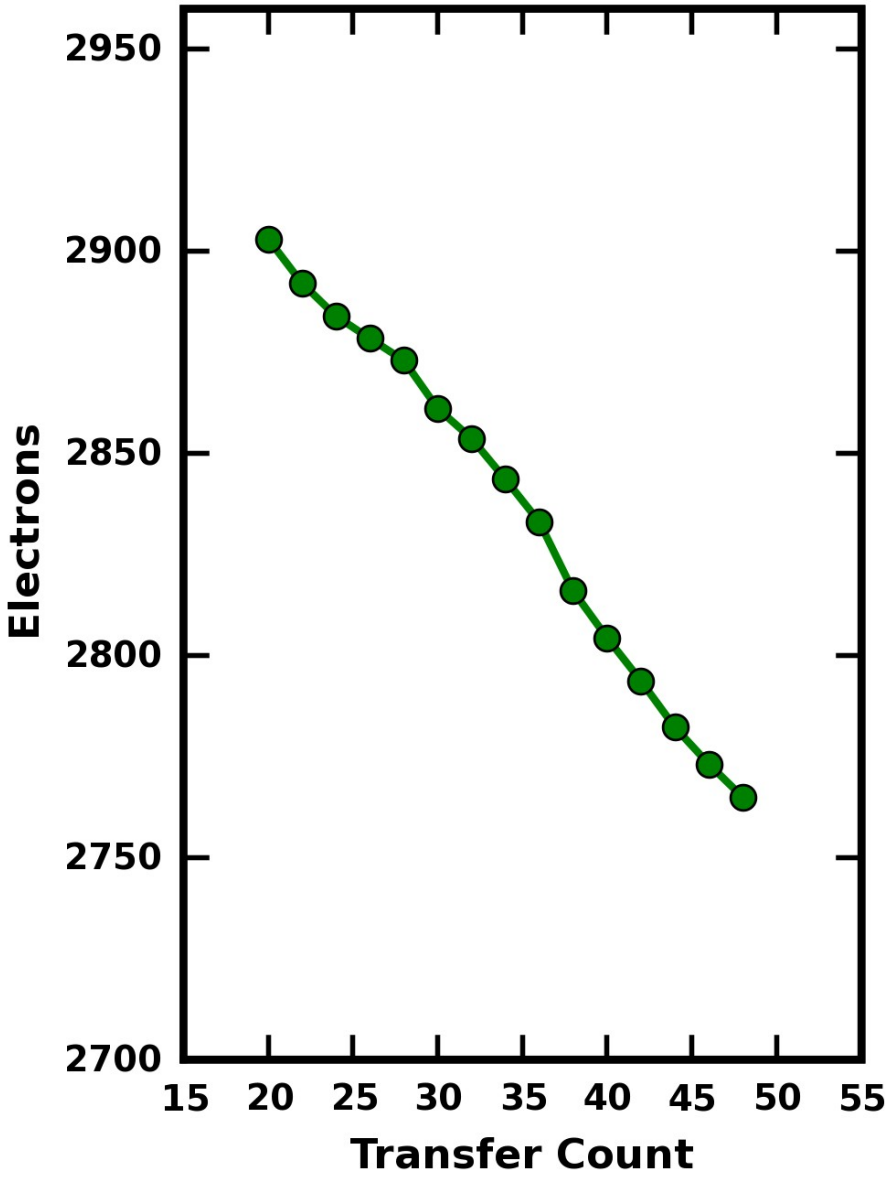


Measured Quantum Efficiency



Measured Charge Transfer Efficiency

- CTE is 99.9% with 3000 electron charge packets for surface channel
- CTE limited by surface interface traps
- CTE is reduced to 98% if holes are accumulated between storage electrodes.

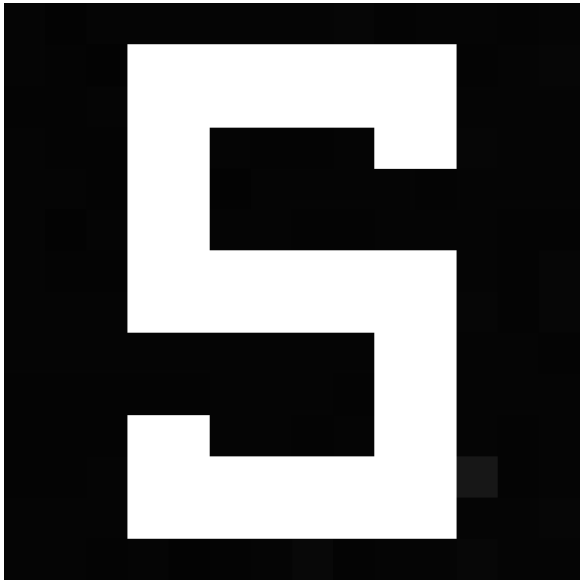


Measured Pixel Characteristics

Well capacity	3500 e-
Conversion gain	165 μV/e-
Sensitivity at 550 nm	0.15V/lux-sec
QE at 450, 550, 650 nm	20, 48, 65 %
Pixel read noise	5 e- rms (1mV)
Dark current at RT	33 e-/sec (5.5 mV/sec)
DSNU	35 % rms
PRNU	2 % rms
Peak SNR	35 dB
Dynamic range	57 dB

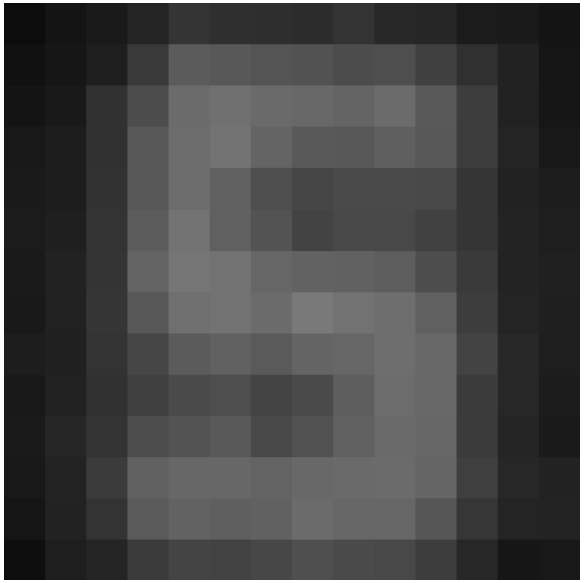
Images from Single Subarray

Electrical



3000 electron charge packets from fill/spill input

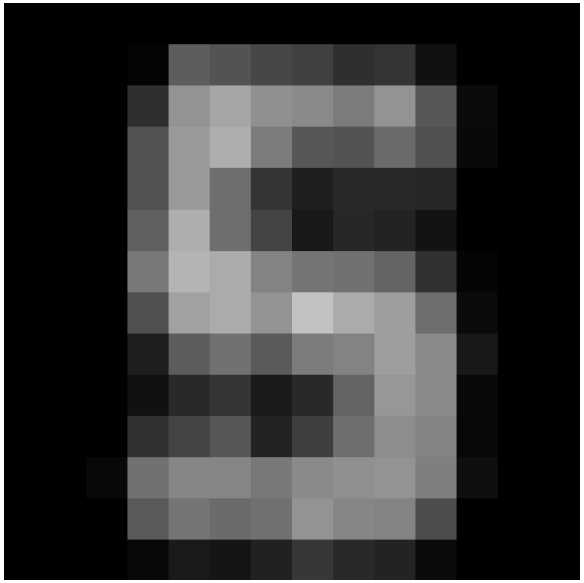
Optical



Raw data

Captured with F/2.8, f=6mm lens at 1/10 sec

Optical



Added contrast

Processed Multi-Aperture Image

Summary

- Developed FT-CCD structures in deep submicron CMOS
  - Ripple charge transfer
  - Transfer to H-CCD
  - Surface mode, buried-channel, and pinned phase
- Many potential applications or benefits
  - Depth
  - Close proximity imaging
  - Color imaging with good spectral separation
  - High defect tolerance
  - Relaxed external optical requirements
- Future work of interest
  - Integration of micro optics
  - Algorithms for data extraction and image formation
  - Improvements to the pixels and sensor architecture

Acknowledgement

- Hertz Foundation
  - Fellowship support
- TSMC
  - C.H. Tseng, David Yen, C.Y. Ko, J.C. Liu, Ming Li, and S.G. Wuu for process customization and fabrication
- Lane Brooks, MIT EECS
  - Collaboration on the design of the testing platform and software system