

# A 3MPixel Multi-Aperture Image Sensor with $0.7\mu\text{m}$ Pixels in $0.11\mu\text{m}$ CMOS

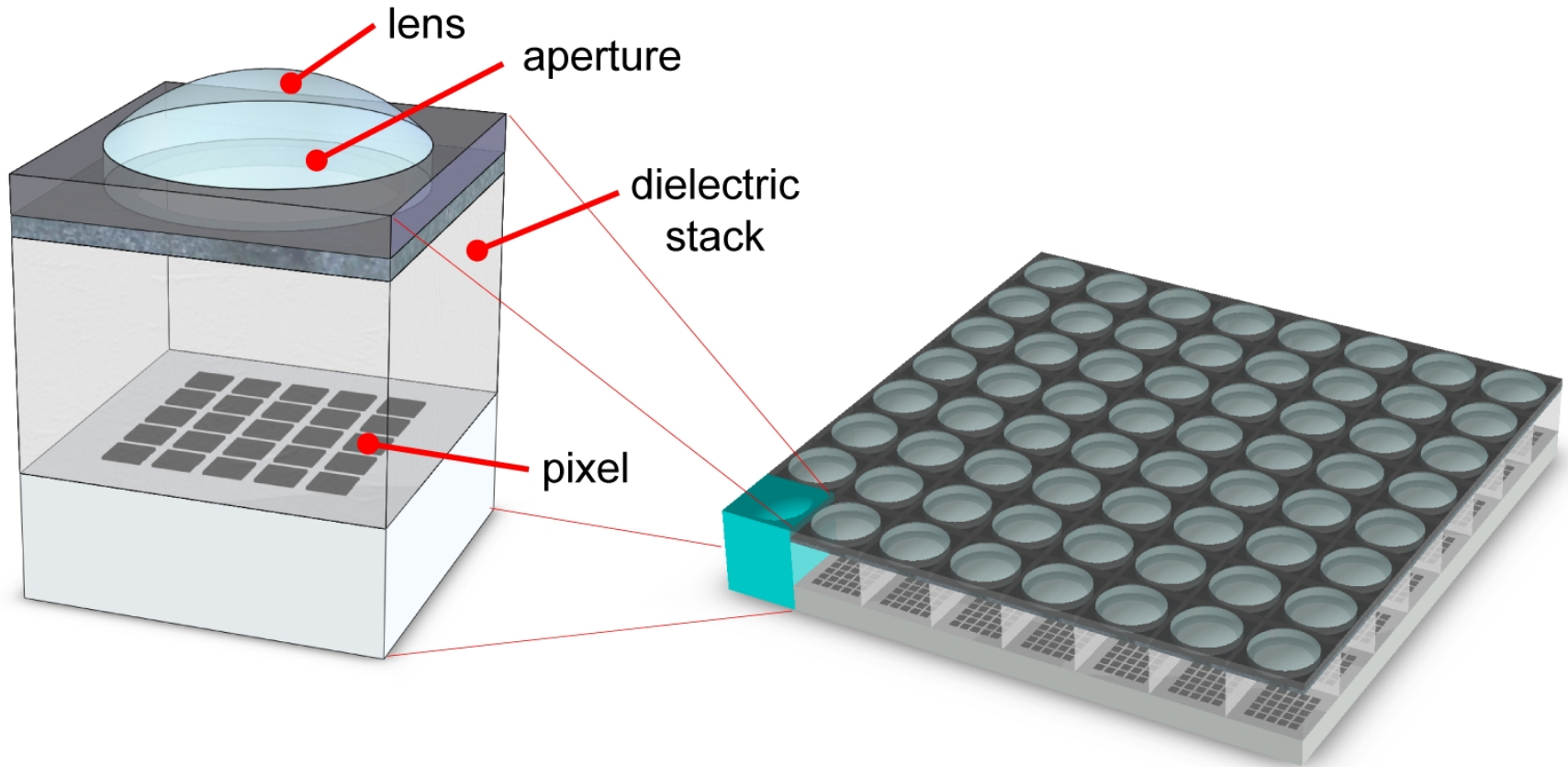
Keith Fife, Abbas El Gamal, H.-S. Philip Wong

Stanford University, Stanford, CA

# Outline

- Introduction
- Chip Architecture
- Detailed Operation
  - FT-CCD array
  - Multi-Aperture array
  - Column ADC
- Results
- Summary

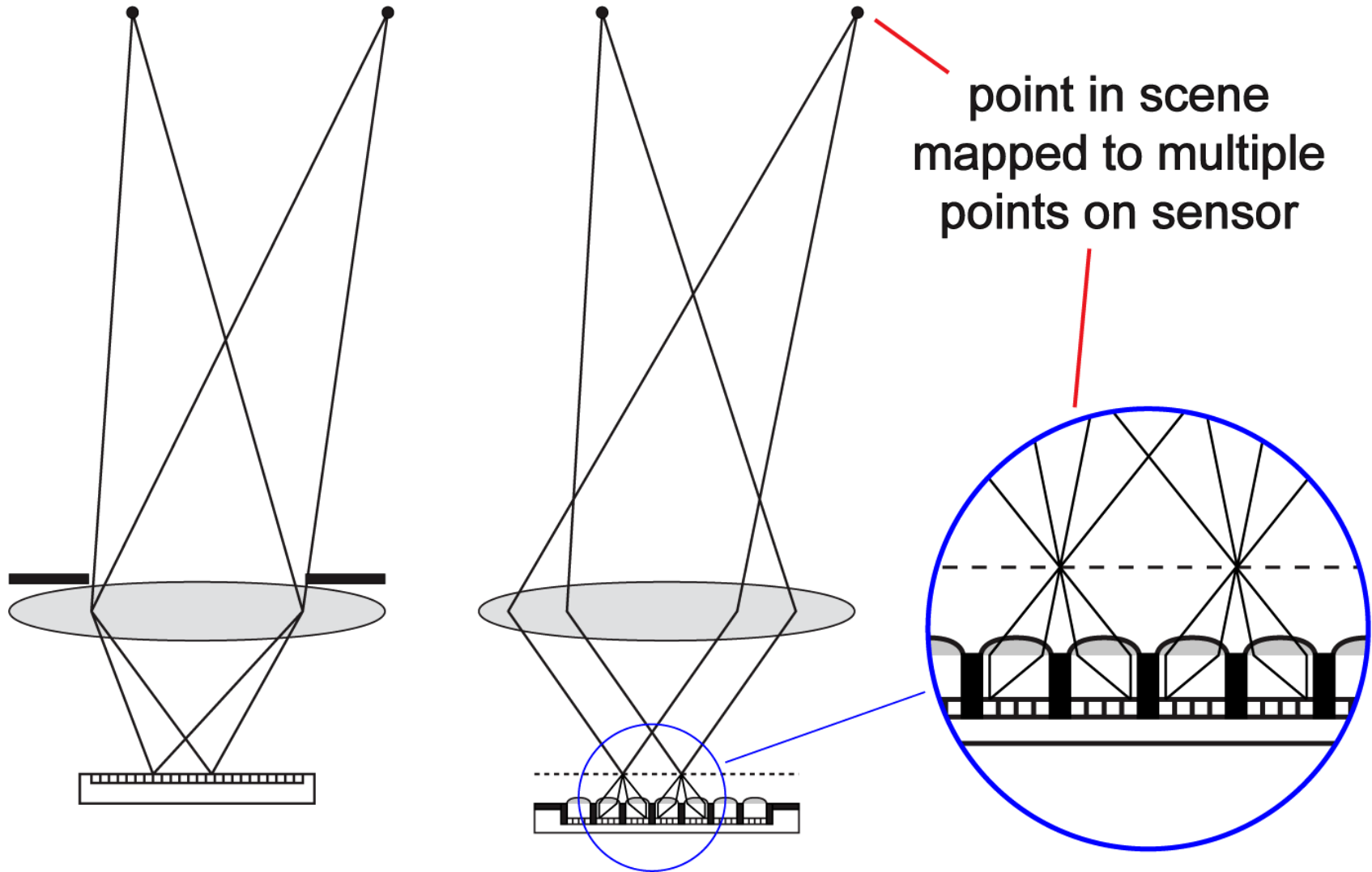
# Multi-Aperture Image Sensor



# Imager sub-array with integrated optics

## Imager sub-arrays integrated to form multi-aperture array

# Conventional vs. Multi-Aperture



Conventional imaging

Multi-aperture imaging



# Multi-Aperture Imaging



Image in focal Plane

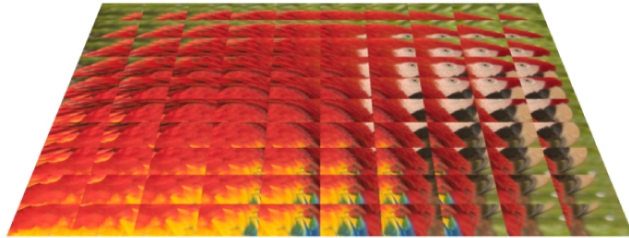
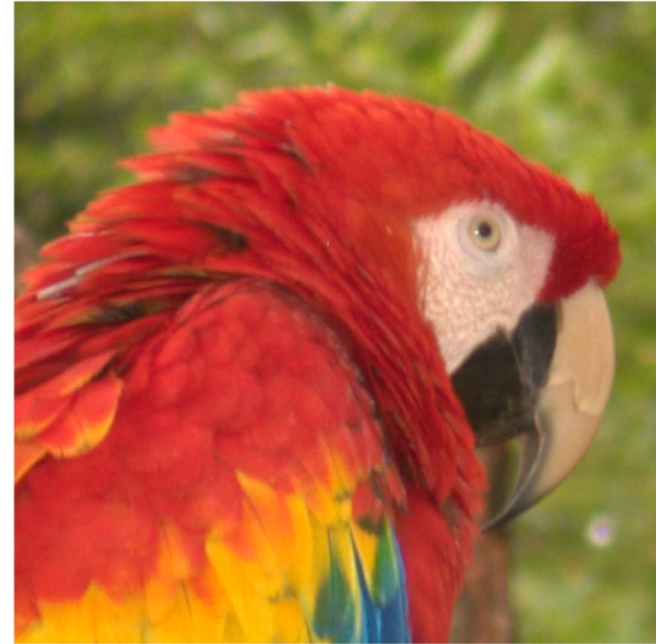
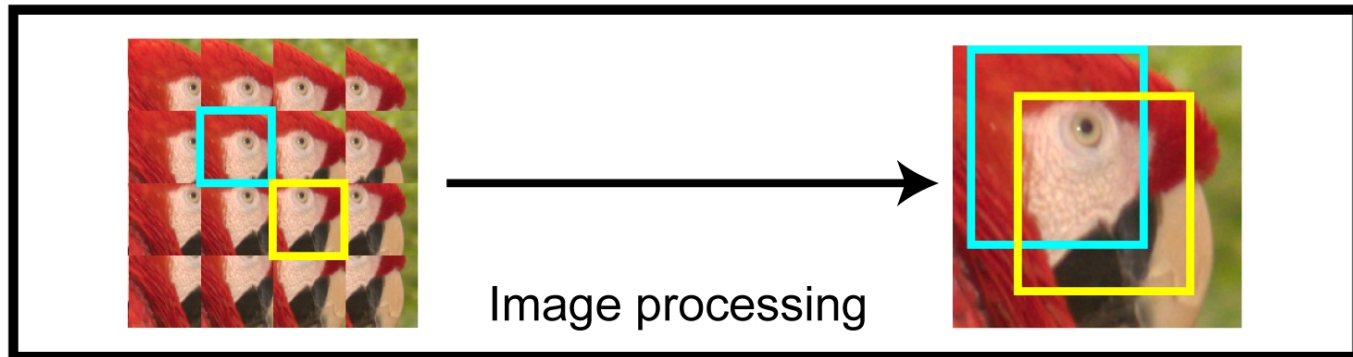


Image captured at MA-imager



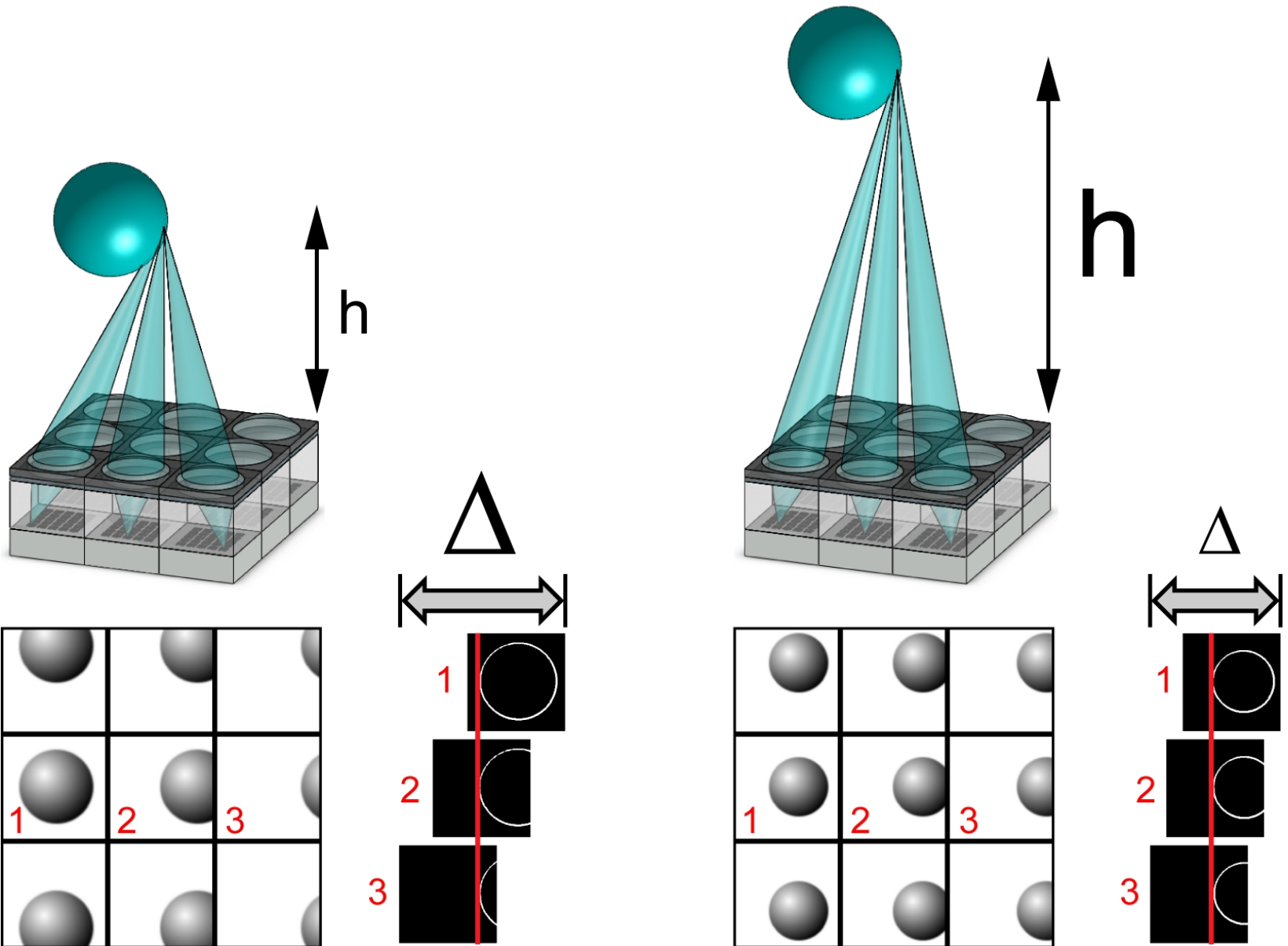
Final reconstructed image



# Benefits of Multi-Aperture Imaging

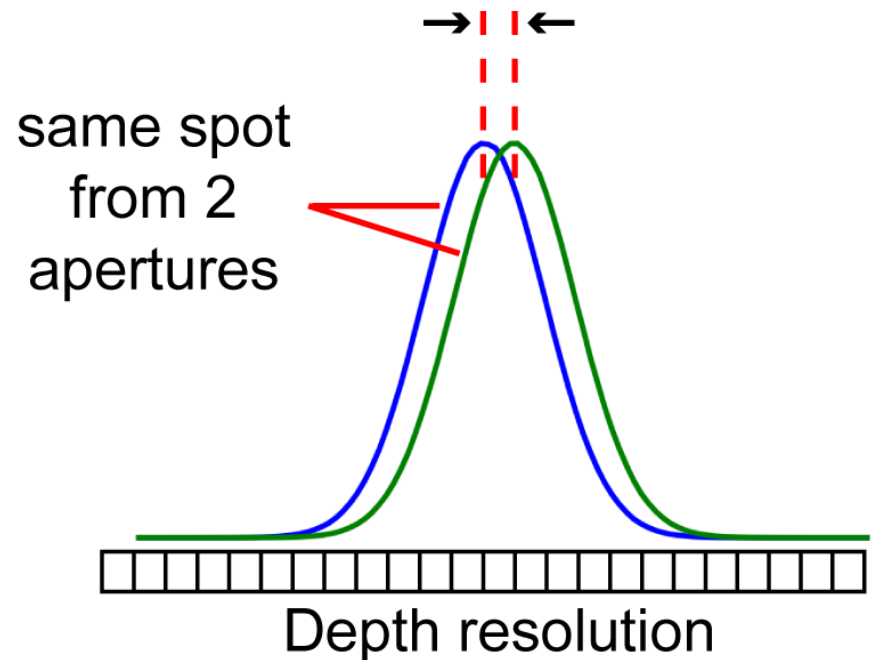
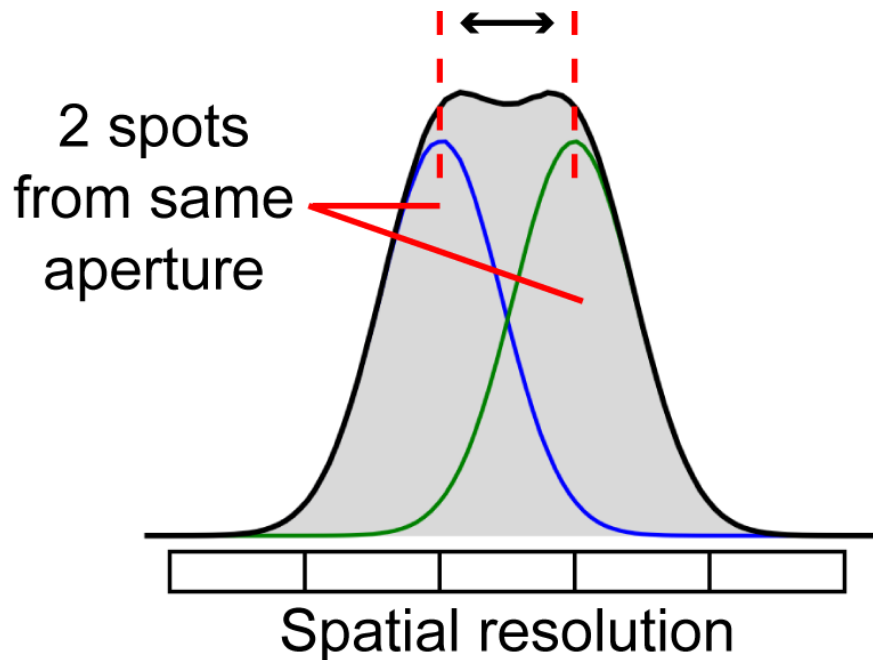
- Capture depth information
- Close proximity imaging
- Achieve better color separation
- Reduce requirements of objective lens
- Increase tolerance to defective pixels

# Depth from Multi-Aperture

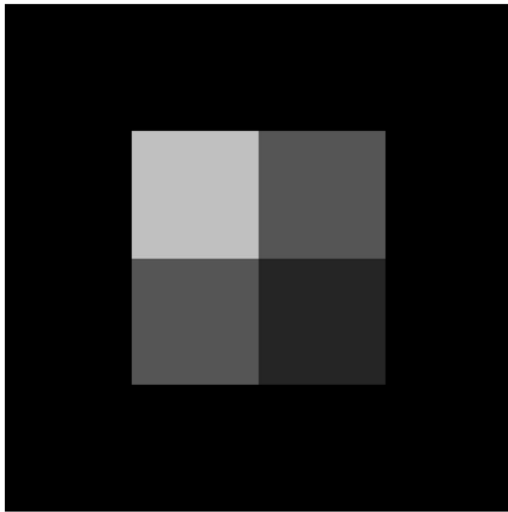
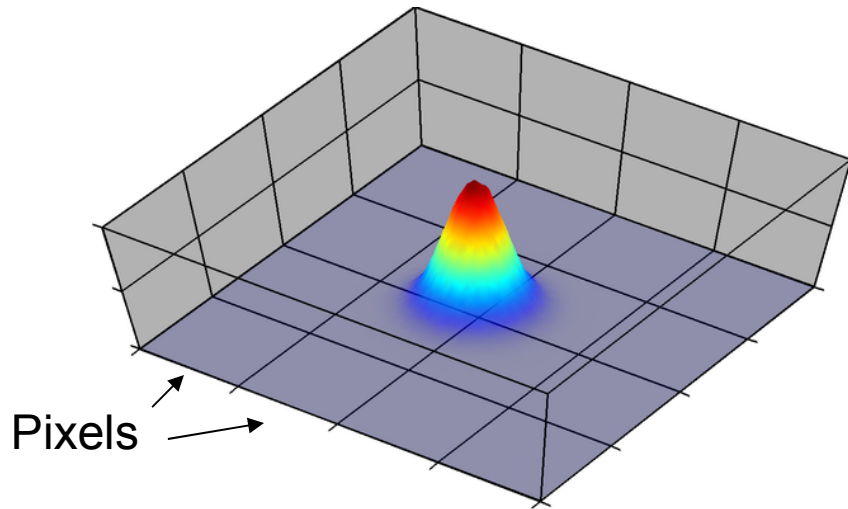


# Why Use Small Pixels?

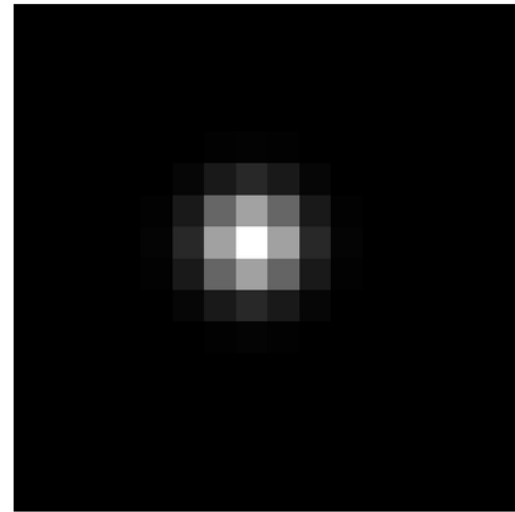
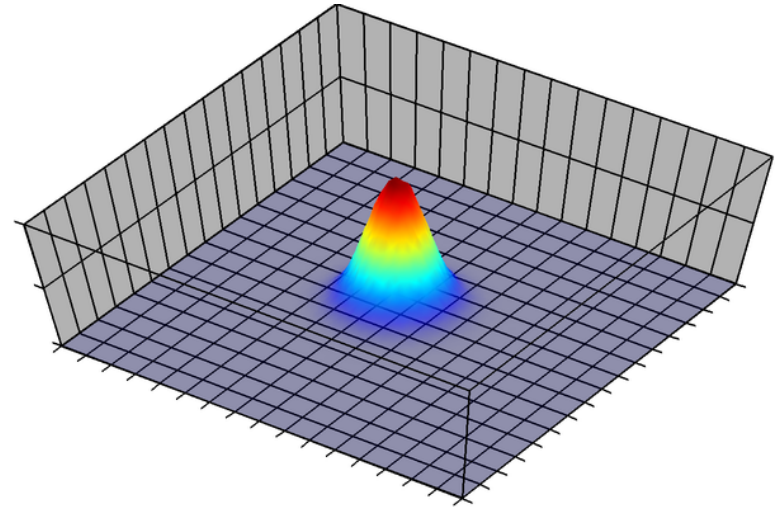
- Depth resolution improves with pixels smaller than the spot size
- Spatial resolution is limited by the spot size
- Depth resolution is limited by accuracy in localization of the spot



# Feature Localization vs. Pixel Size

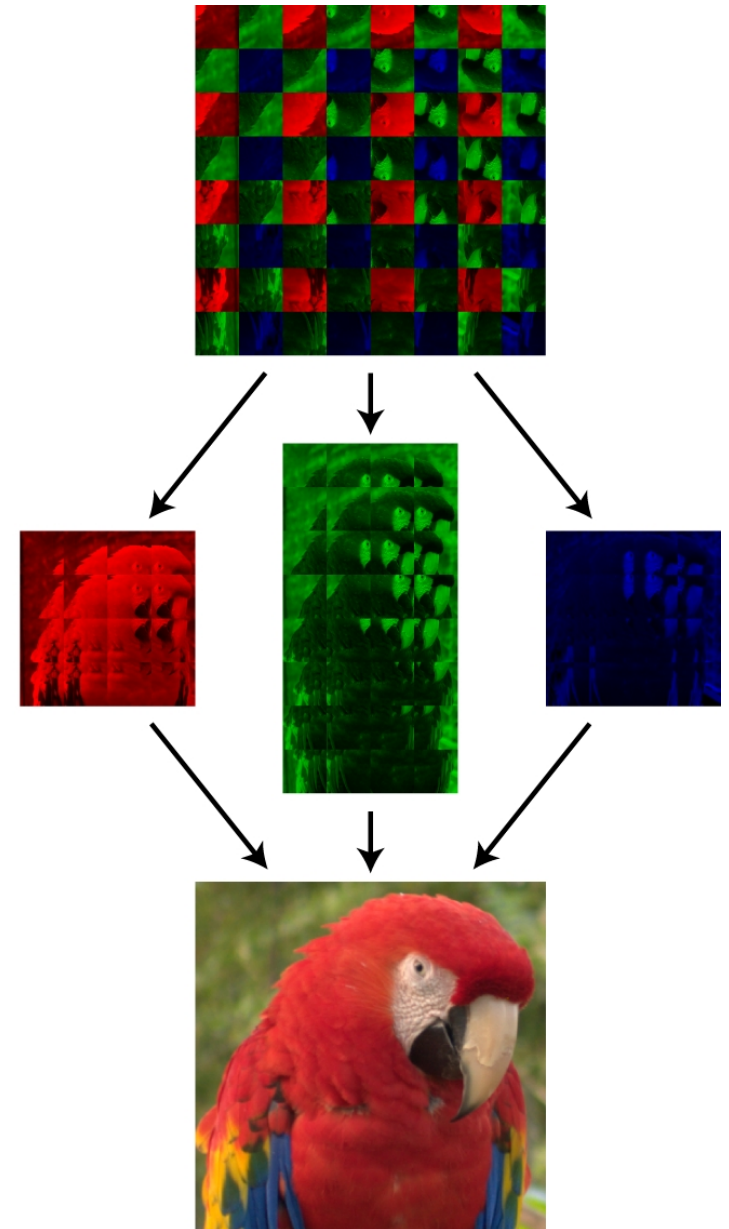
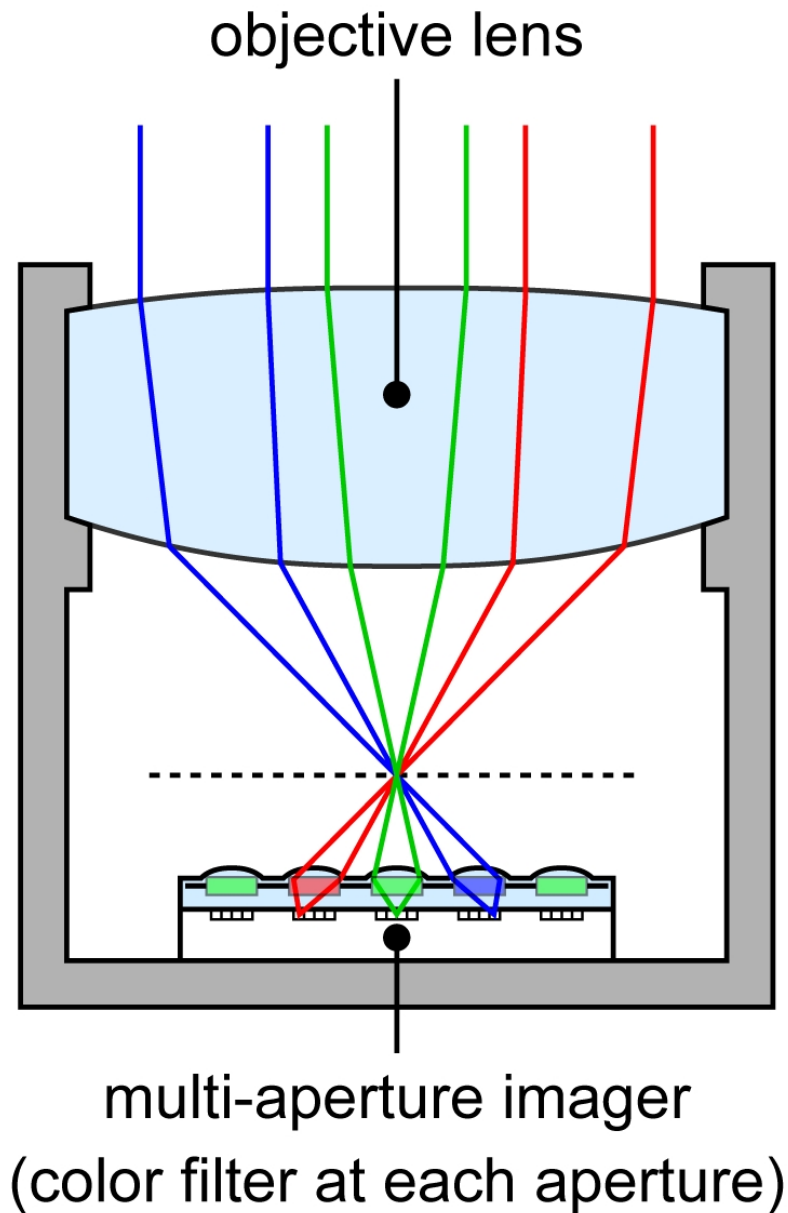


Poor location accuracy



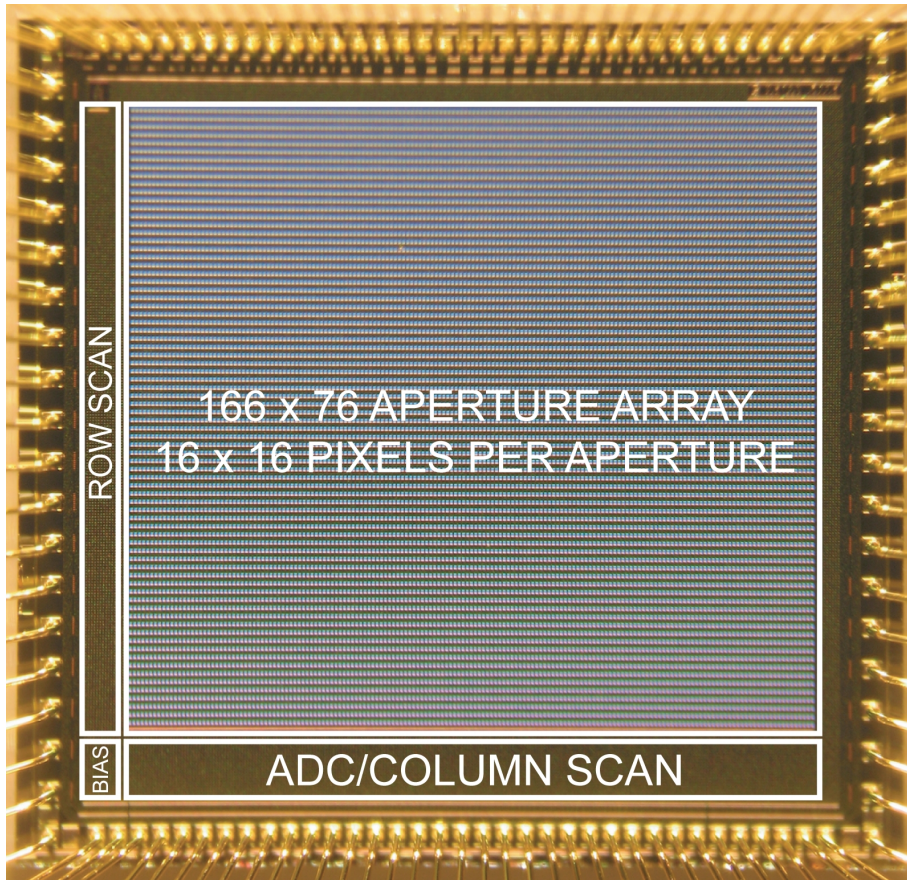
High location accuracy

# Color with Multi-Aperture





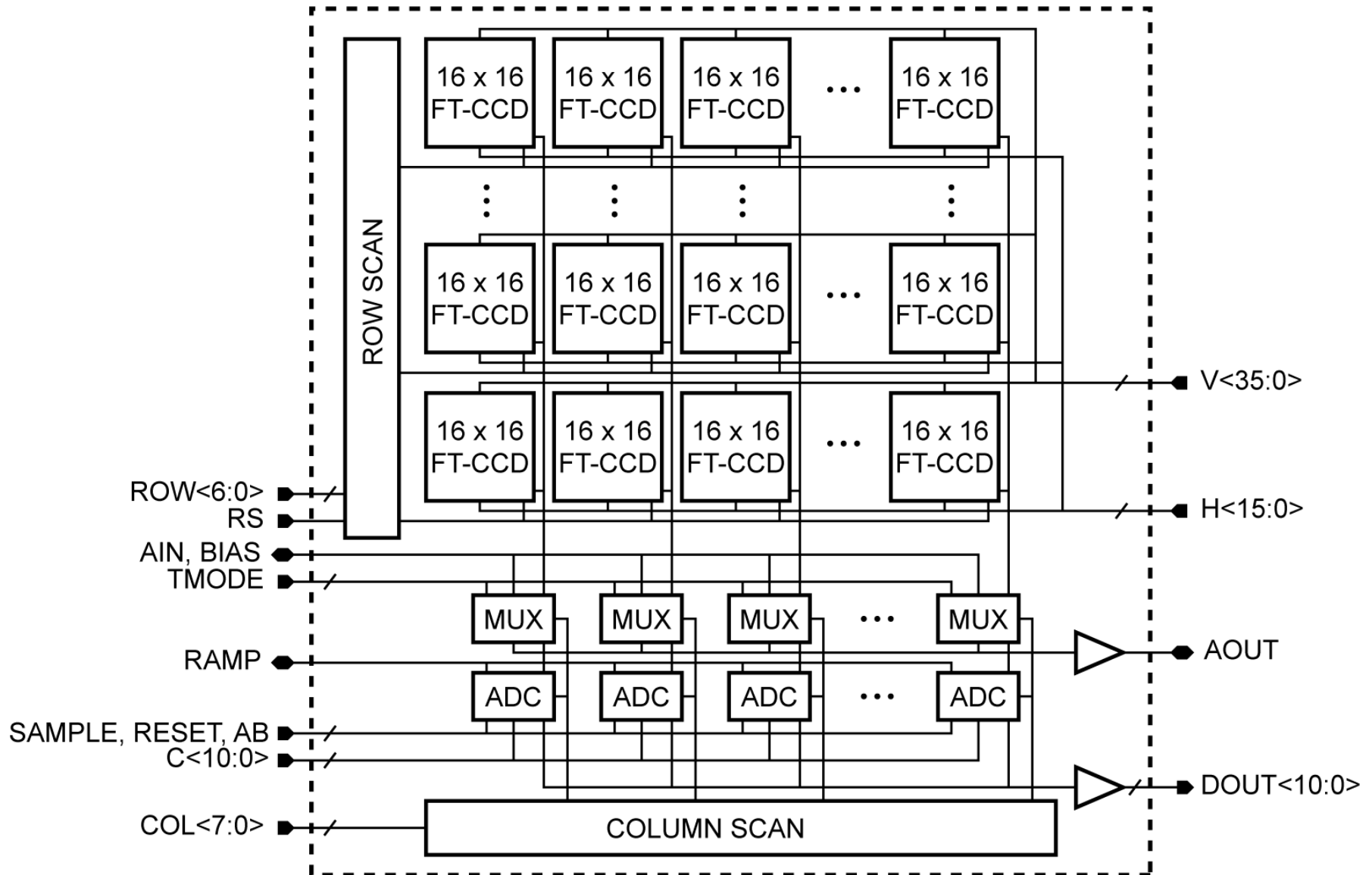
# Fabricated Multi-Aperture Imager



- 0.11 $\mu\text{m}$  CMOS (TSMC)
- Chip size: 3.0 x 2.9mm<sup>2</sup>
- 166 x 76 aperture array
- 16 x 16 pixel FT-CCD per aperture
- Pixel size: 0.7  $\mu\text{m}$
- Max frame rate: 15fps
- ADC resolution: 10 bit
- Power: 10.45mW

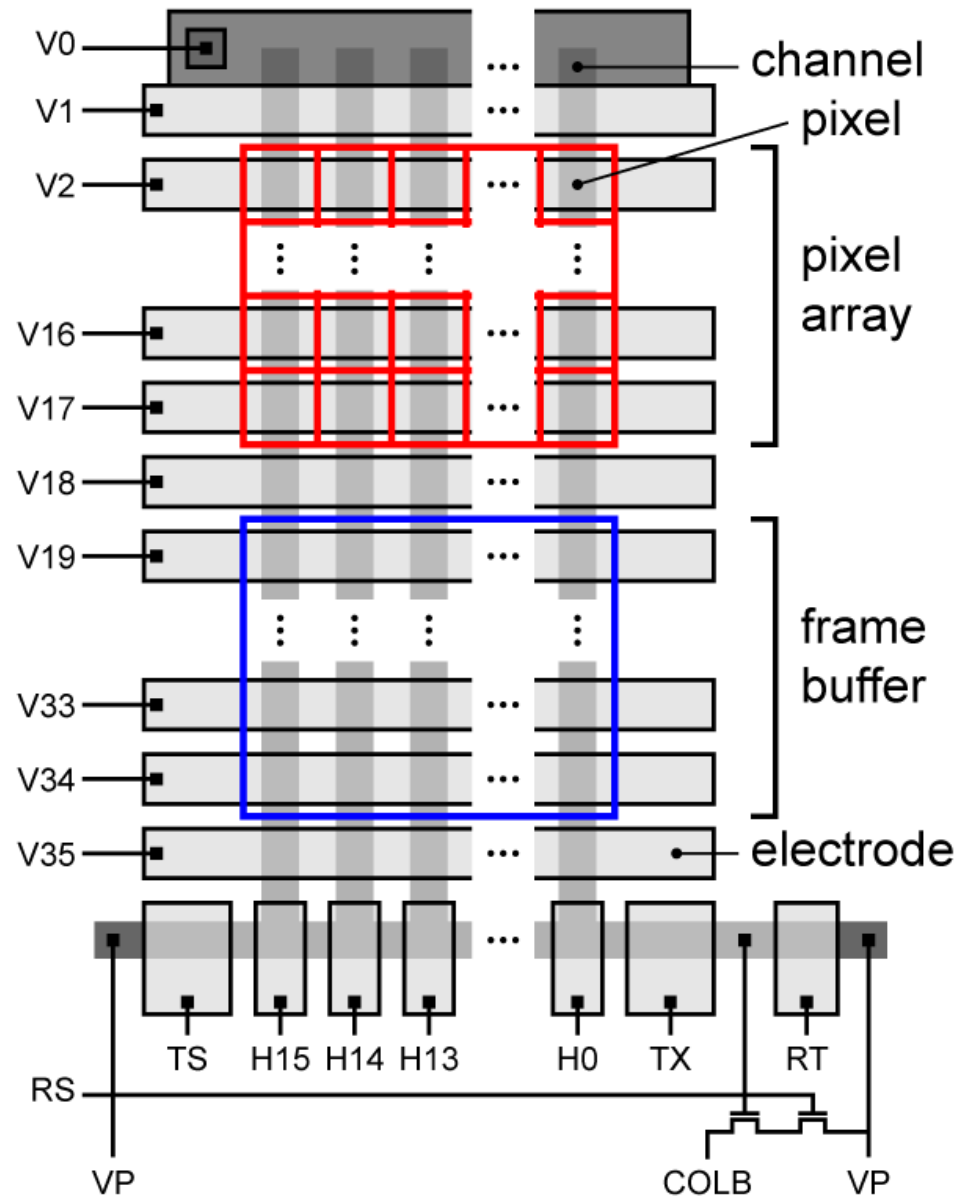
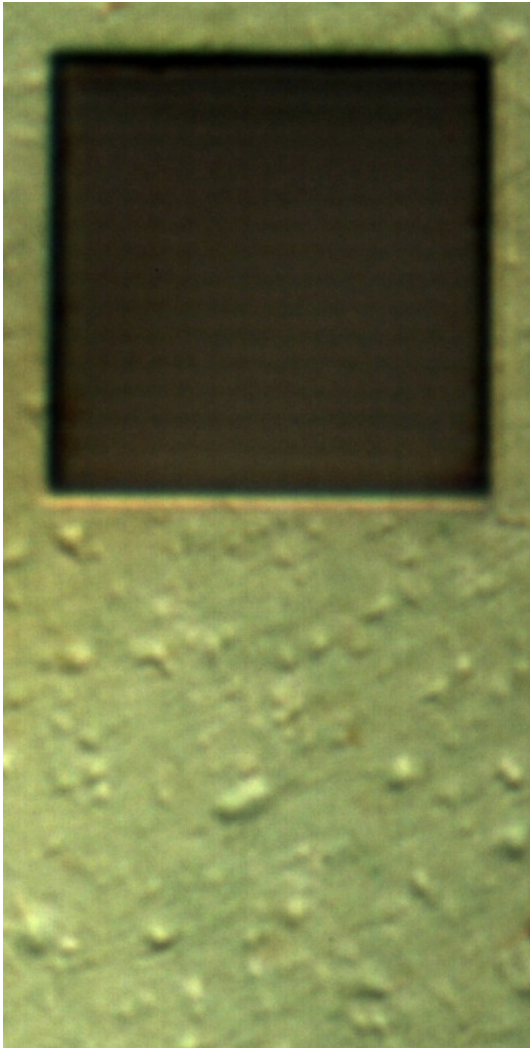
\* Local optics are not integrated on this chip.

# Block Diagram of Fabricated Chip



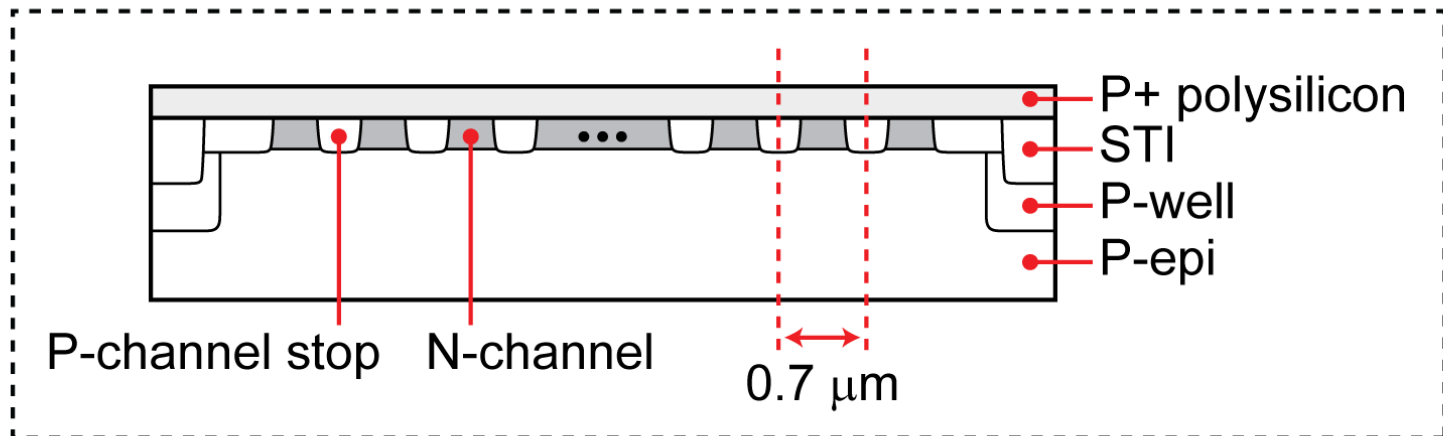
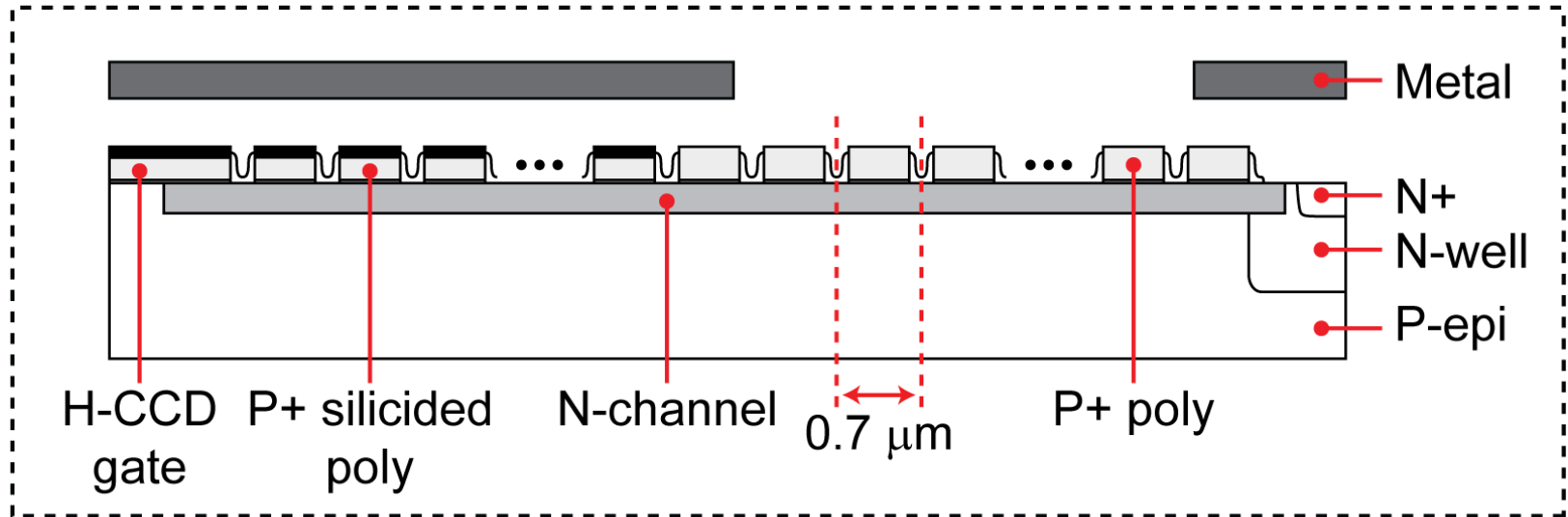


# 16 x 16 FT-CCD schematic



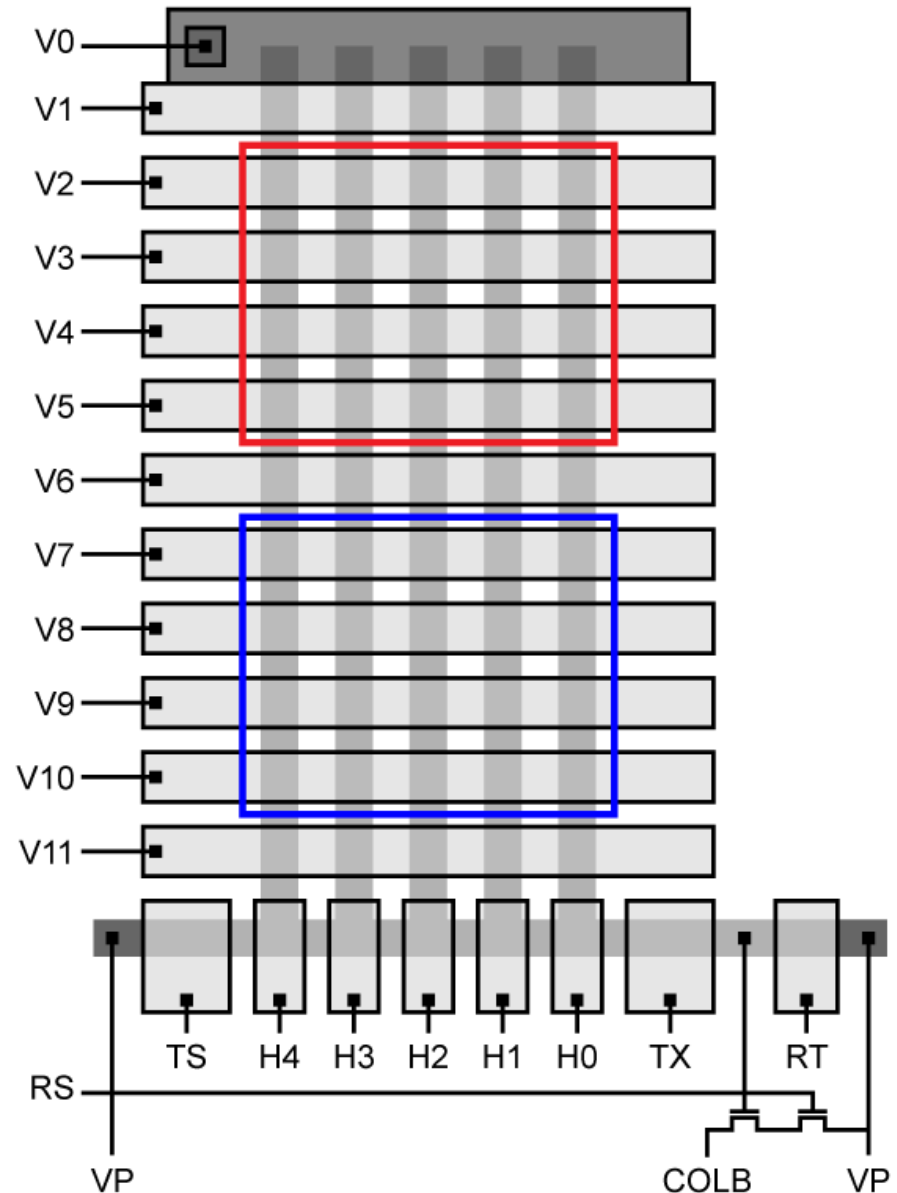
\* K. Fife, A. El Gamal and H.-S. P. Wong,  
IEDM 2007, p1003-1006

# CCD Cross Sections

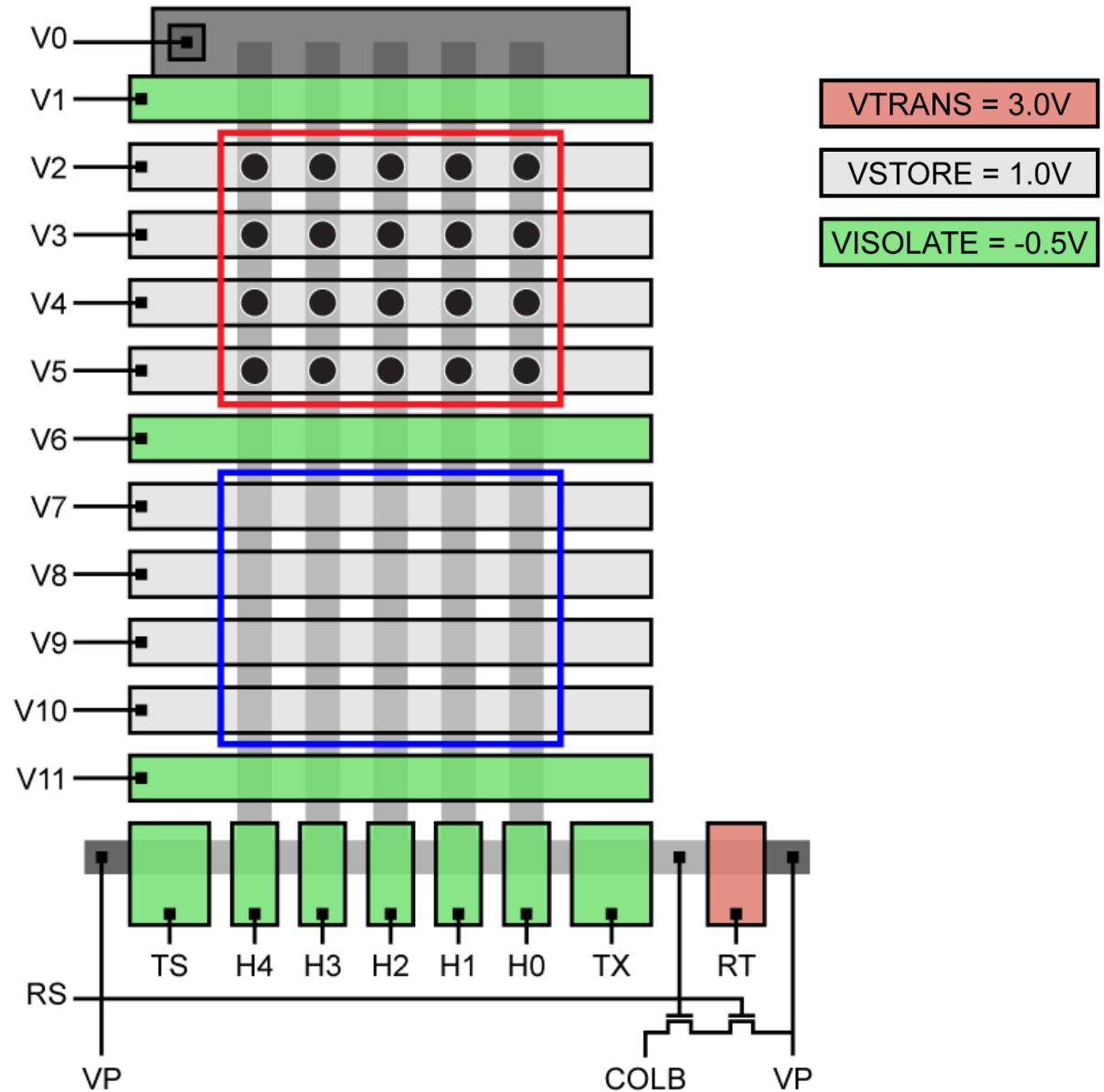


# Operation

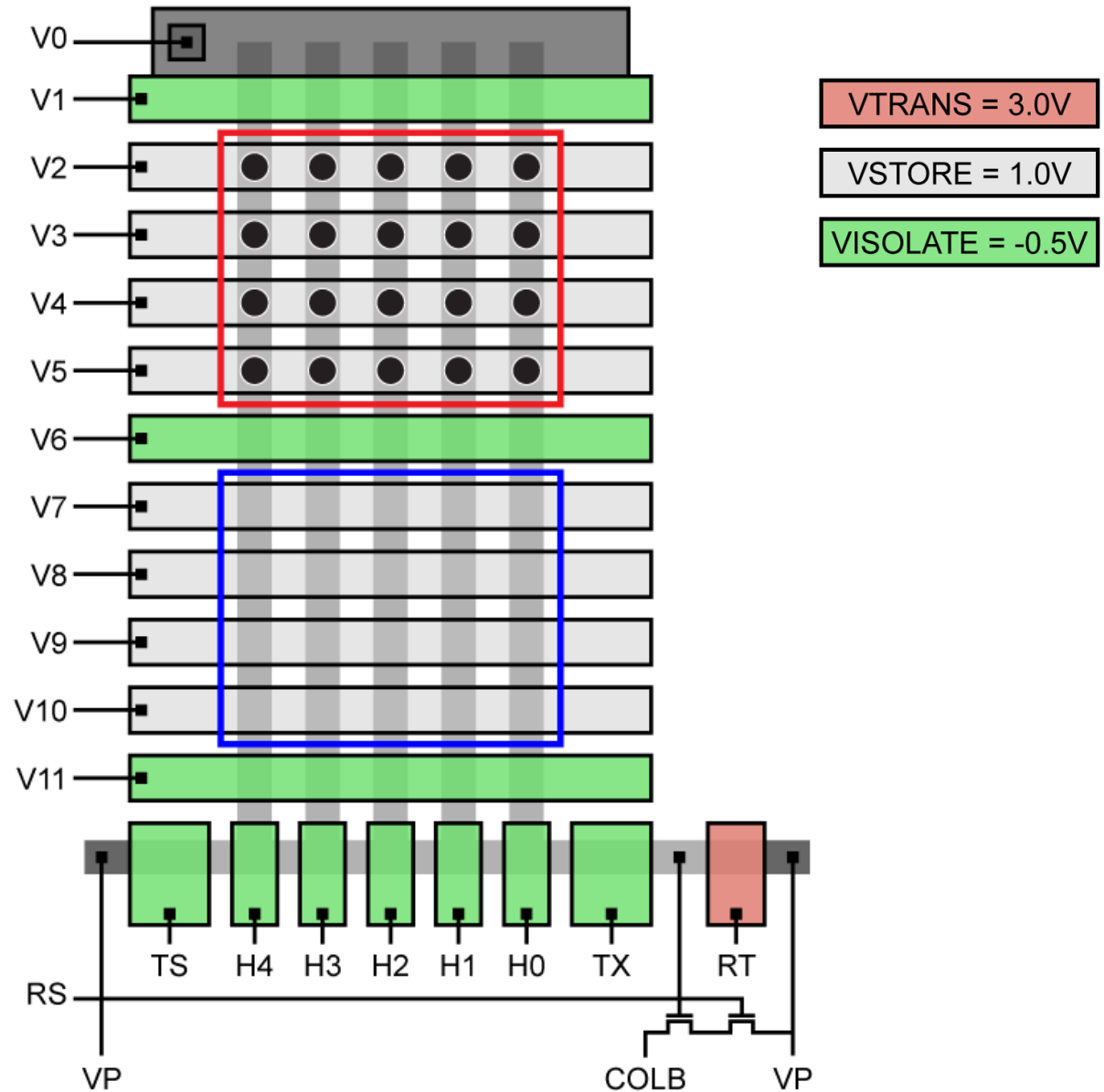
- Flush
- Integrate
- Frame Transfer
- Horizontal Readout



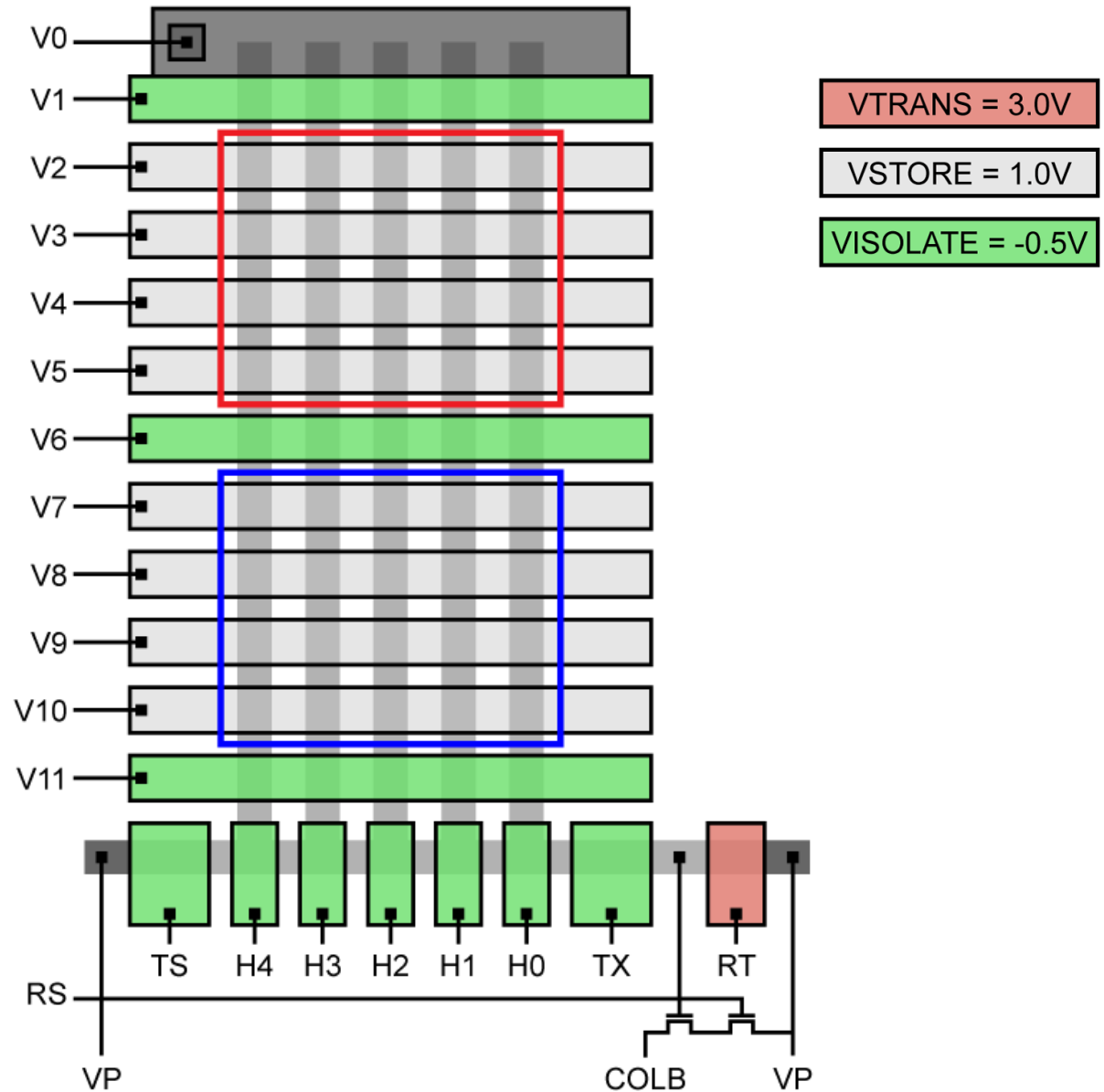
# Operation (Flush)



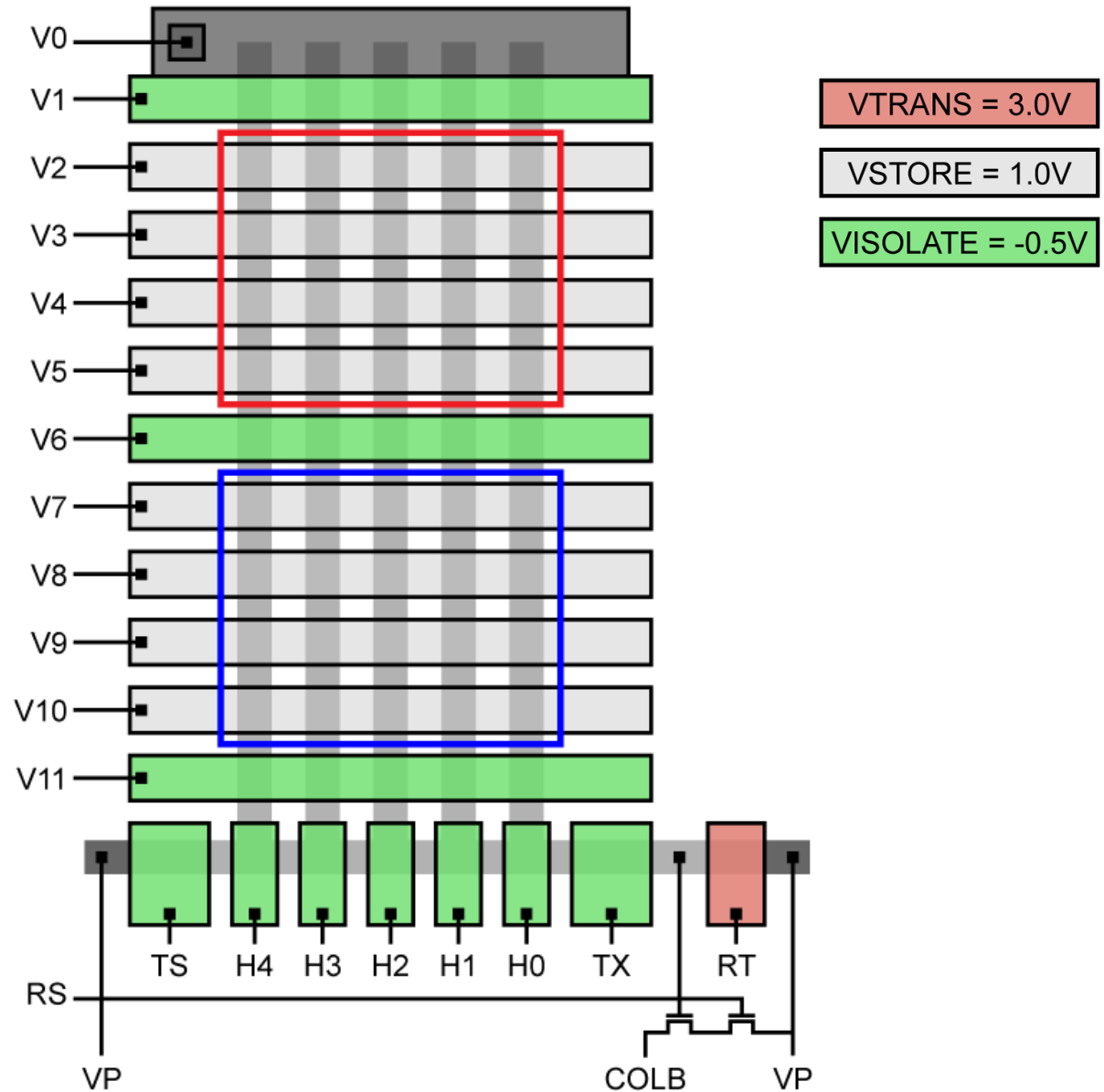
# Operation (Flush)



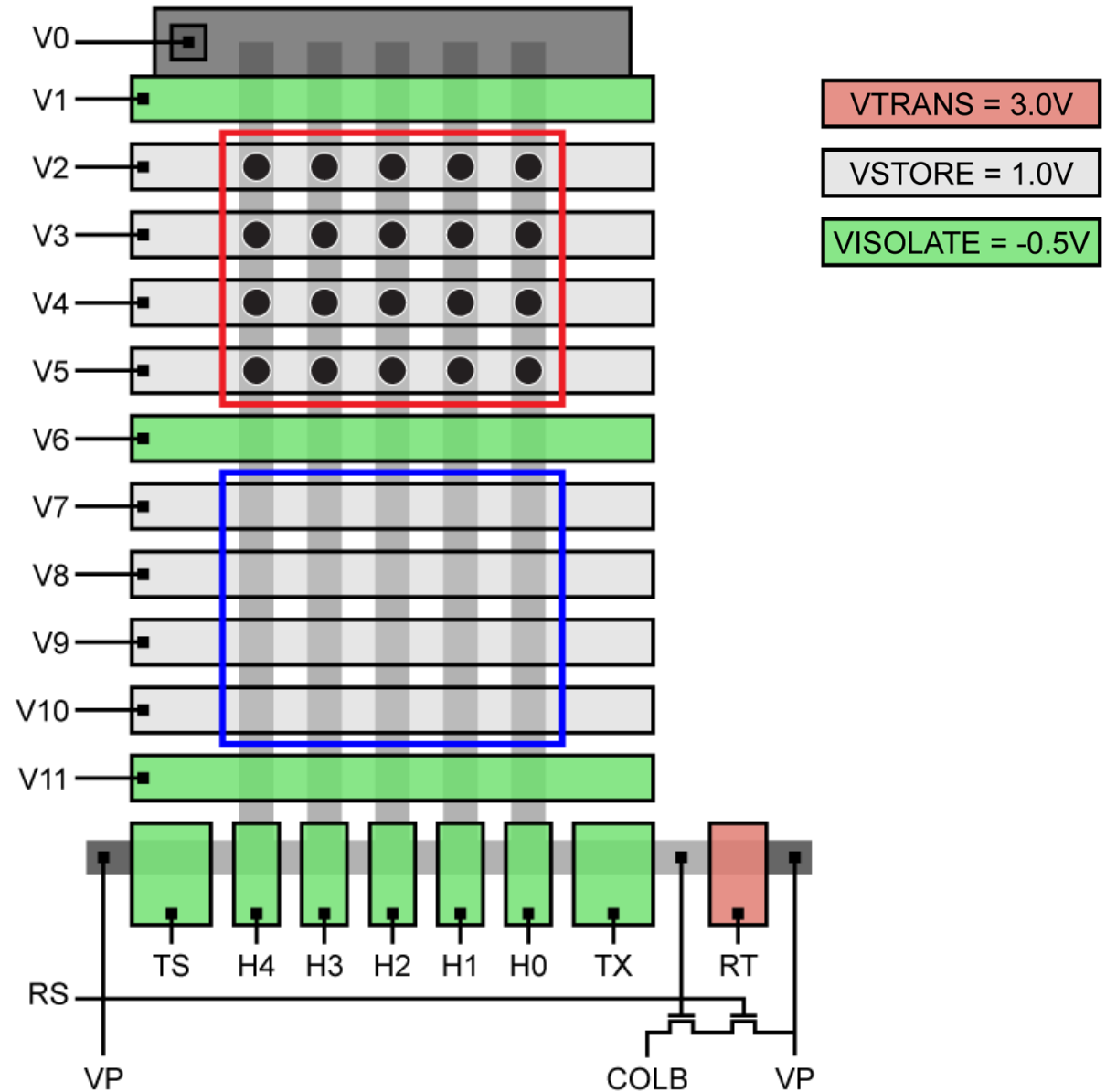
# Operation (Integrate)



# Operation (Integrate)

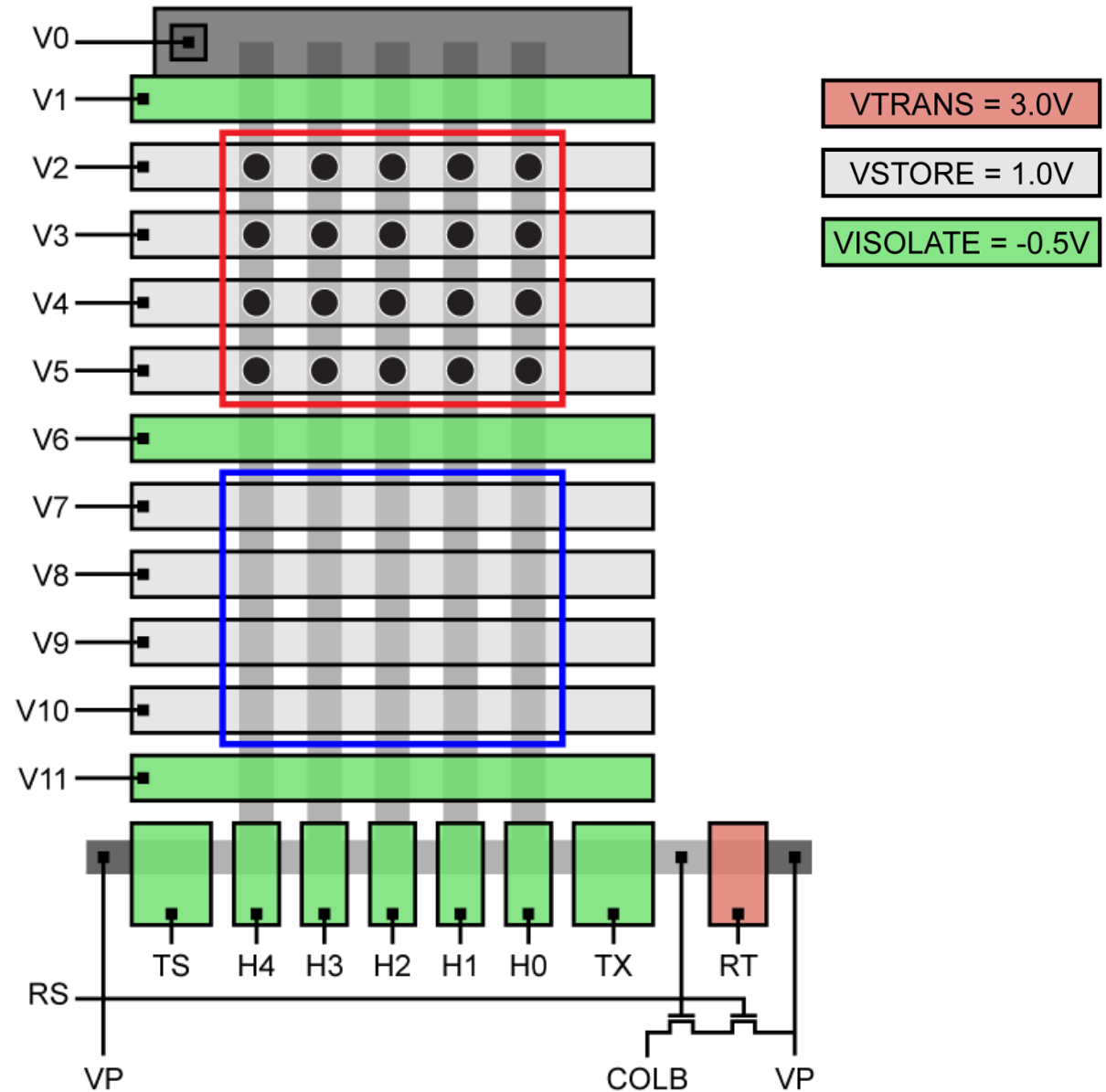


# Operation (Frame Transfer)

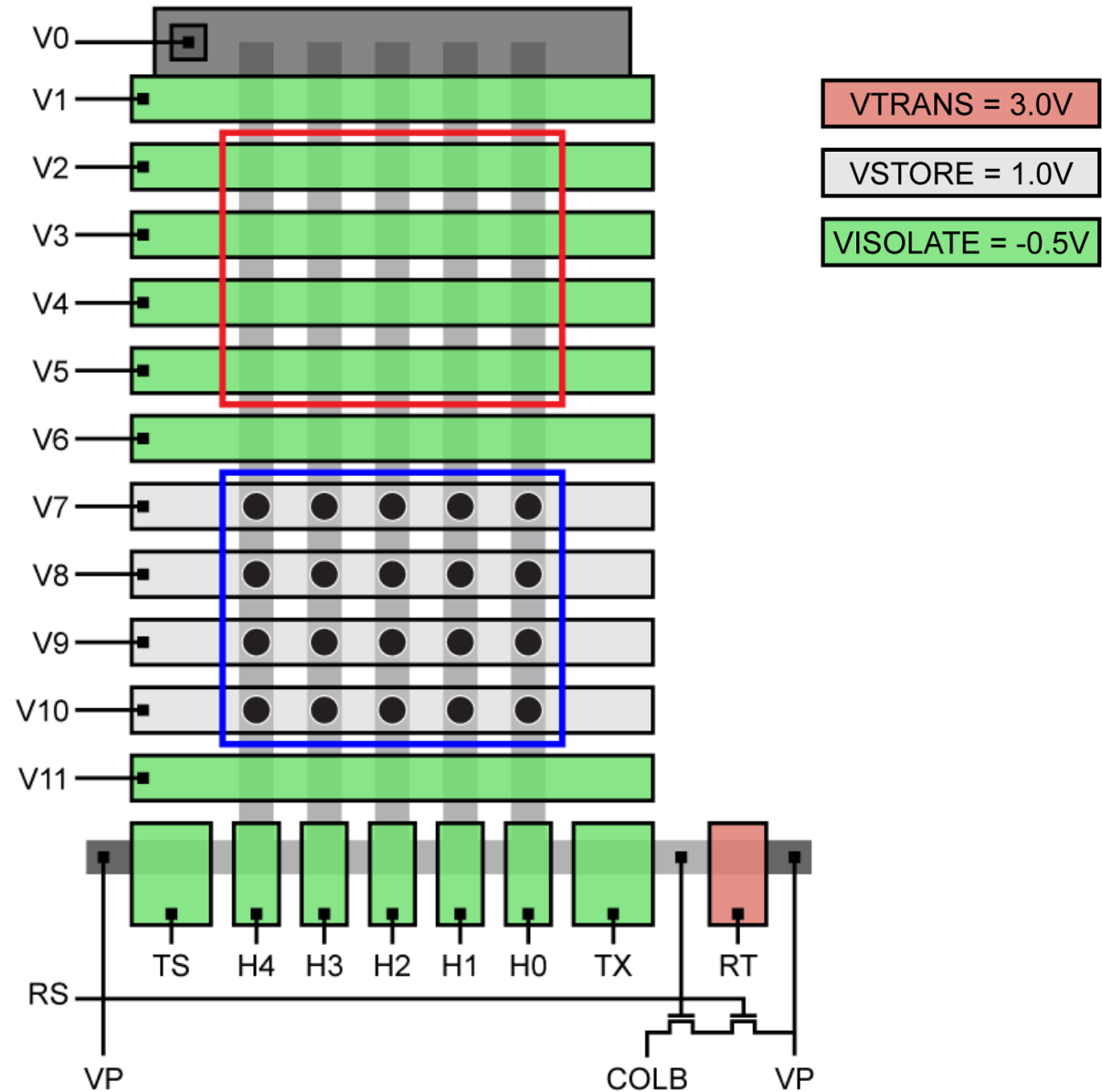




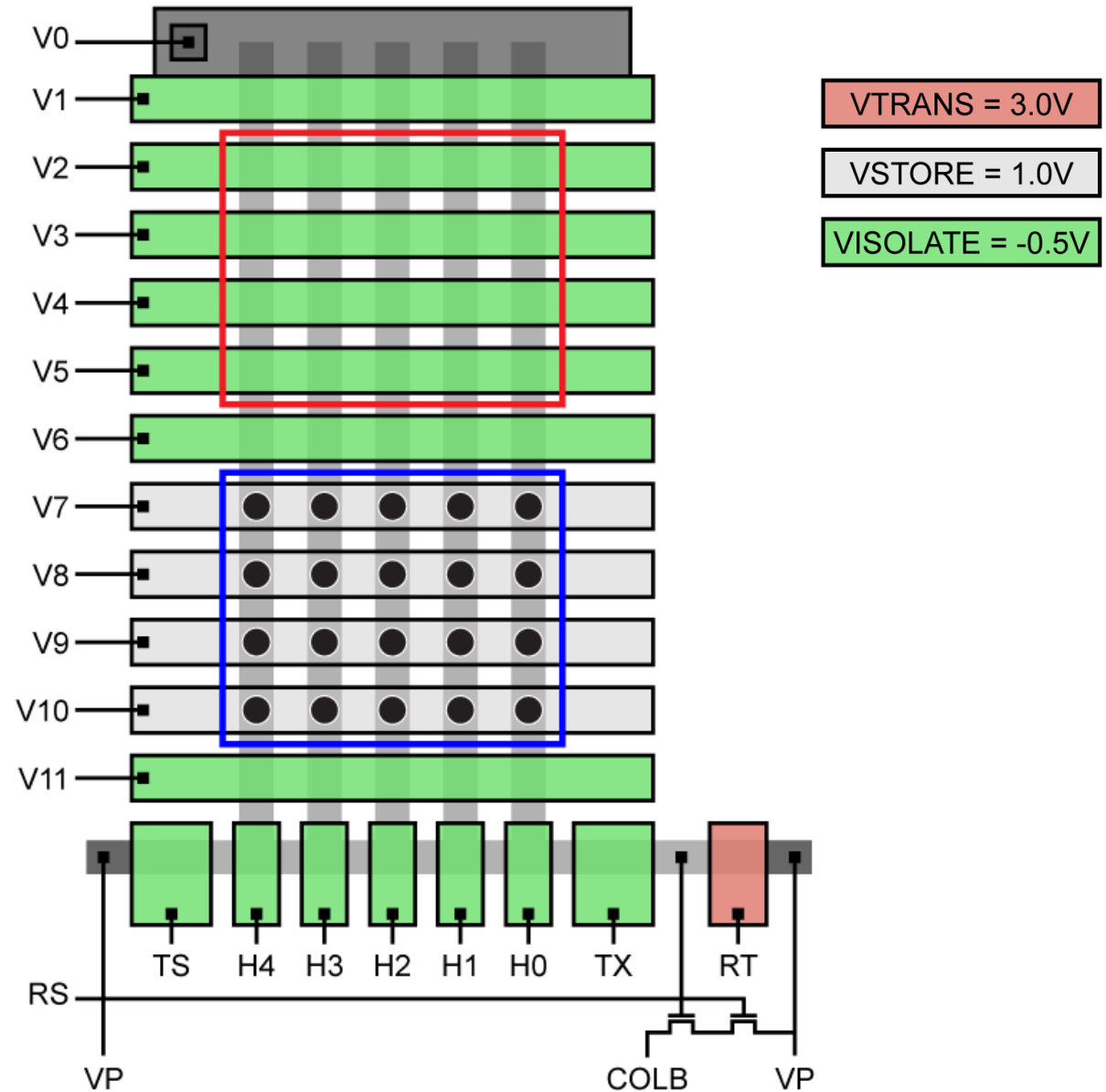
# Operation (Frame Transfer)



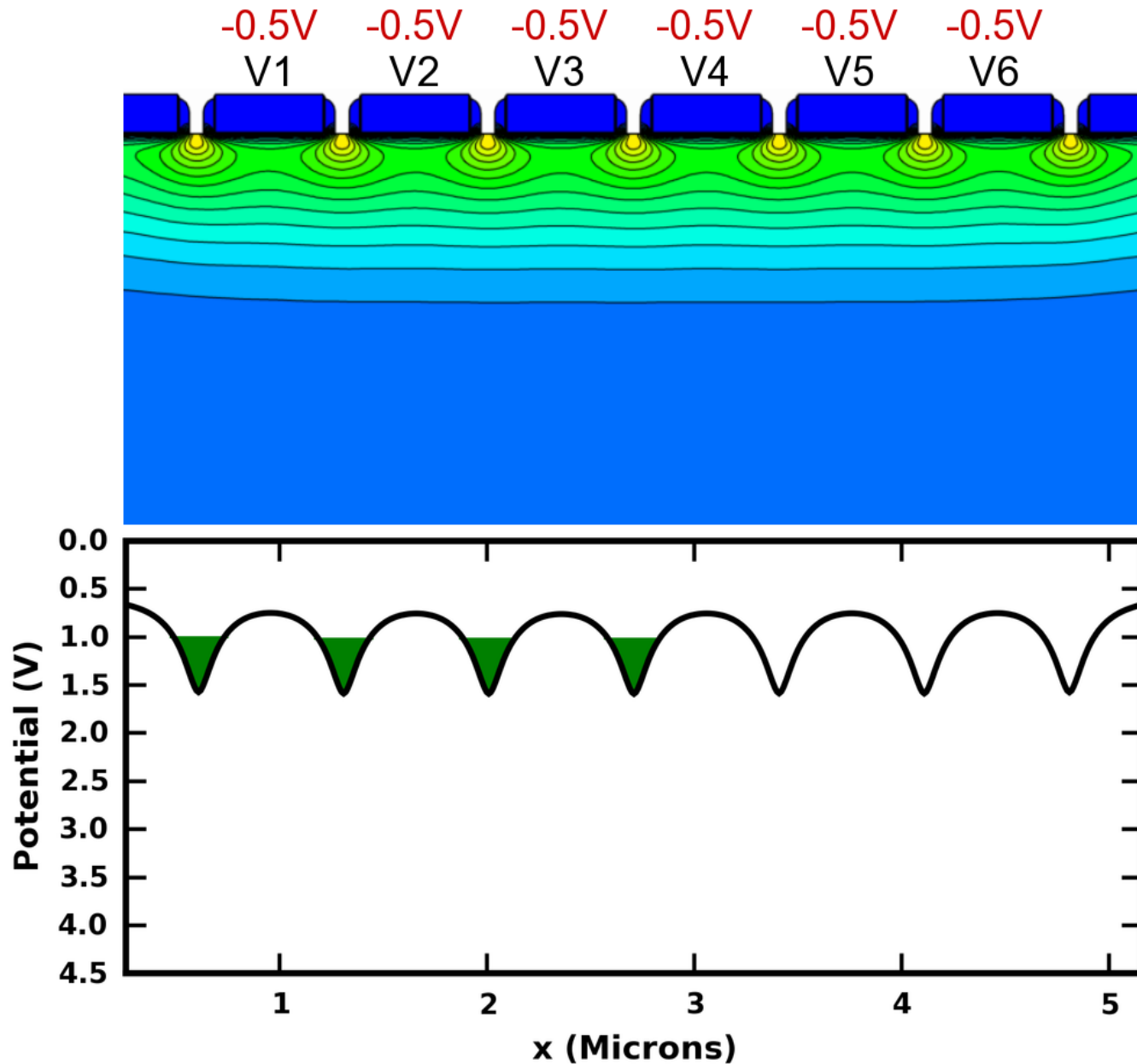
# Operation (Horizontal Transfer)



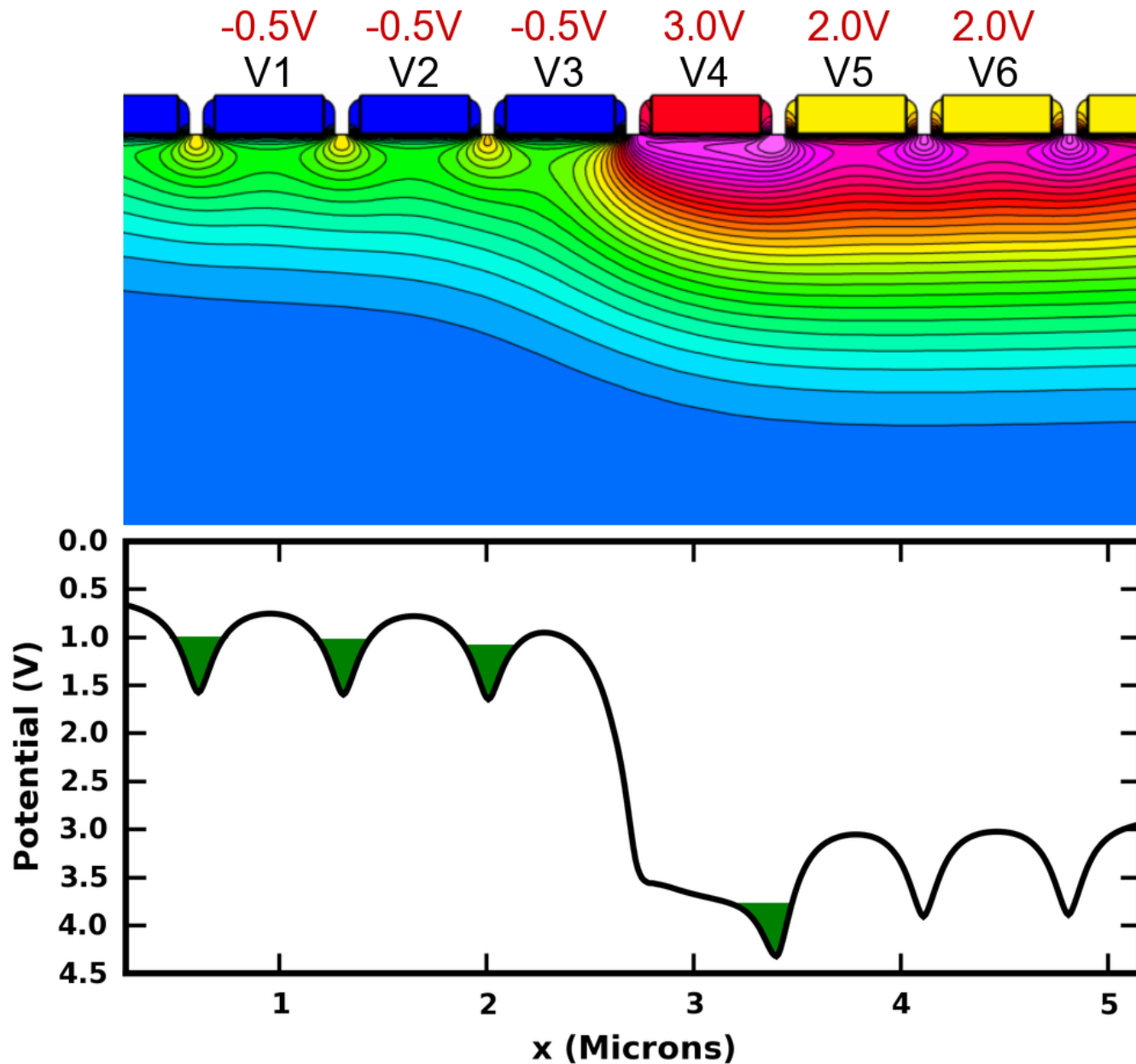
# Operation (Horizontal Transfer)



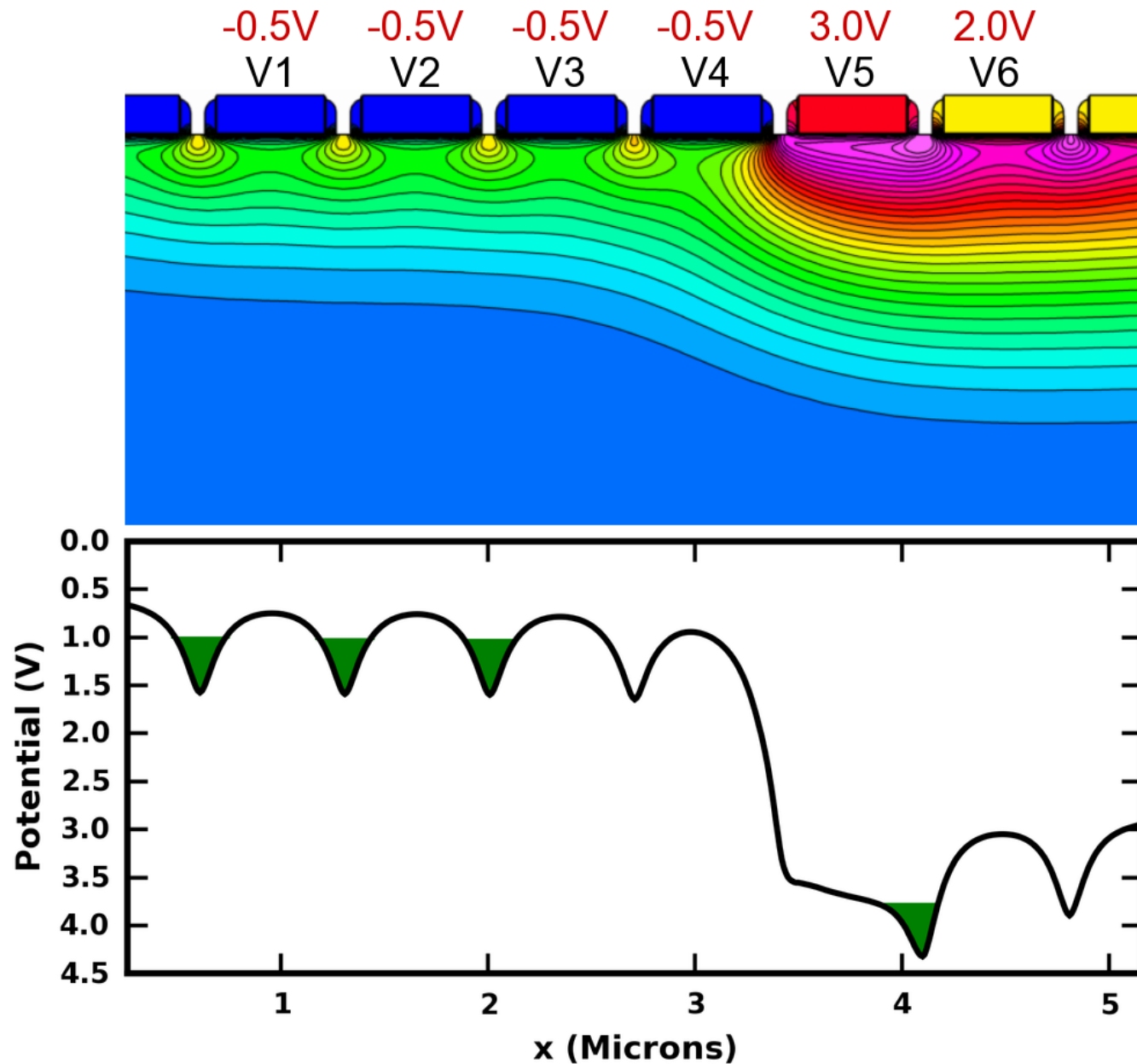
# Potential Profile Along Channel



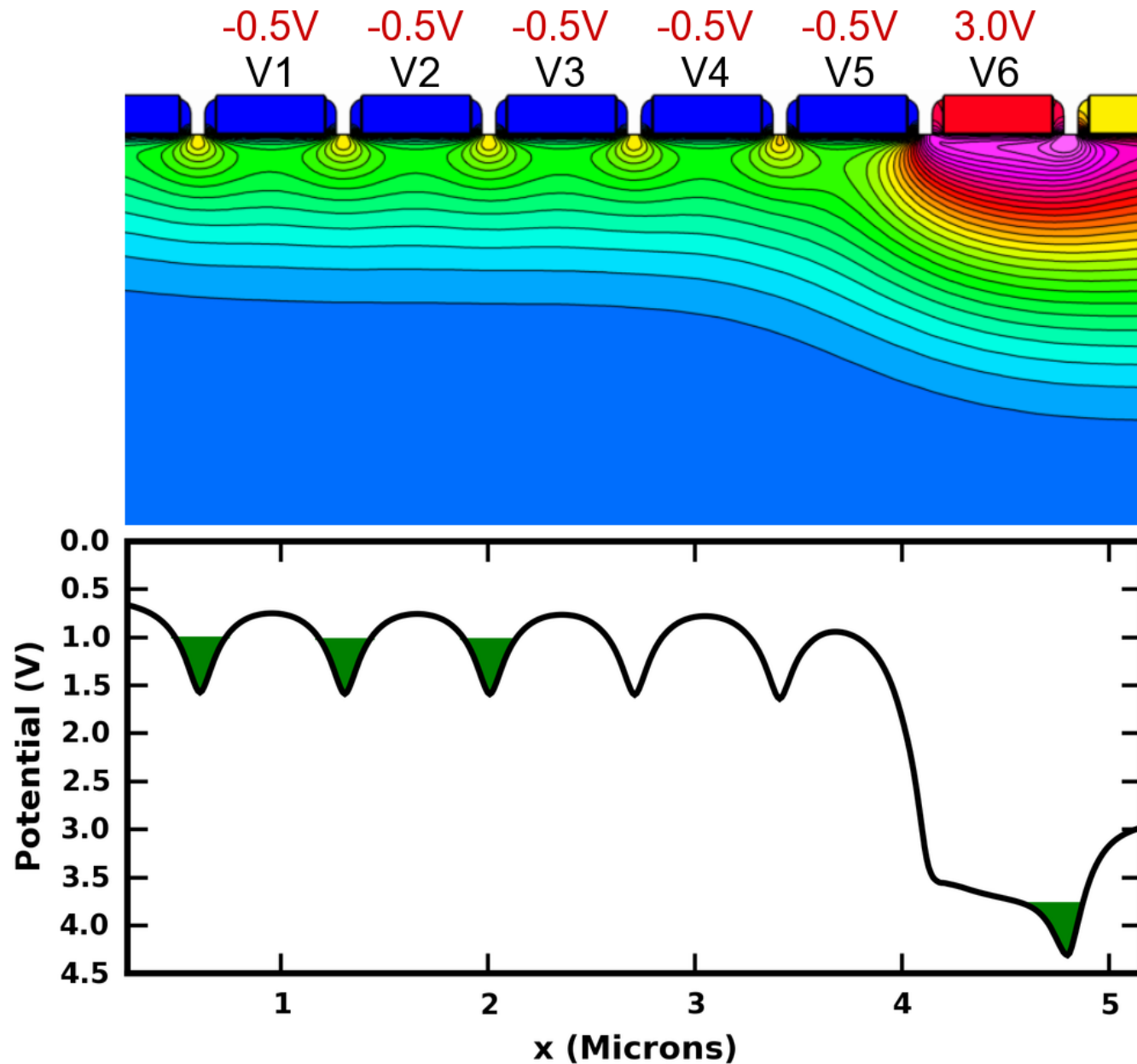
# Potential Profile Along Channel



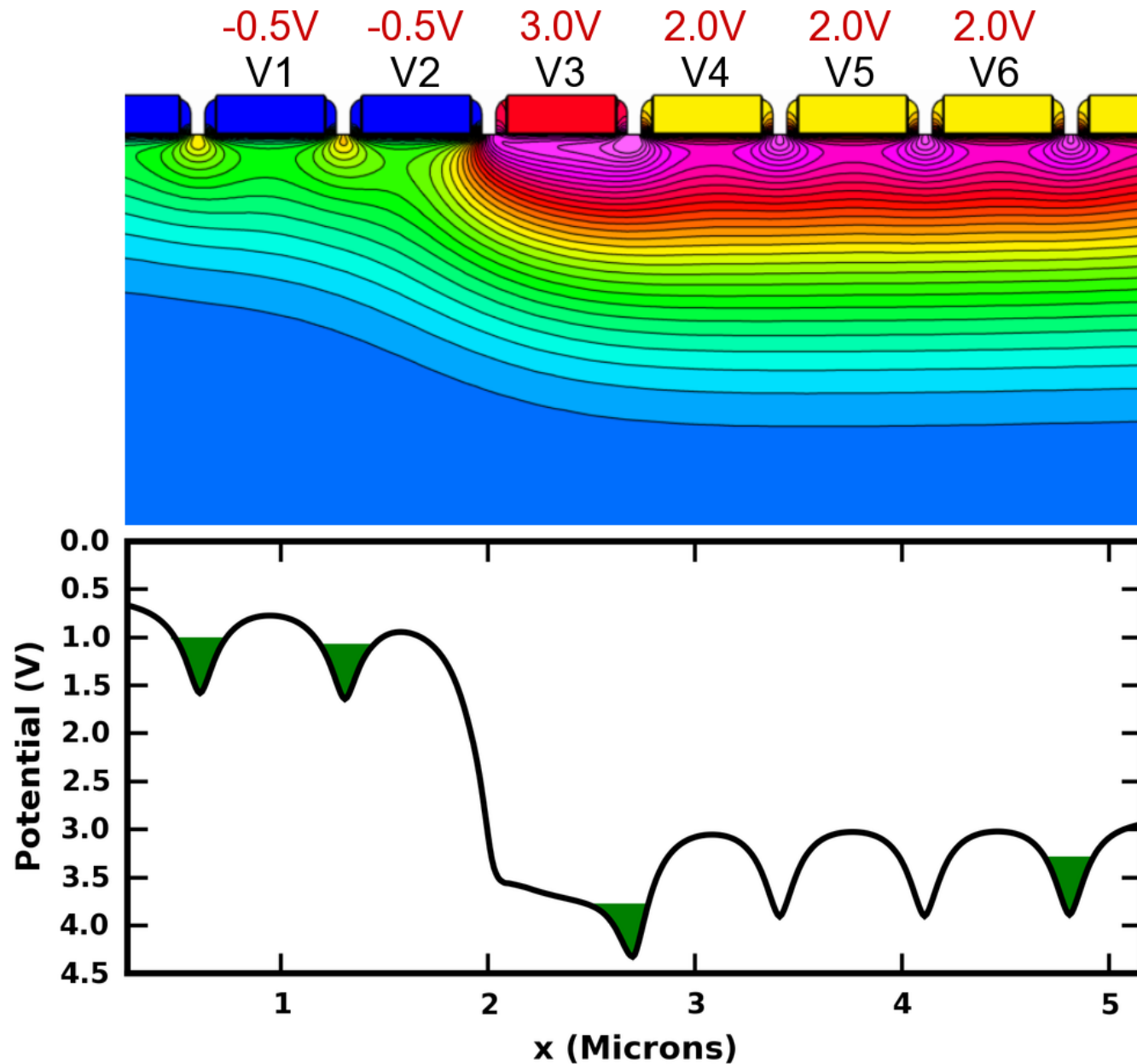
# Potential Profile Along Channel



# Potential Profile Along Channel

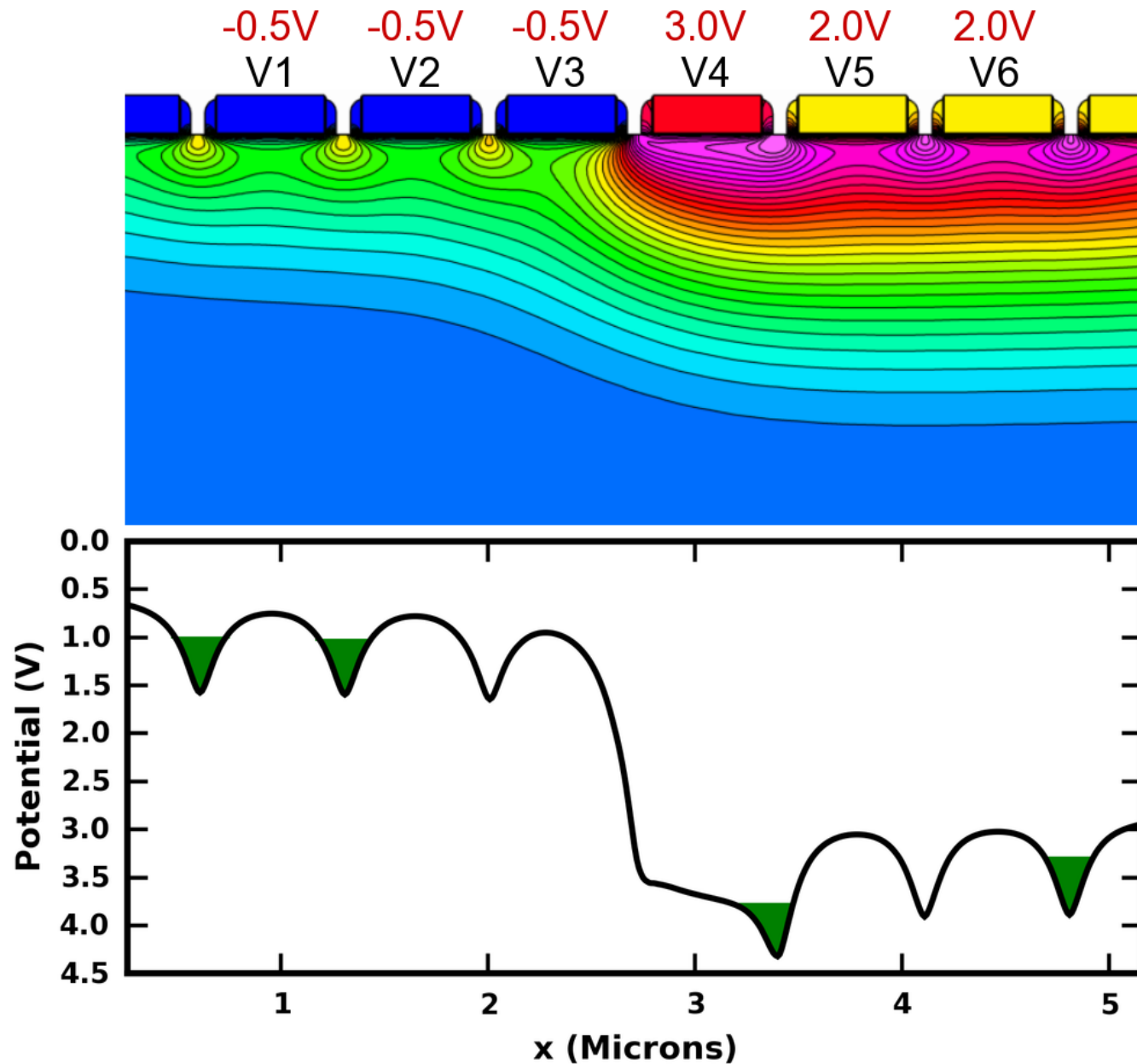


# Potential Profile Along Channel

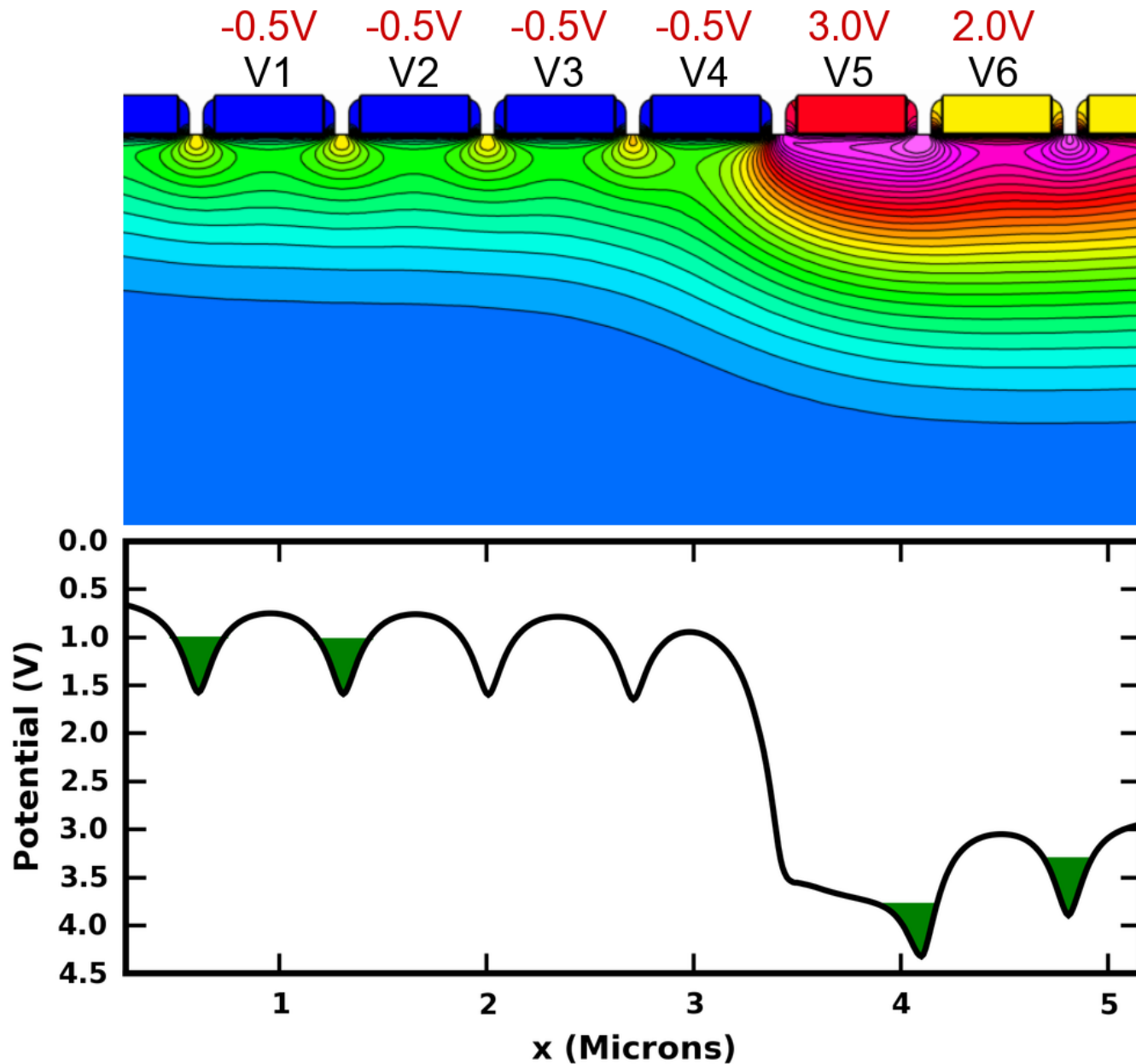




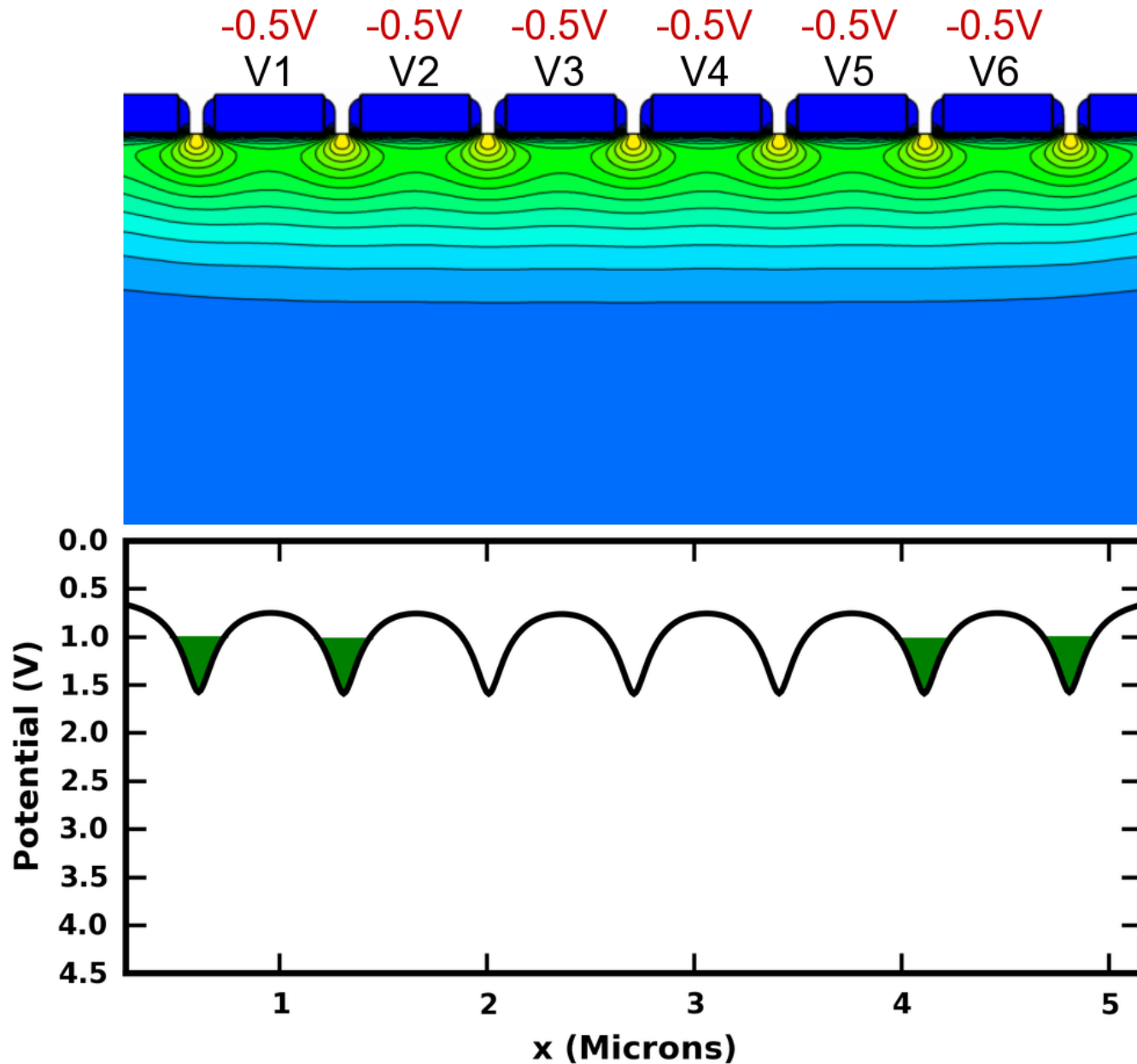
# Potential Profile Along Channel



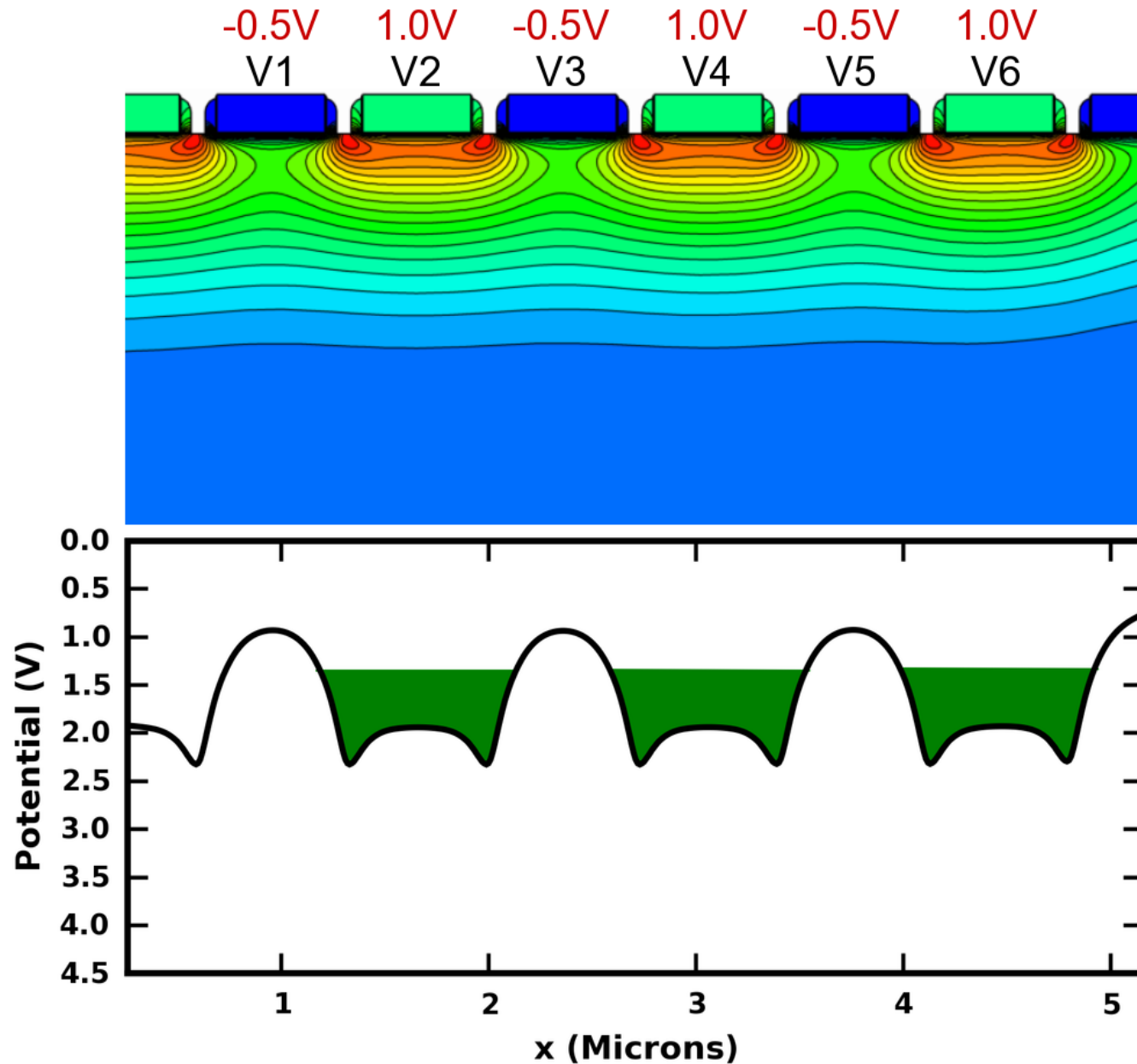
# Potential Profile Along Channel



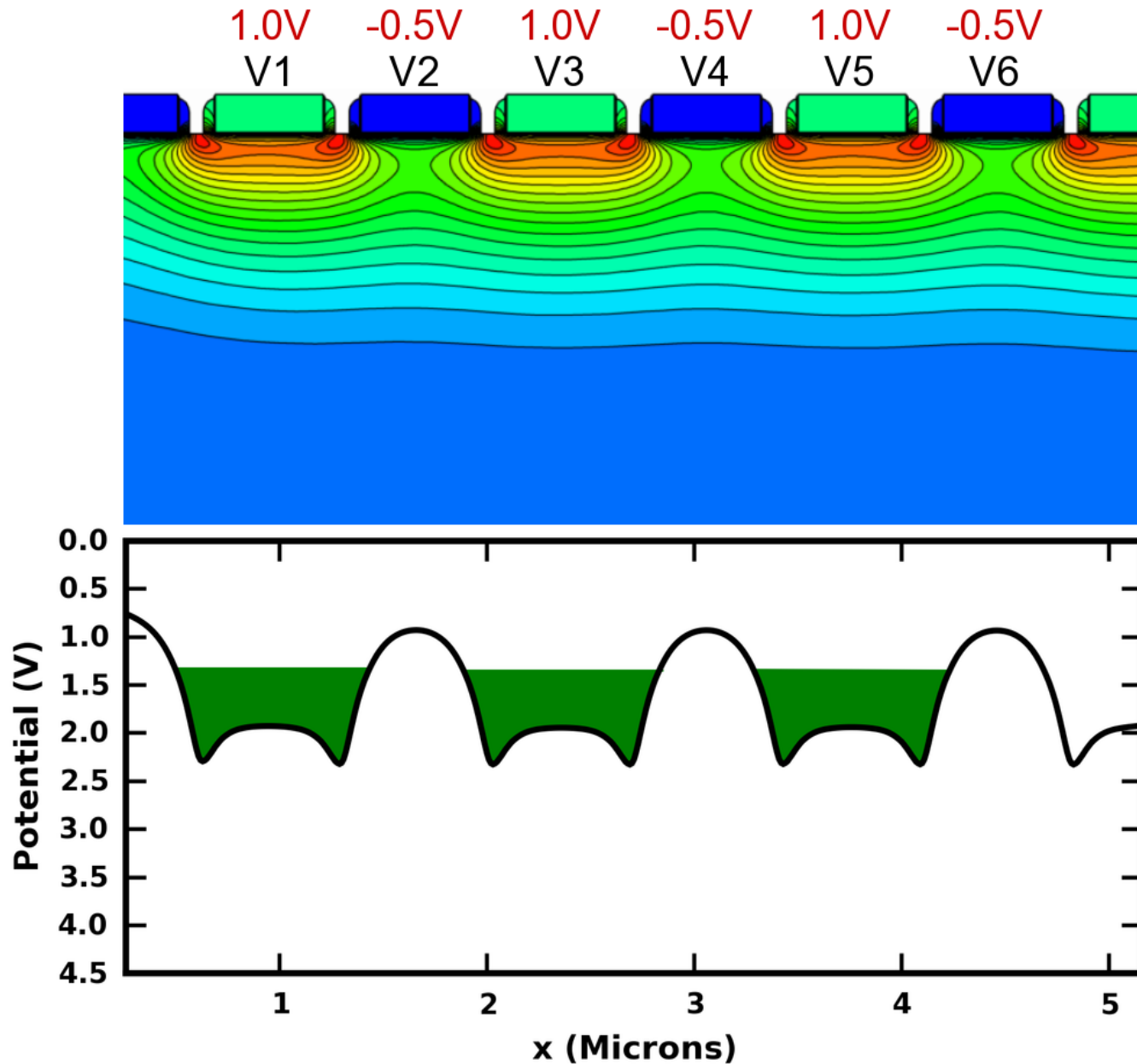
# Potential Profile Along Channel



# Interlaced Mode (Even Field)

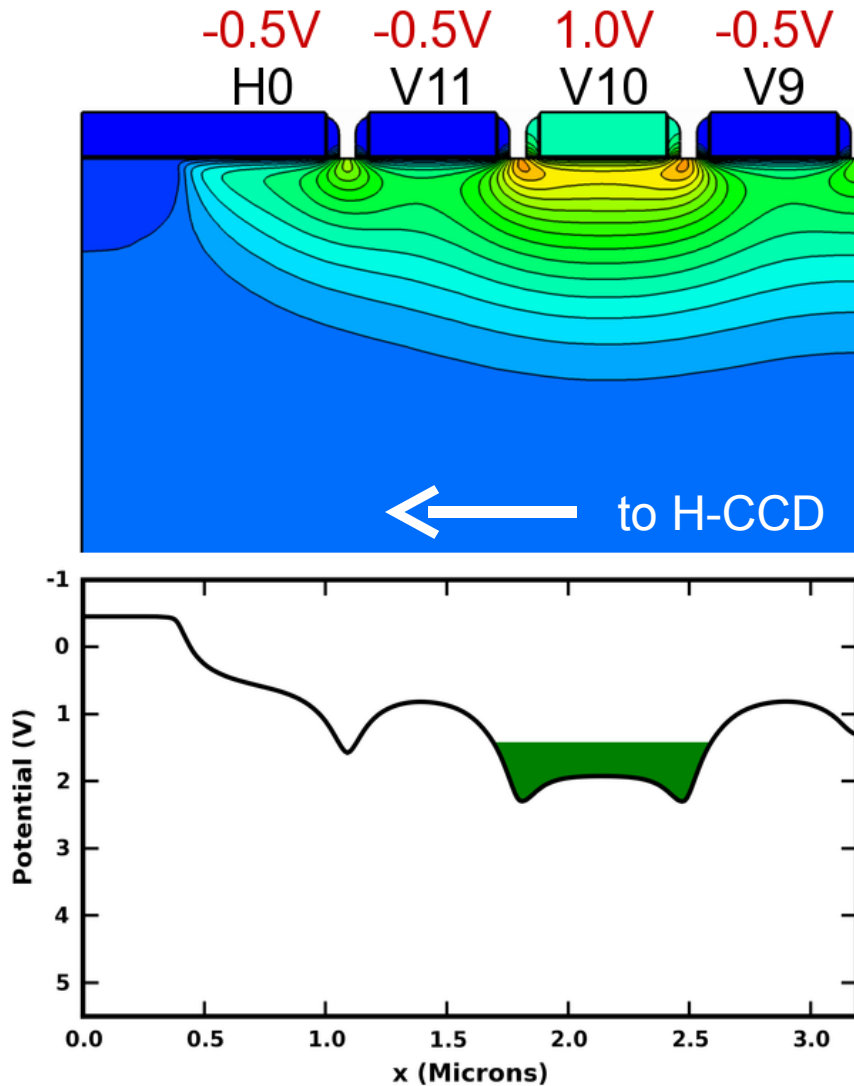


# Interlaced Mode (Odd Field)

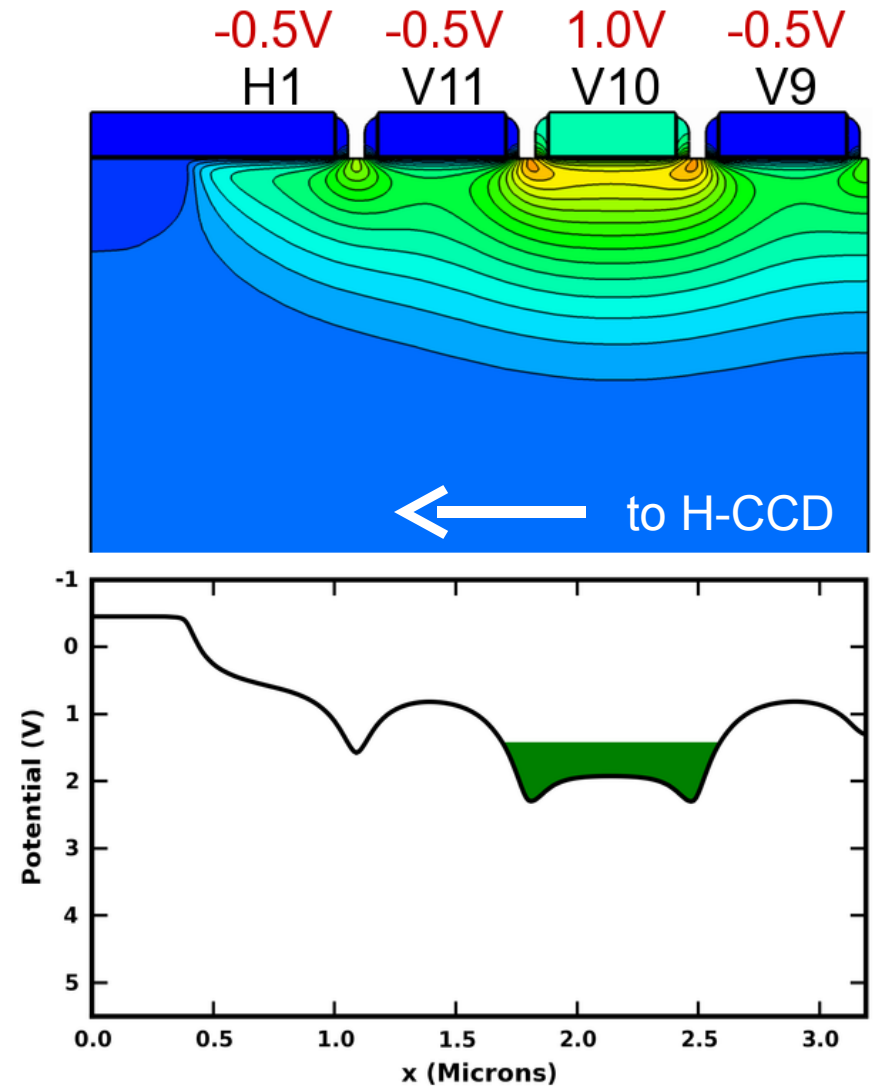


# Vertical to Horizontal Transfer

Even column

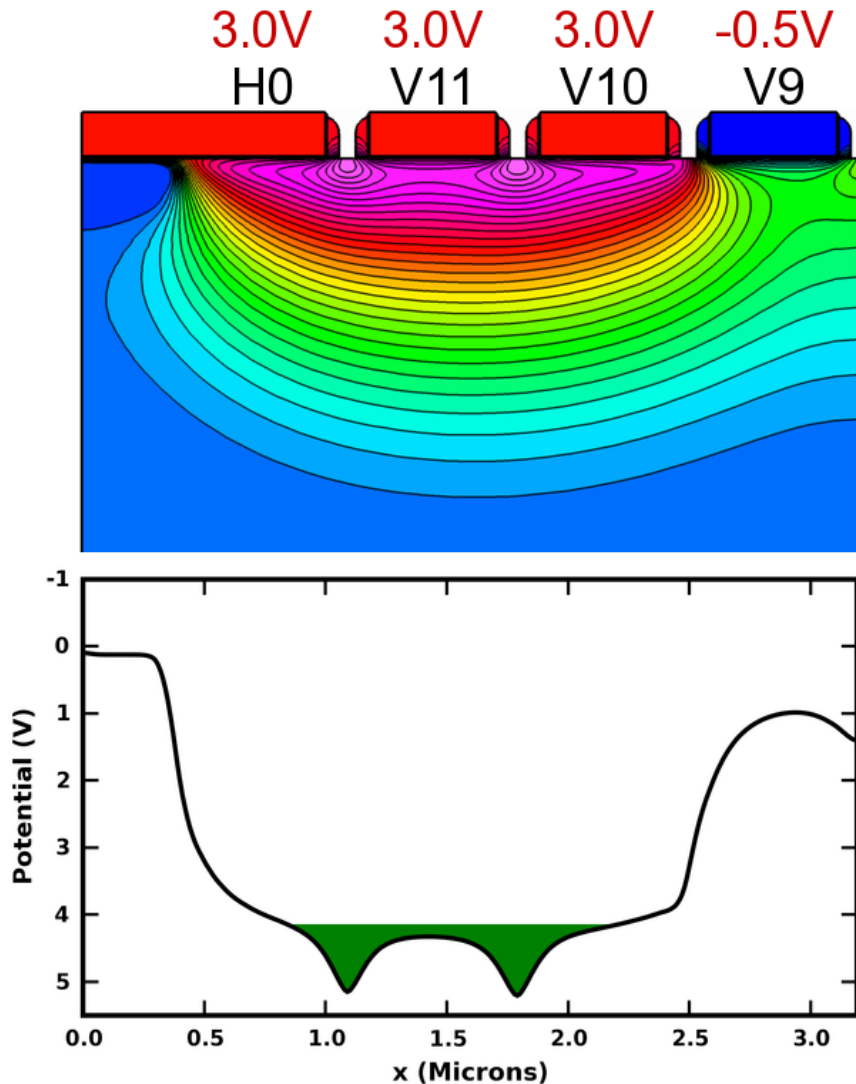


Odd column

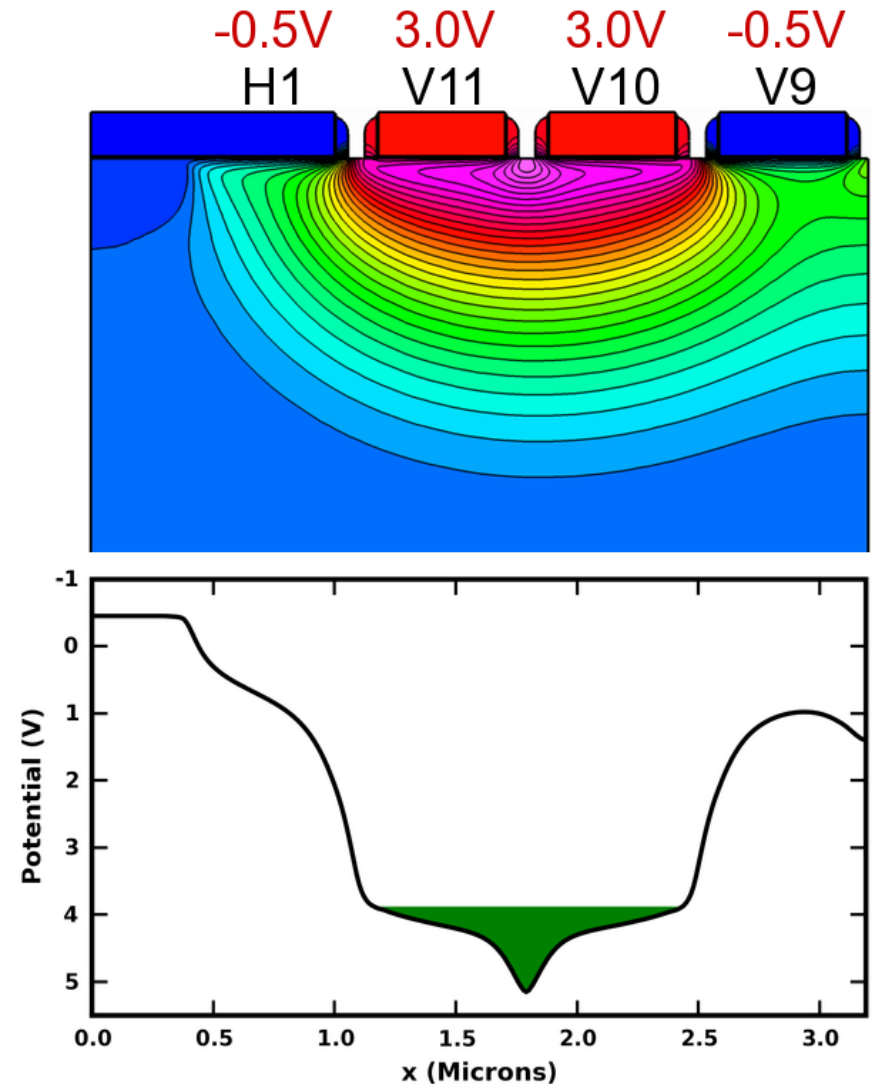


# Vertical to Horizontal Transfer

Even column

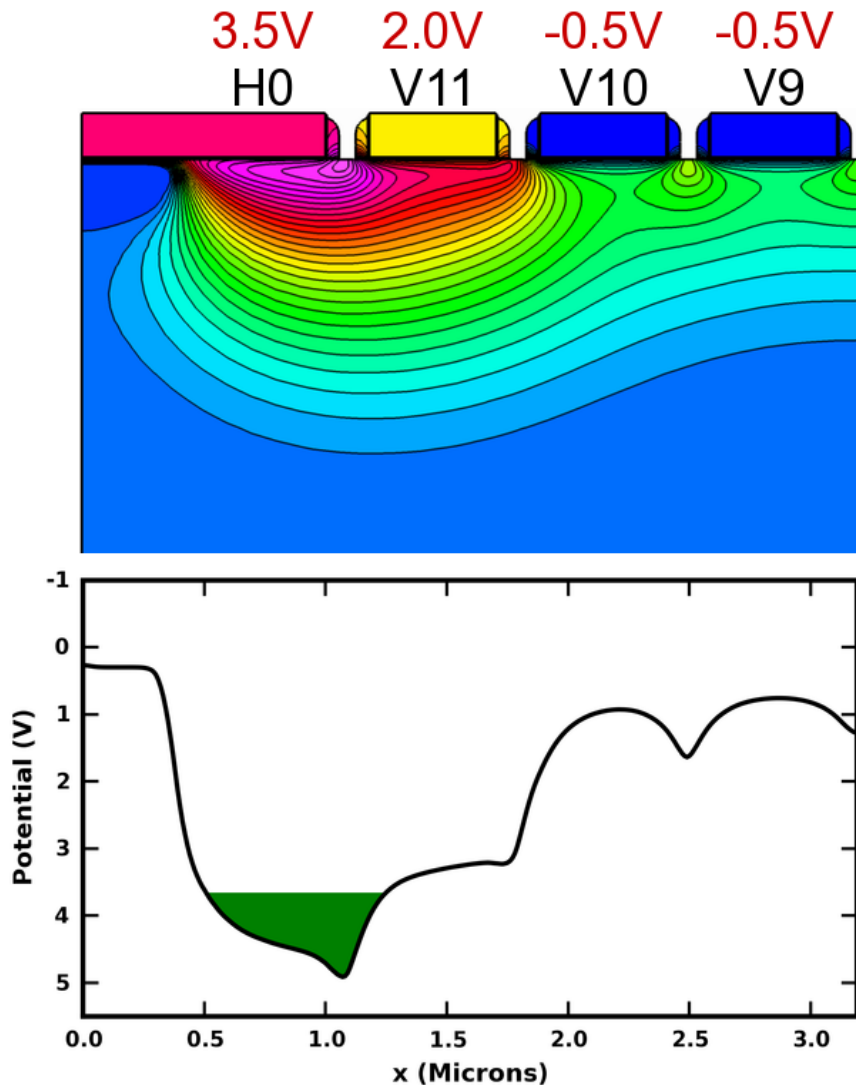


Odd column

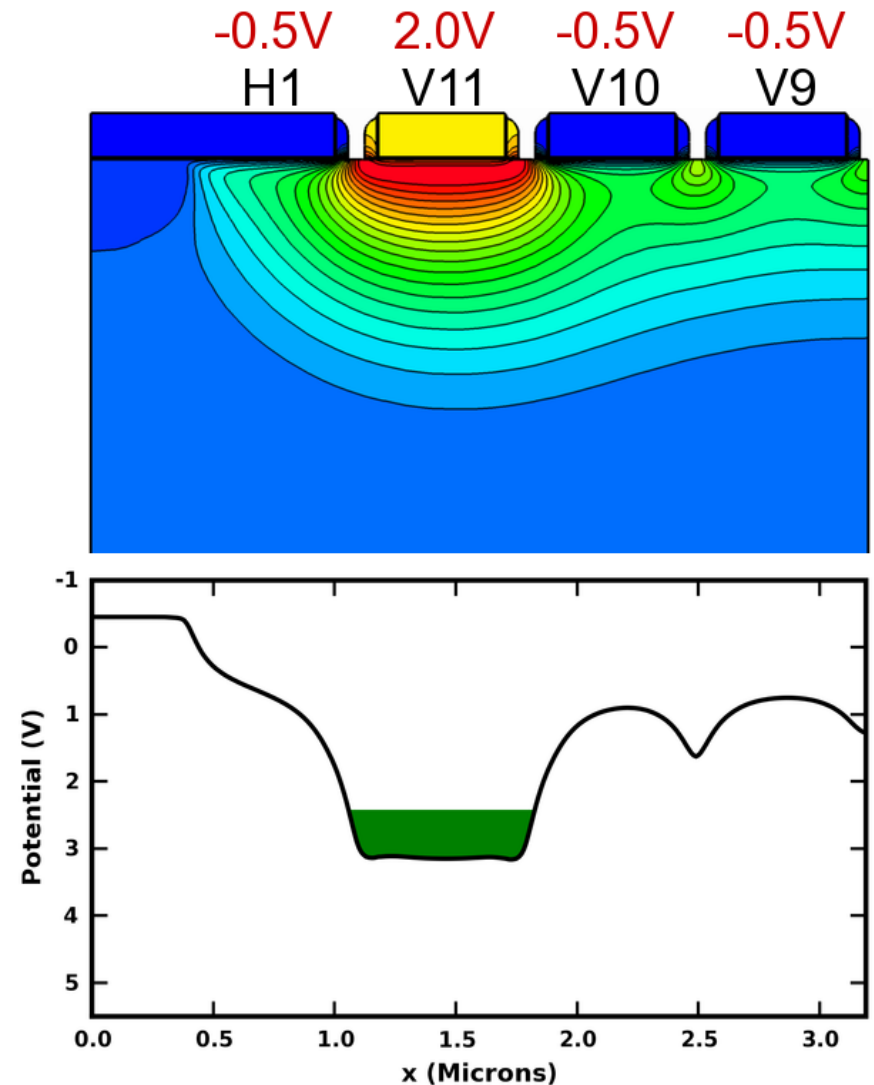


# Vertical to Horizontal Transfer

Even column



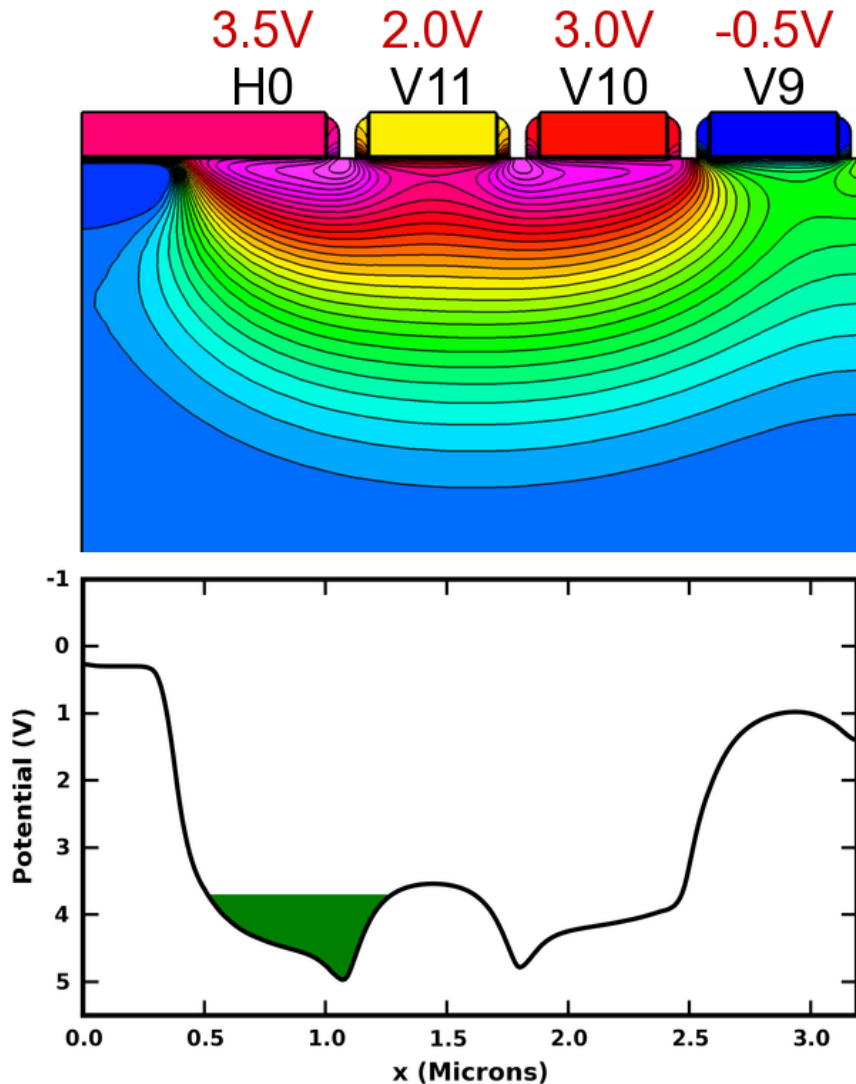
Odd column



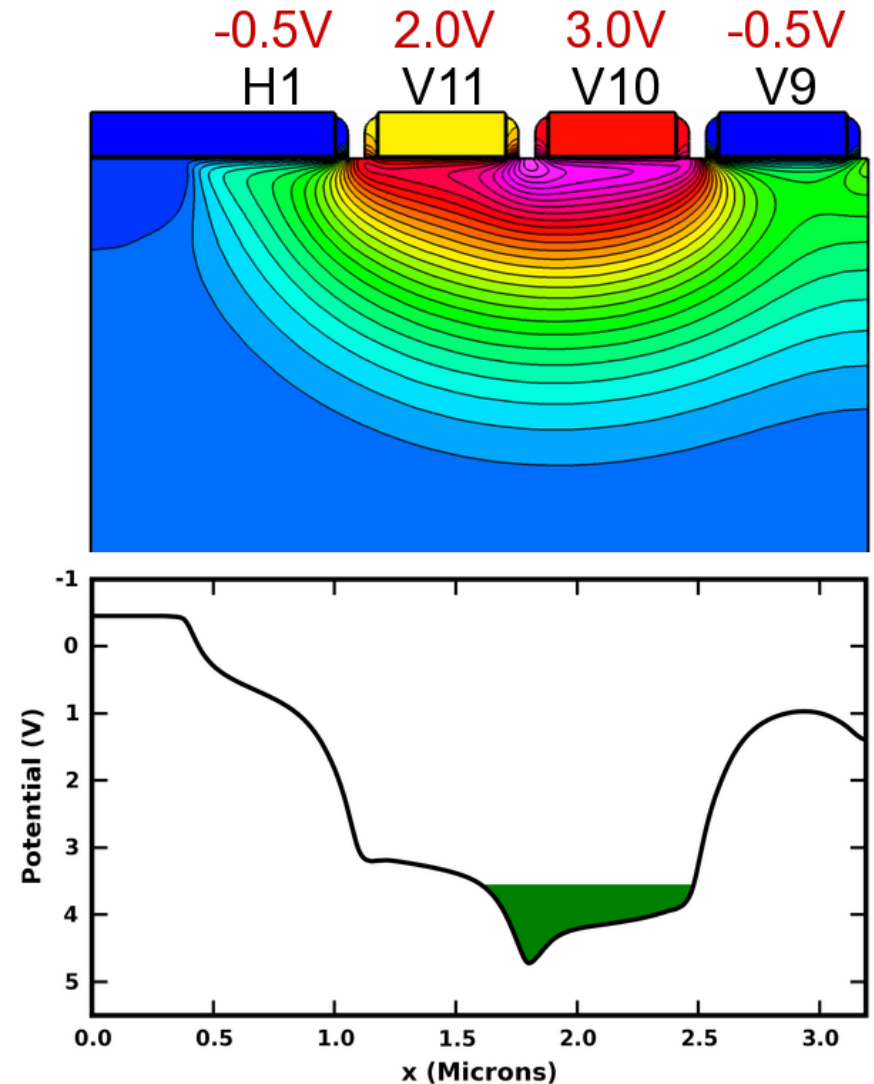


# Vertical to Horizontal Transfer

Even column

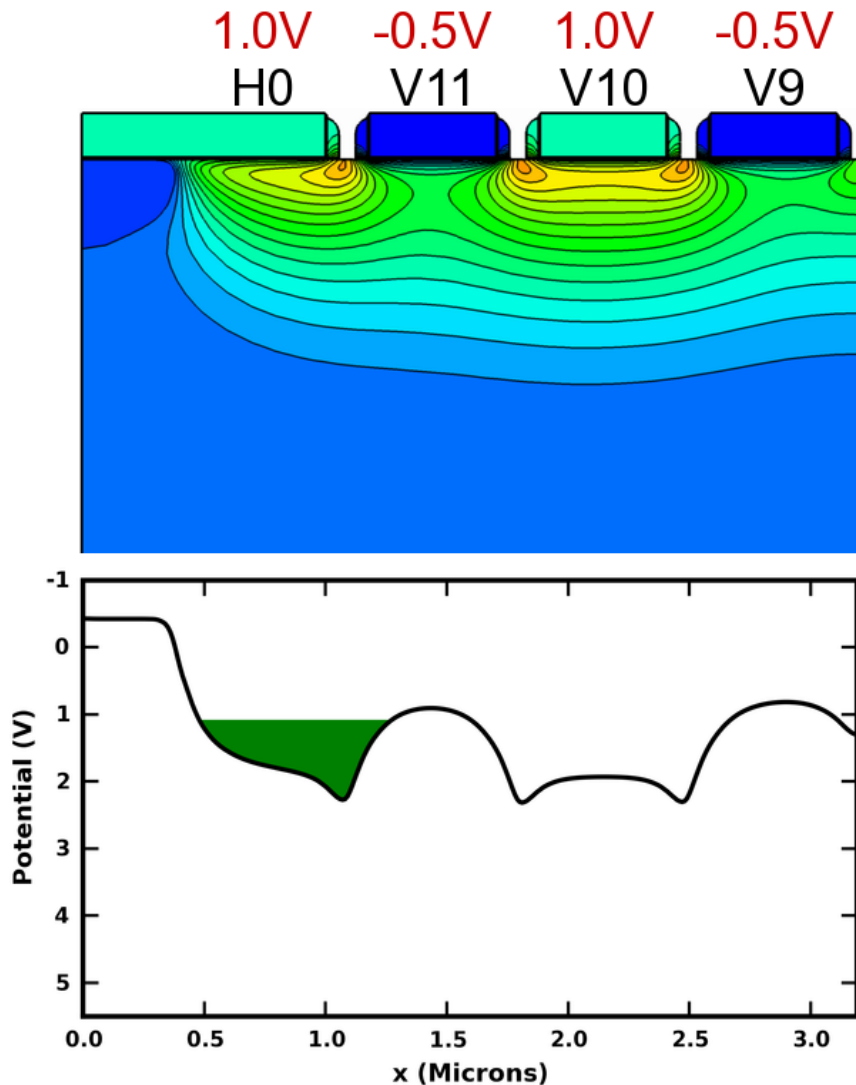


Odd column

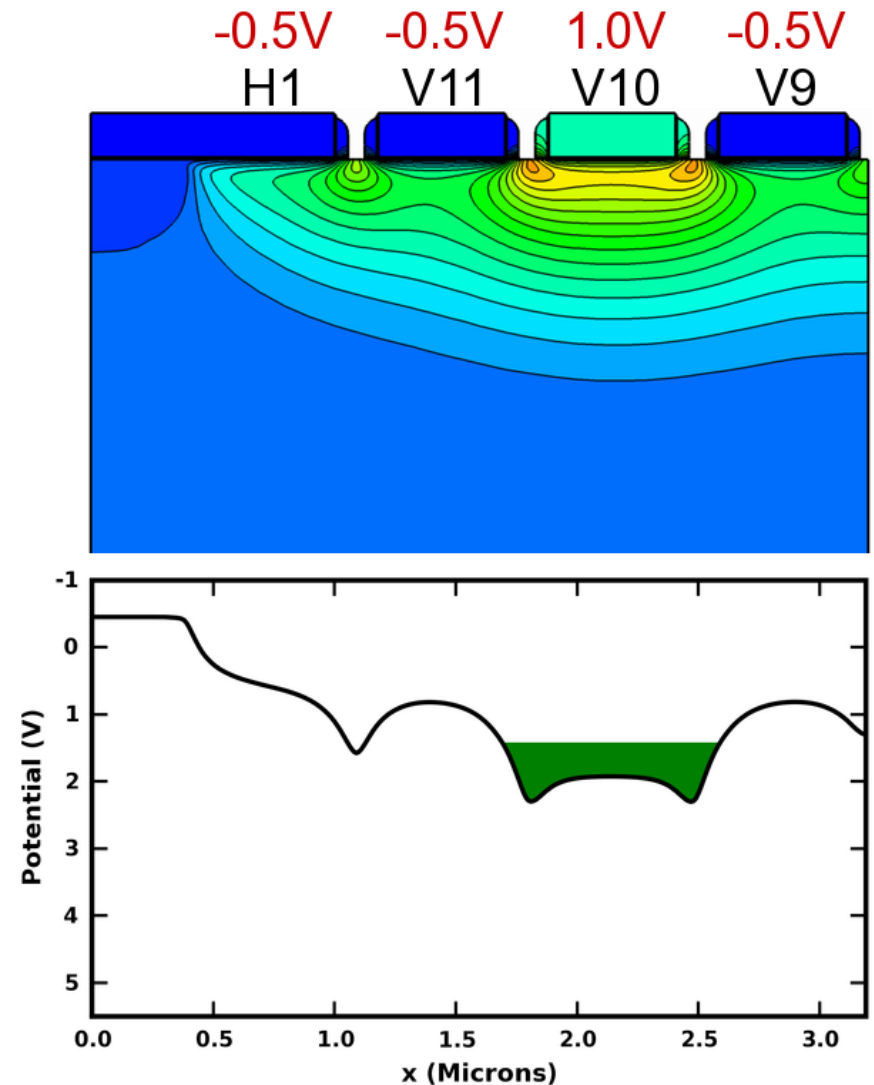


# Vertical to Horizontal Transfer

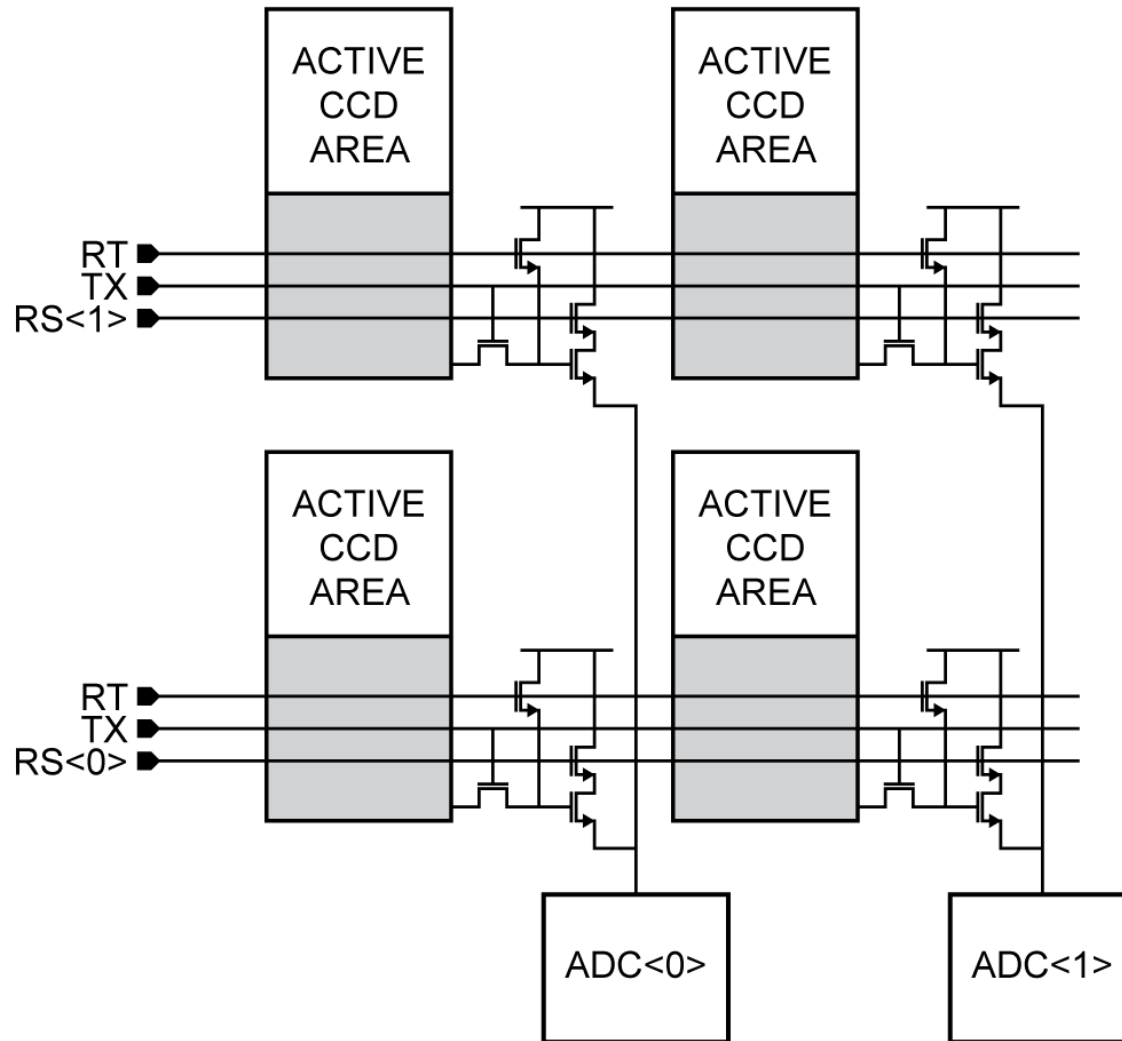
Even column



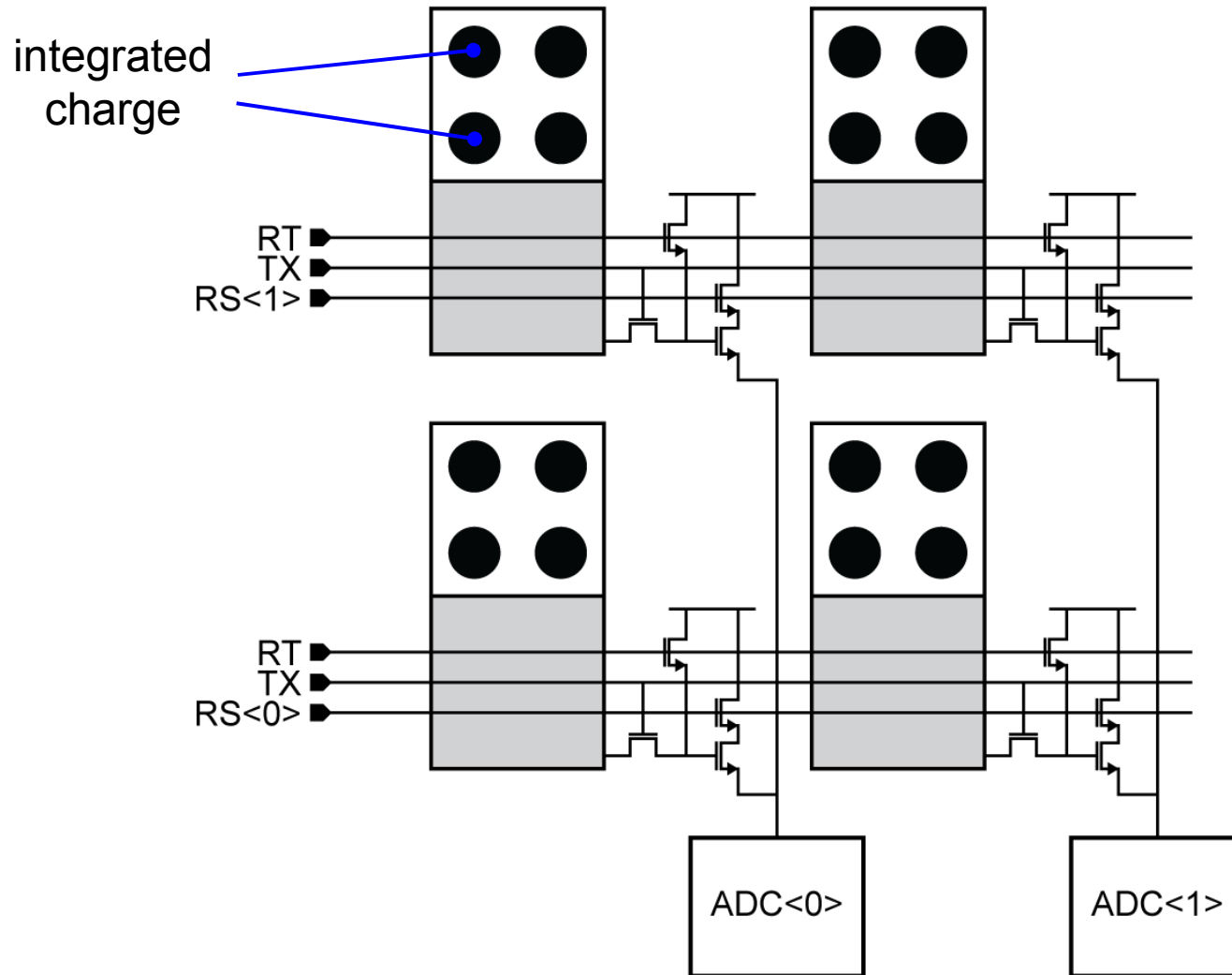
Odd column



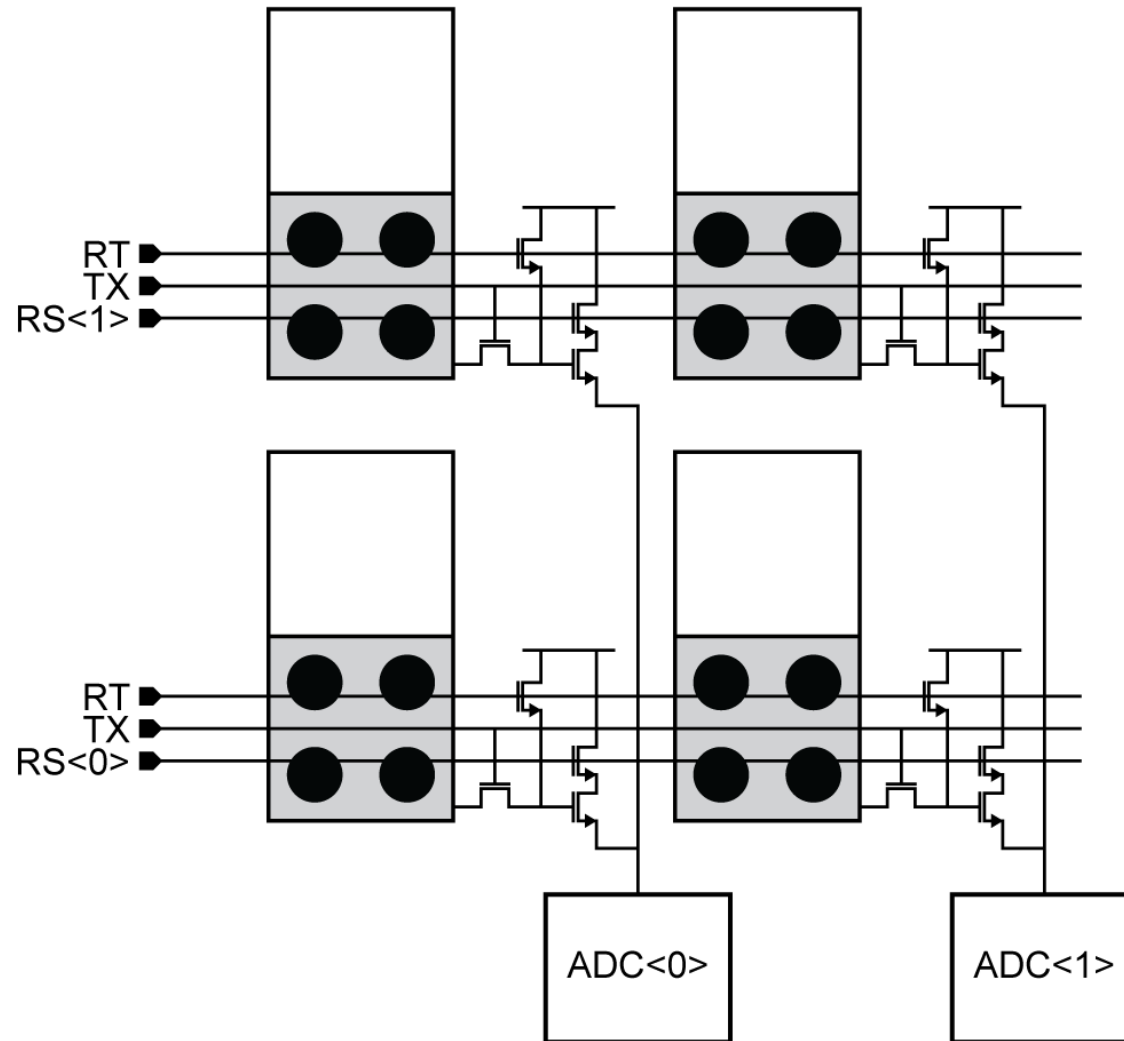
# Chip Operation



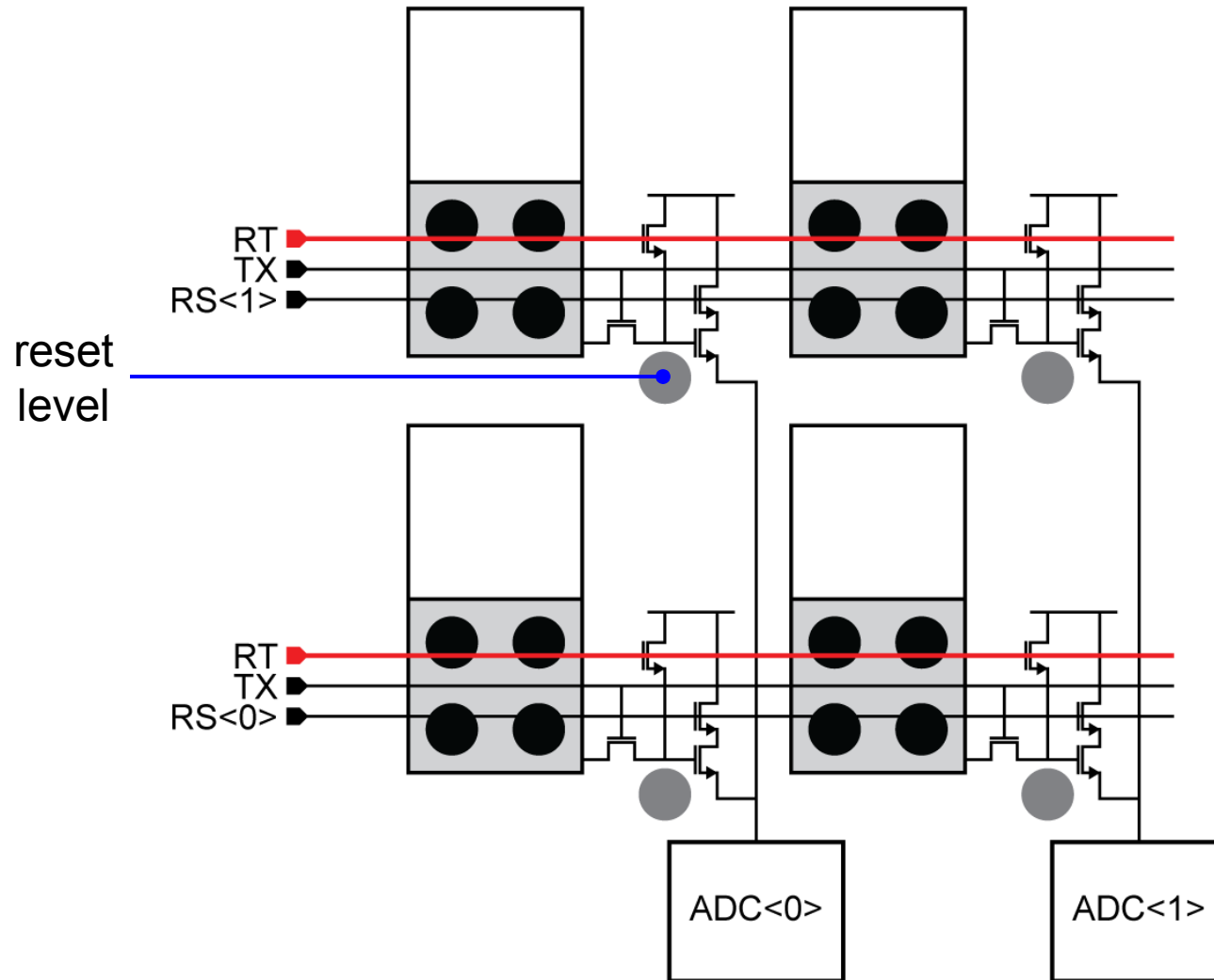
# Chip Operation (Integrate)



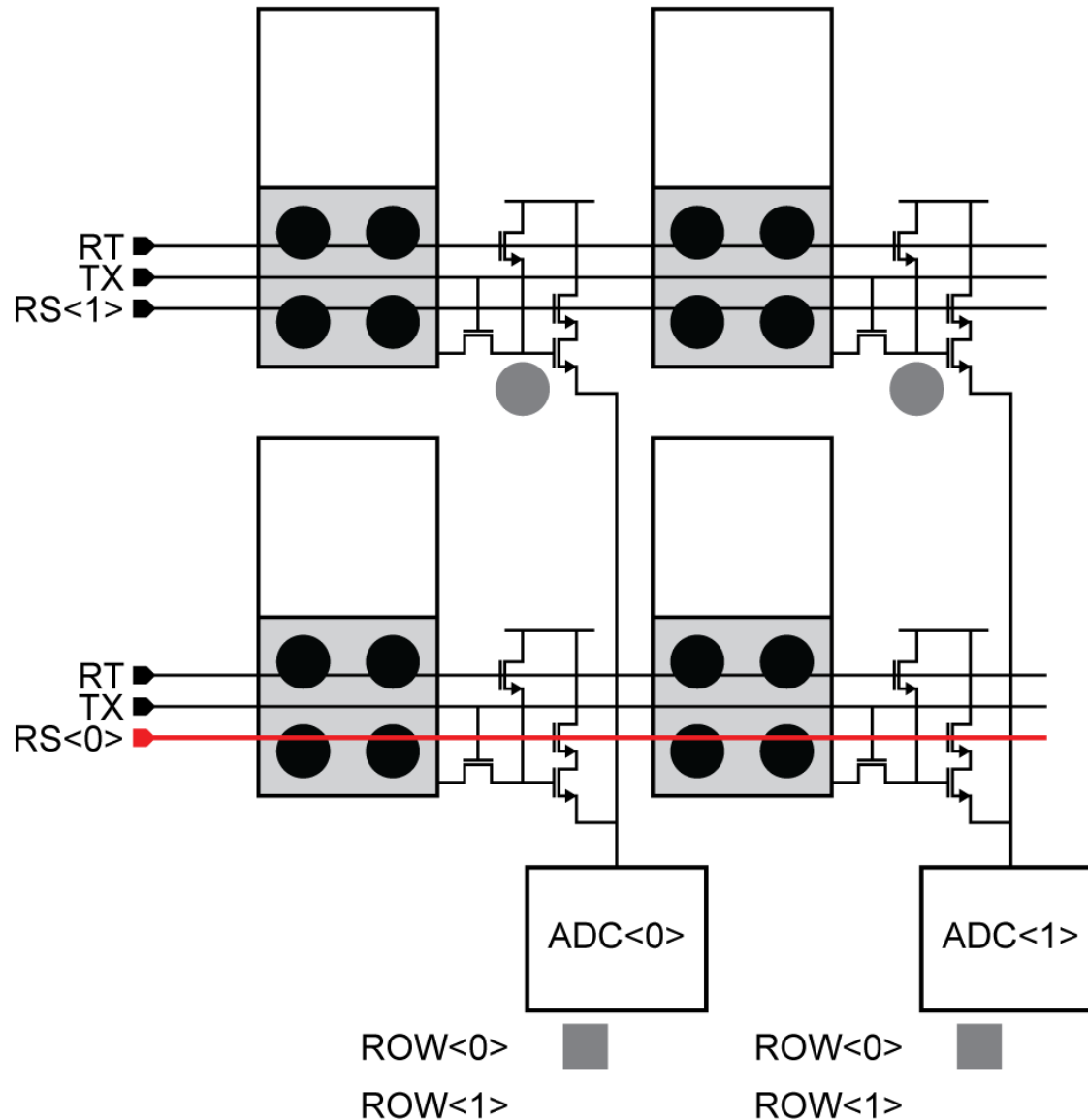
# Chip Operation (Frame Transfer)



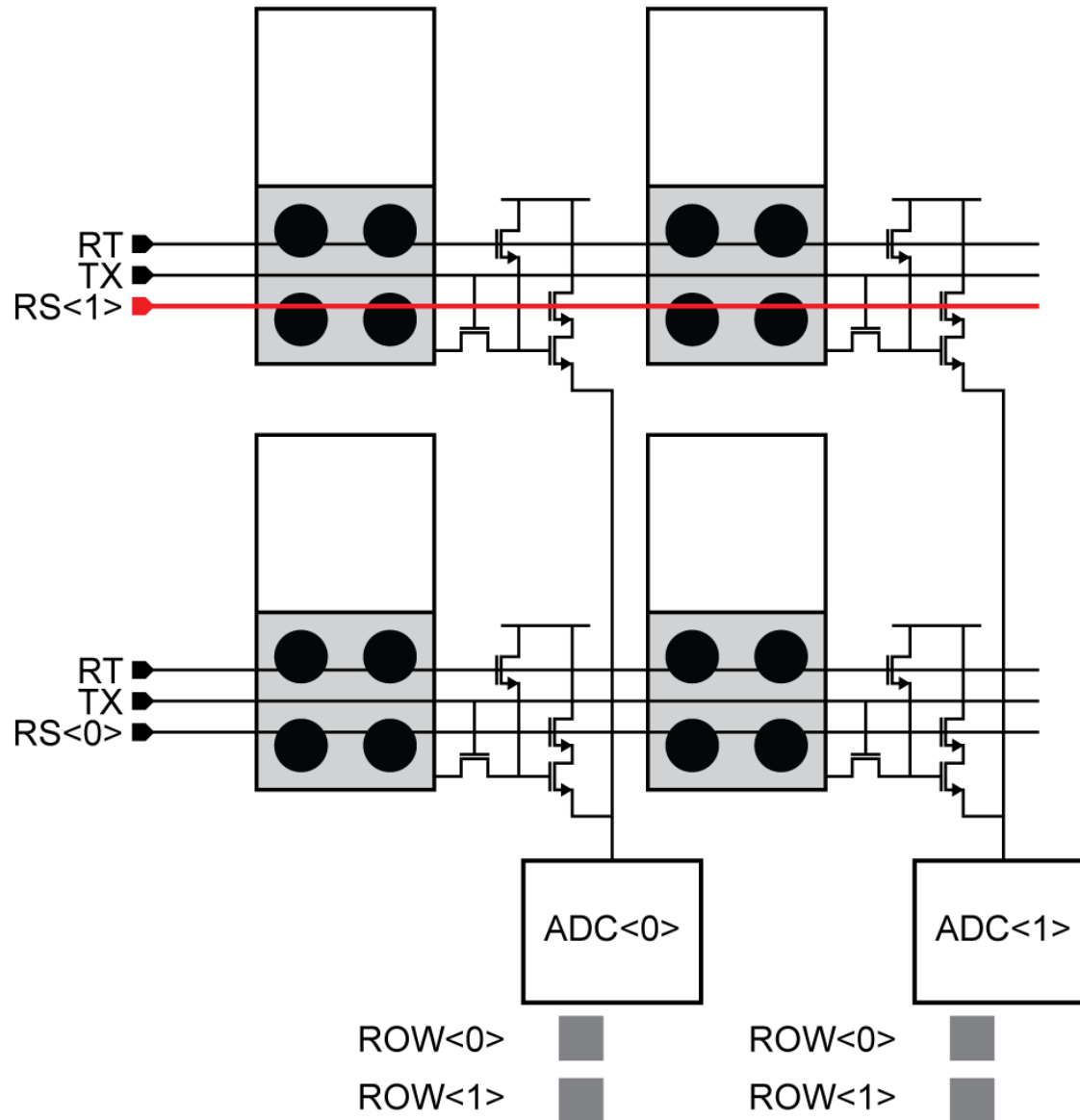
# Chip Operation (Reset FD)



# Chip Operation (Read Row<0>)

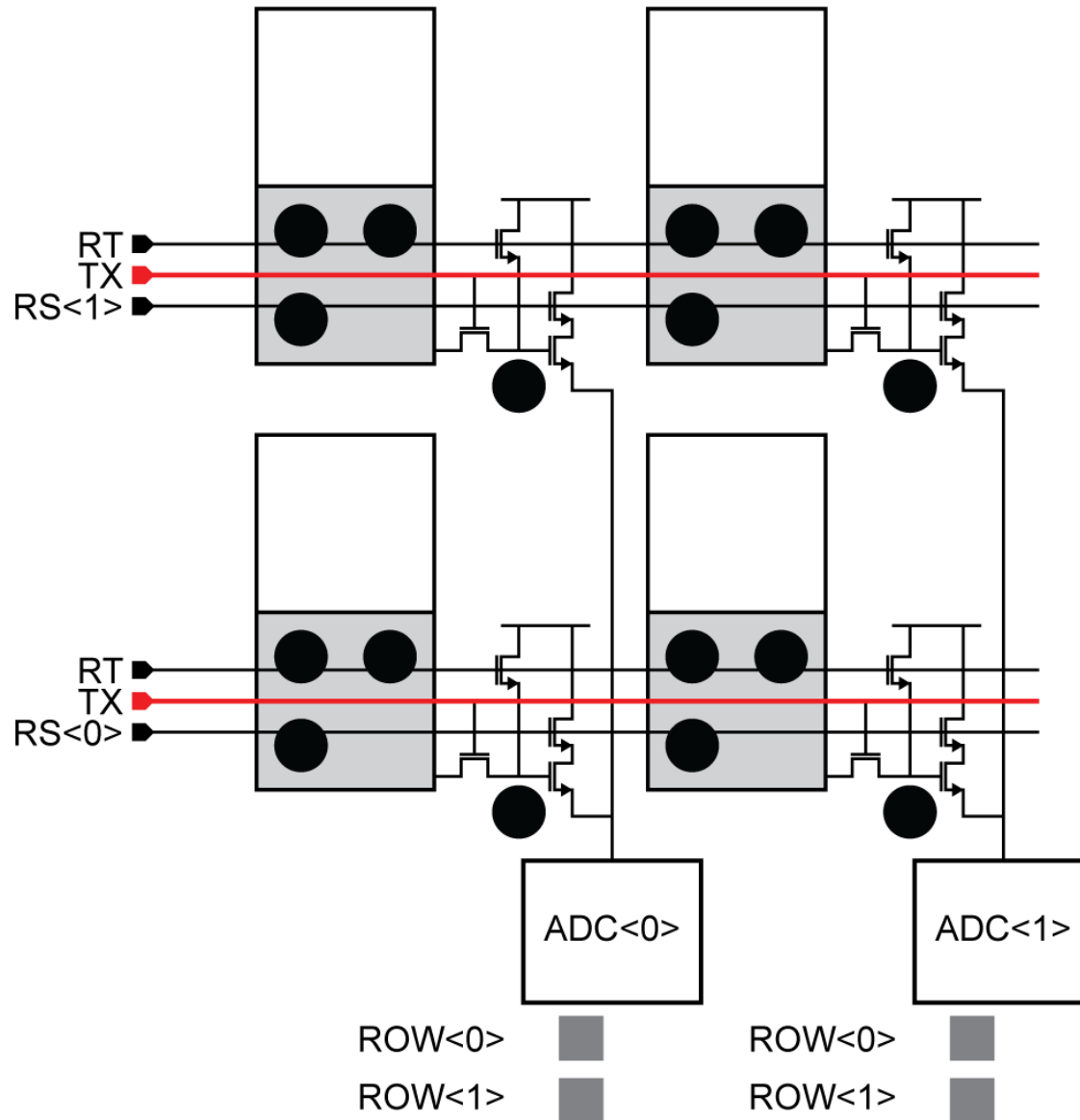


# Chip Operation (Read Row<1>)

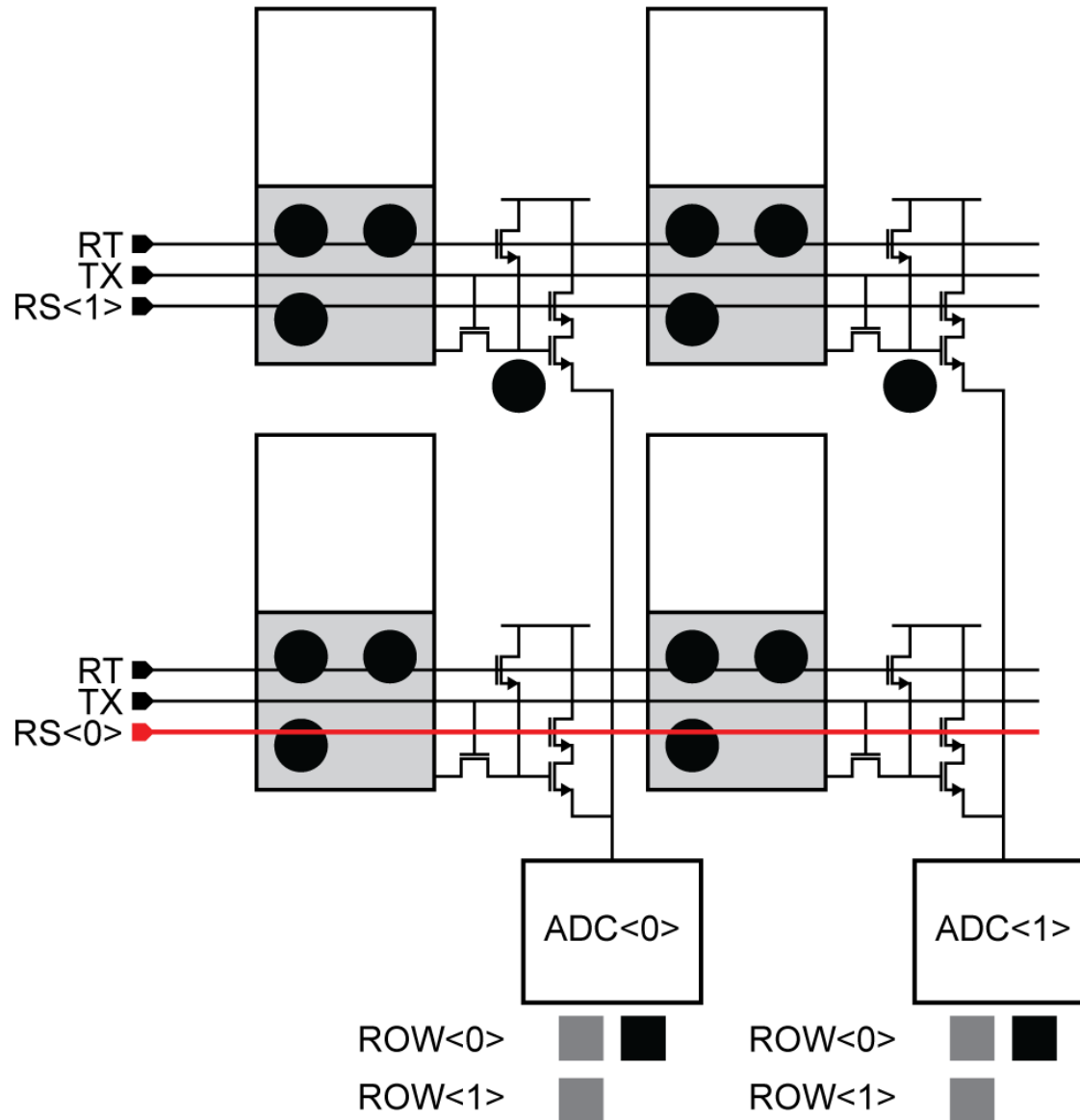




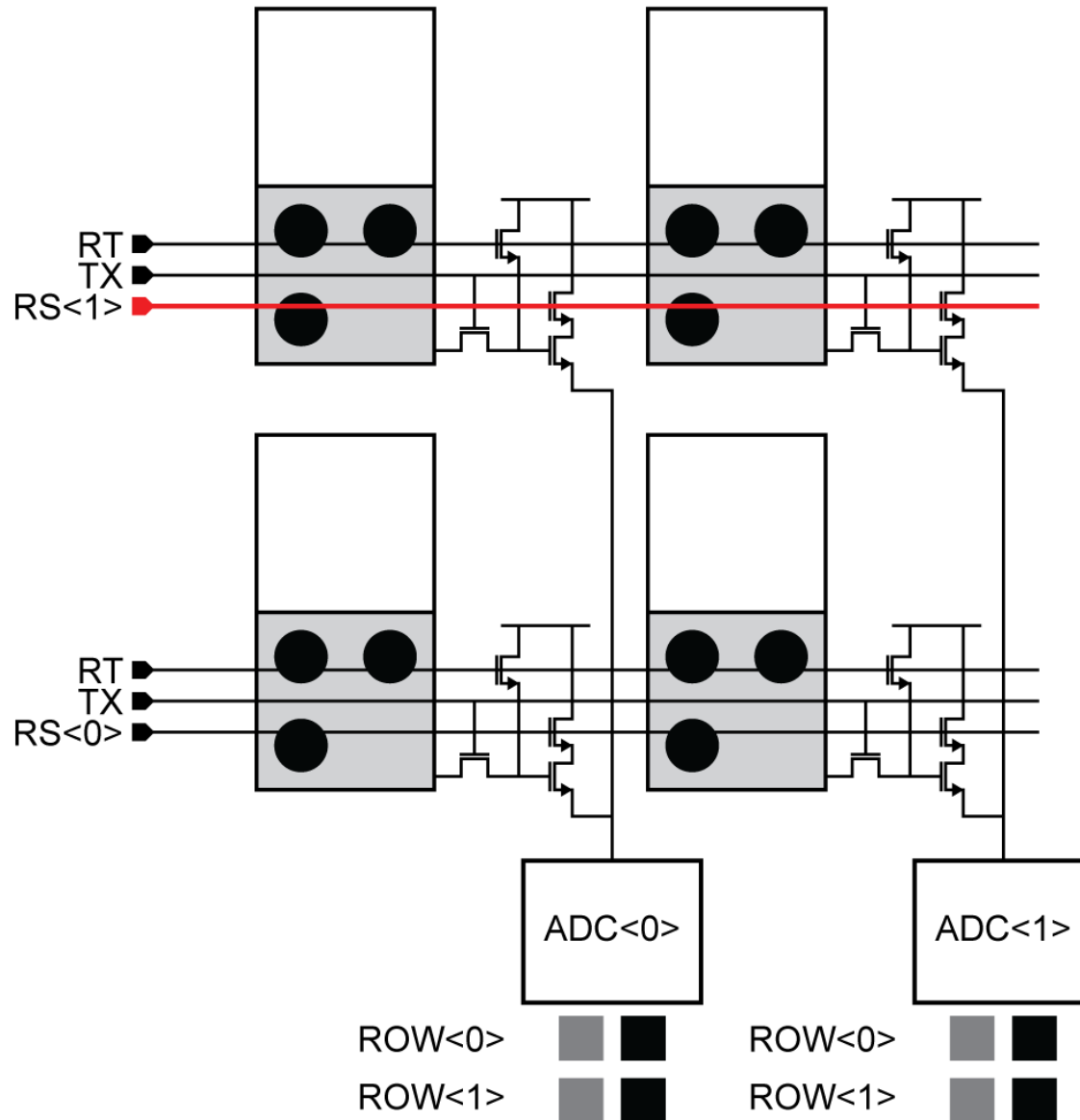
# Chip Operation (Transfer Charge)



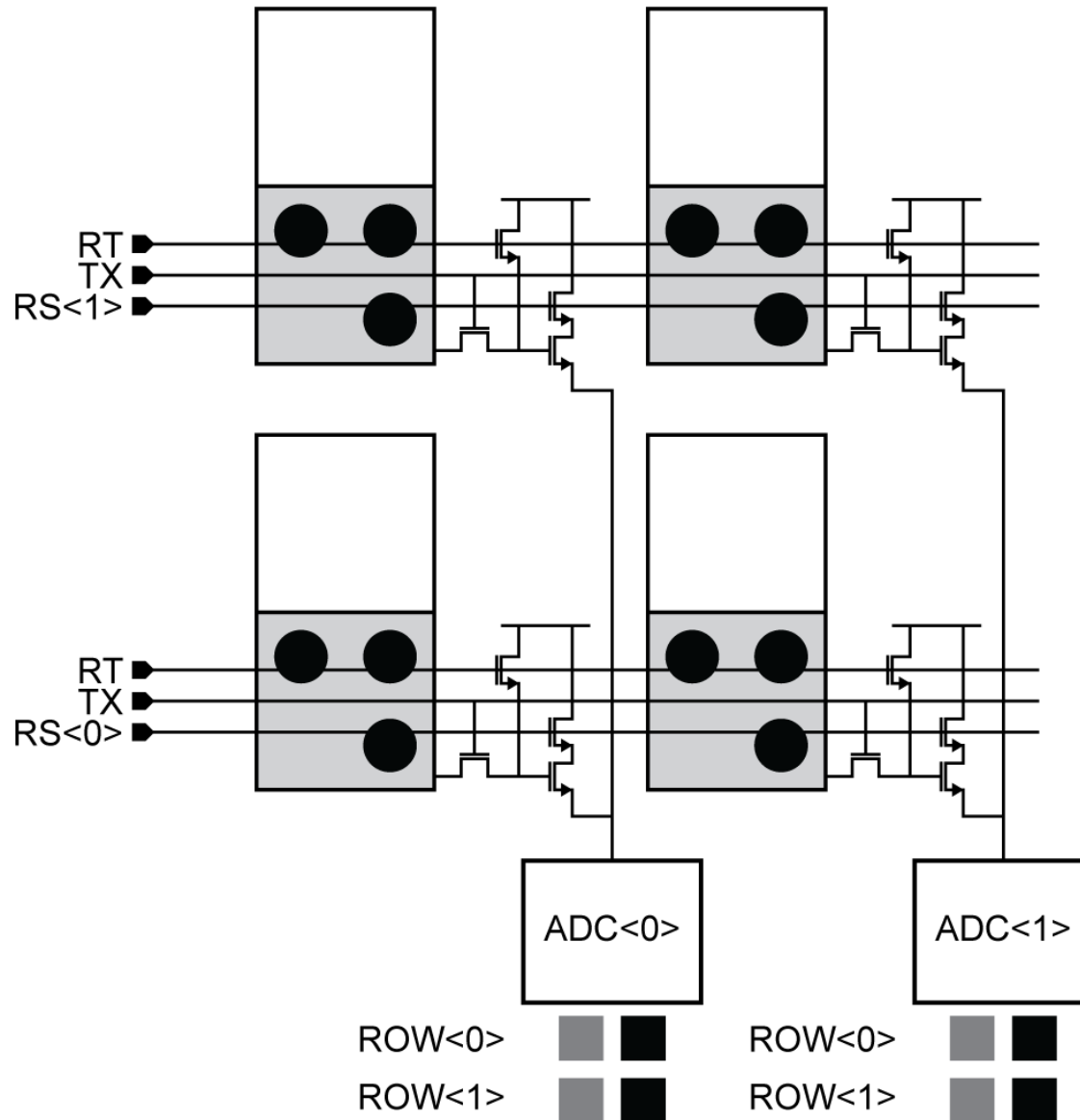
# Chip Operation (Charge Row<0>)



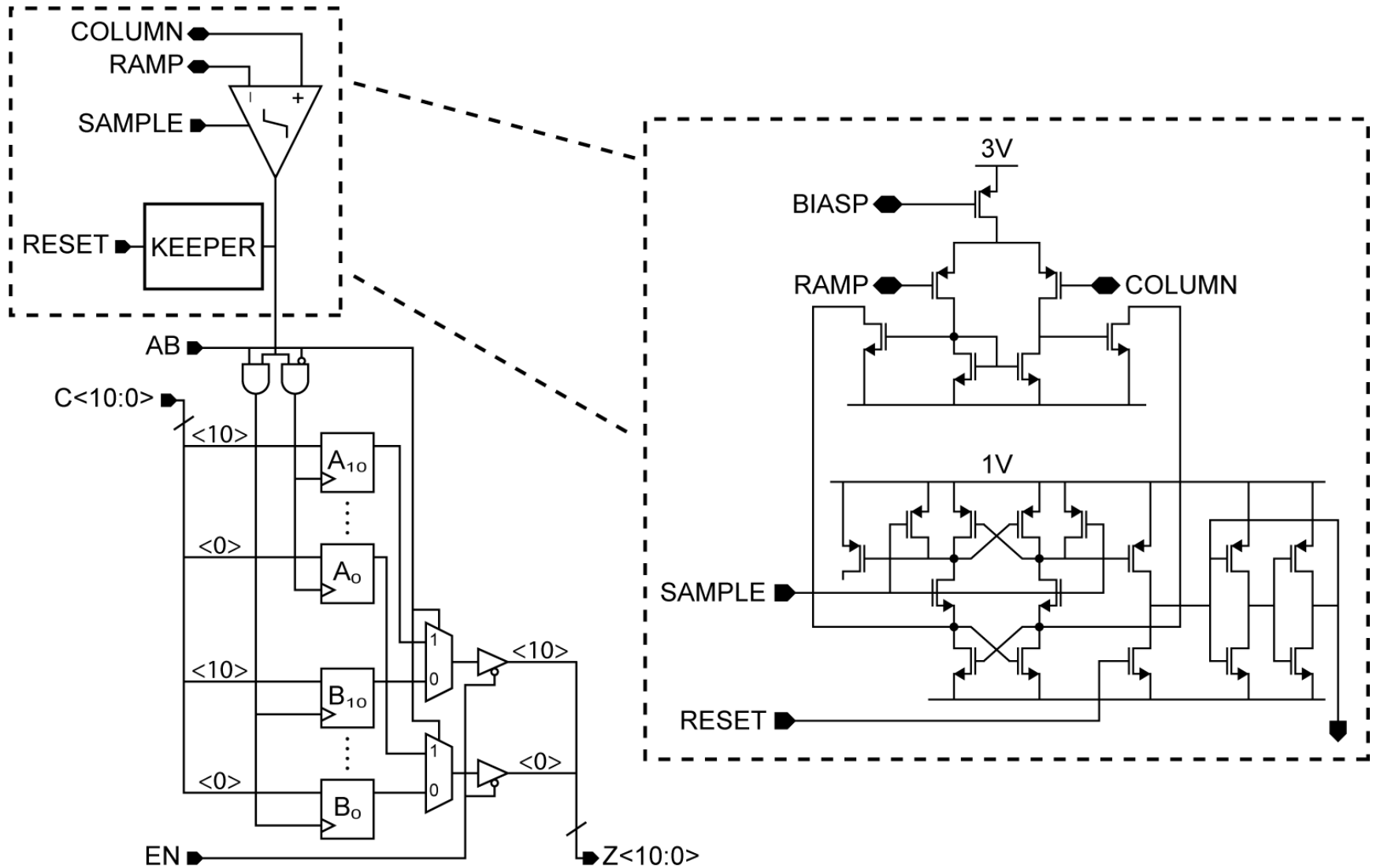
# Chip Operation (Charge Row<1>)



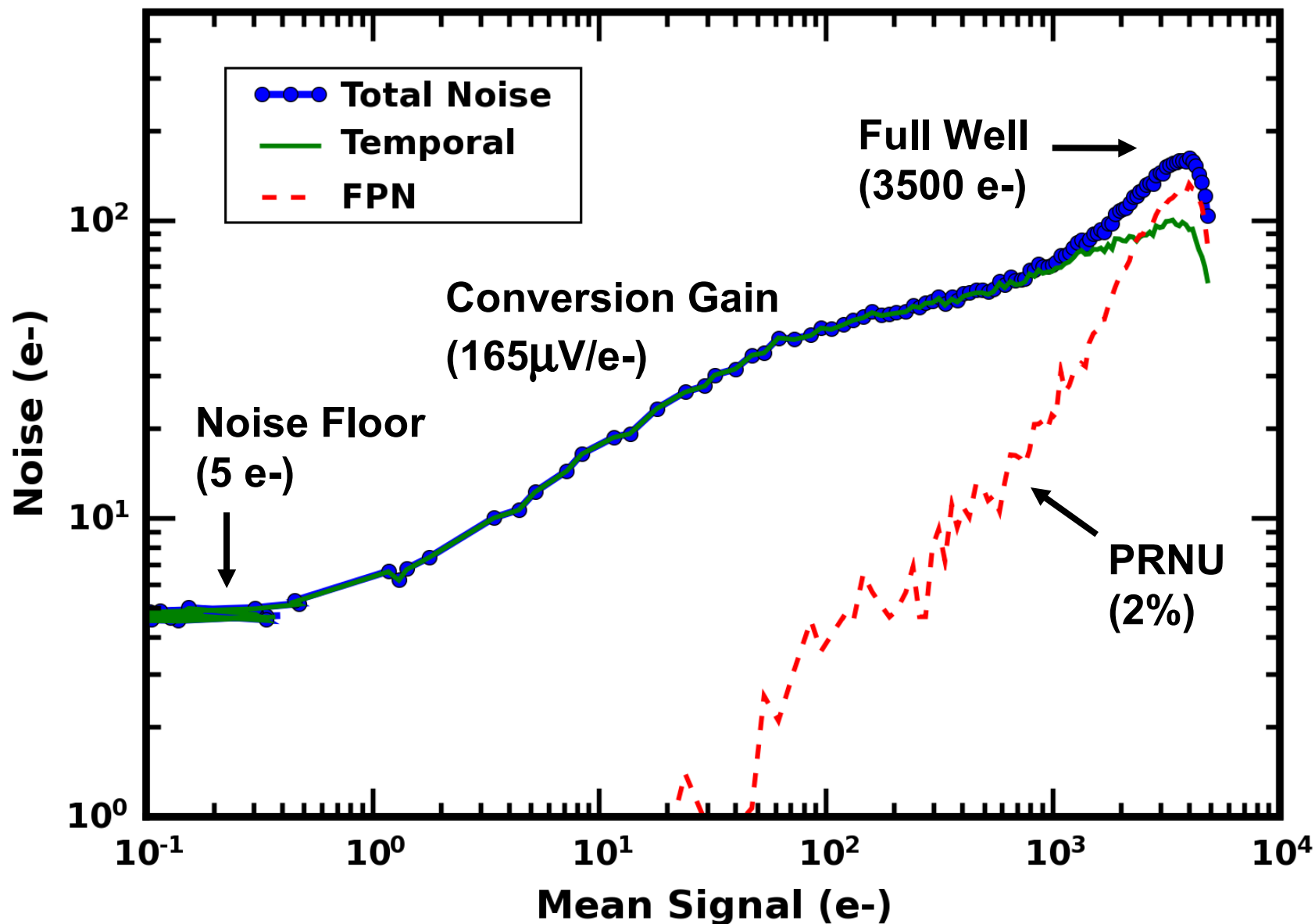
# Chip Operation (Shift Charge)



# Column ADC Schematic



# Measured Photon Transfer Curve

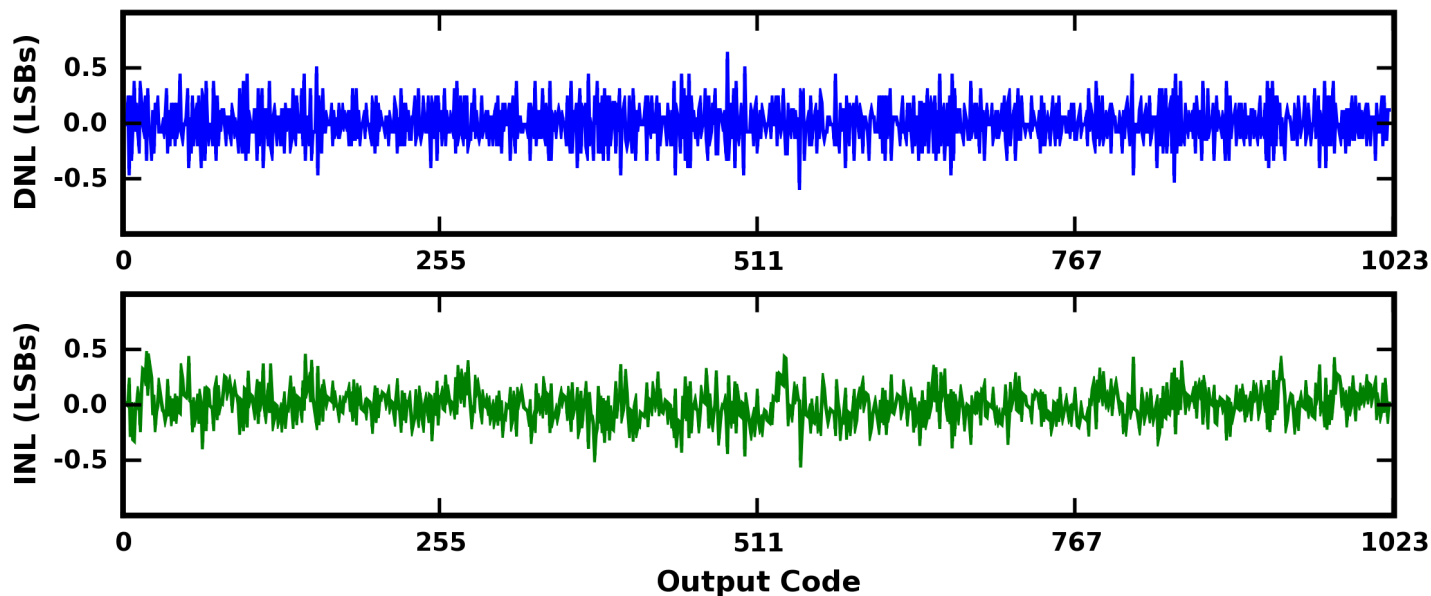


# Measured Pixel Characteristics

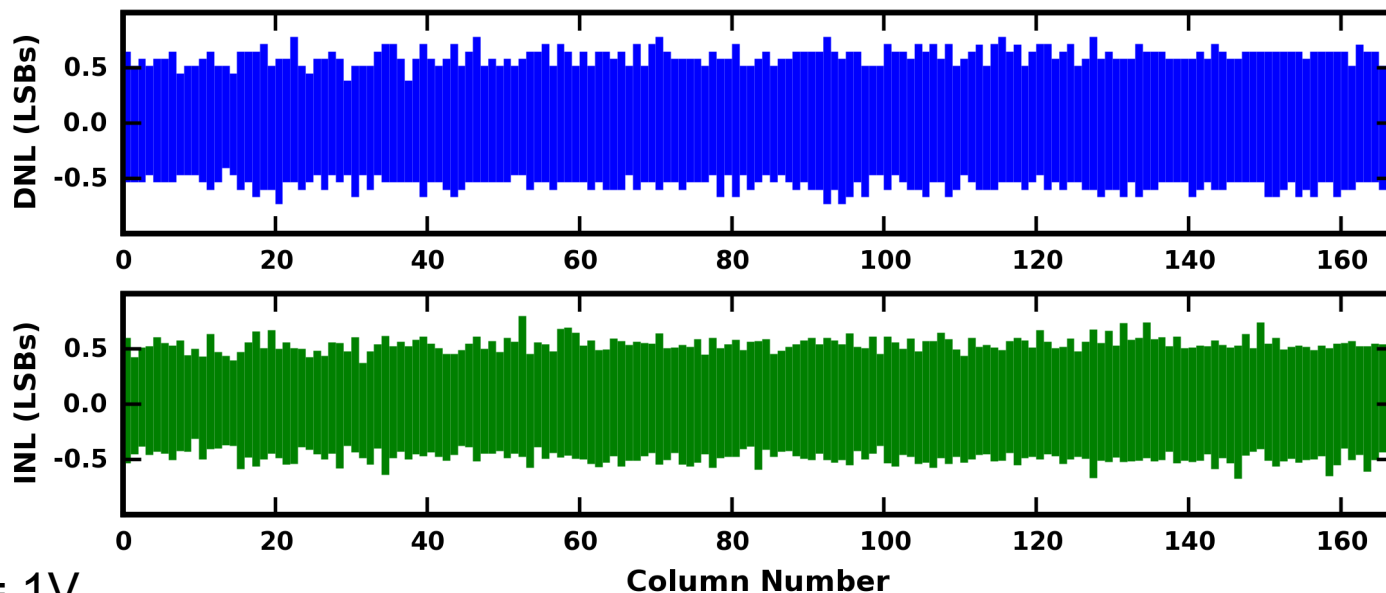
|                        |                                     |
|------------------------|-------------------------------------|
| Well capacity          | 3500 e <sup>-</sup>                 |
| Conversion gain        | 165 $\mu\text{V}/\text{e}^-$        |
| Sensitivity at 550 nm  | 0.15V/lux-sec                       |
| QE at 450, 550, 650 nm | 20, 48, 65 %                        |
| Pixel read noise       | 5 e <sup>-</sup> rms (1mV)          |
| Dark current at RT     | 33 e <sup>-</sup> /sec (5.5 mV/sec) |
| DSNU                   | 35 % rms                            |
| PRNU                   | 2 % rms                             |
| Peak SNR               | 35 dB                               |
| Dynamic range          | 57 dB                               |

# Measured ADC Linearity

Single  
Column  
(10-b)



All  
Columns  
(10-b)

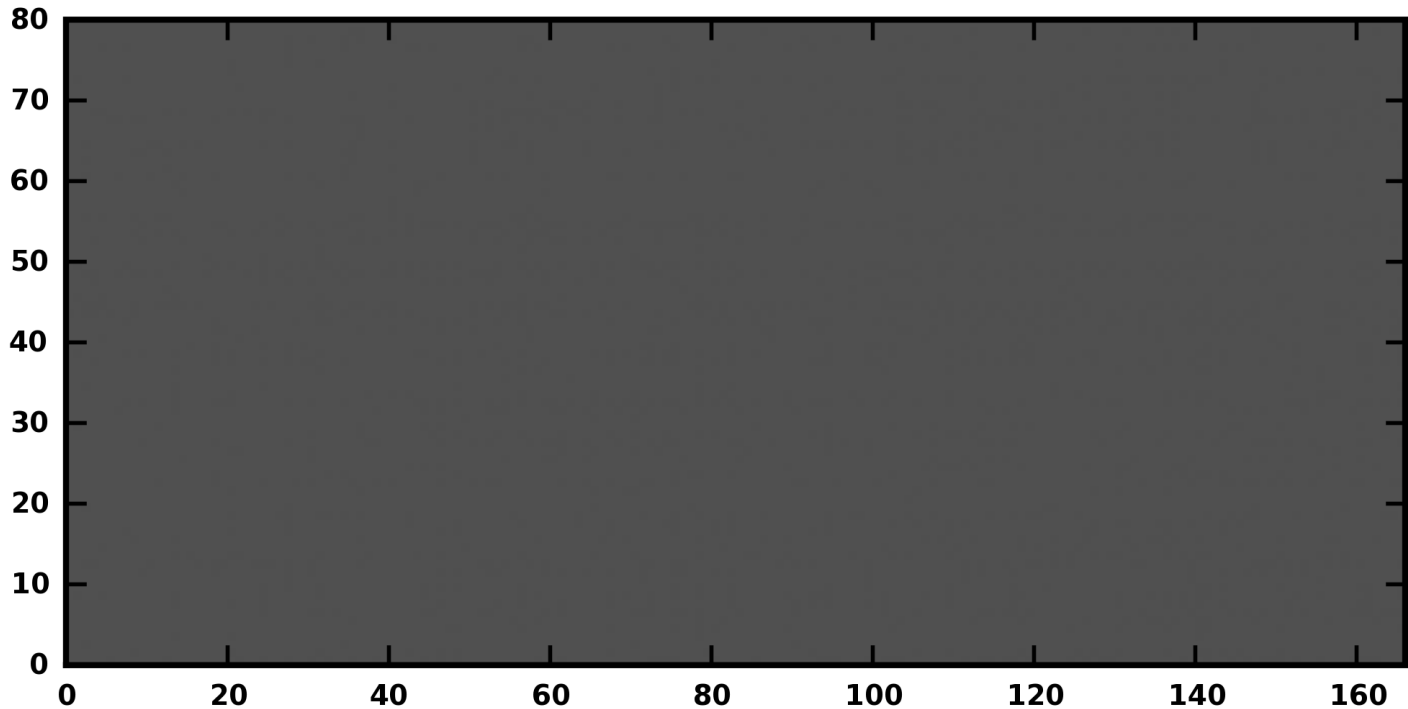


Input Range = 1V

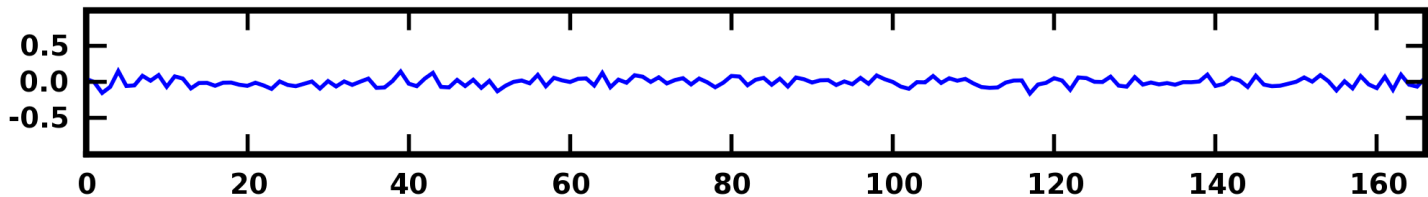


# Measured ADC Noise

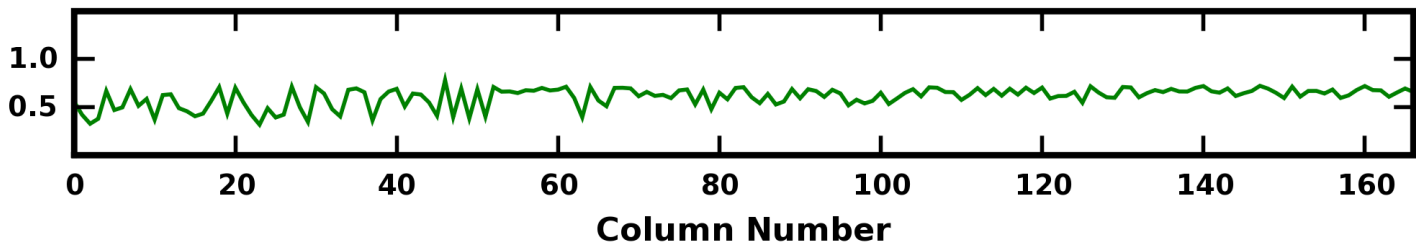
Image at  
constant  
ADC test  
input level



FPN  
(10-b LSBs)

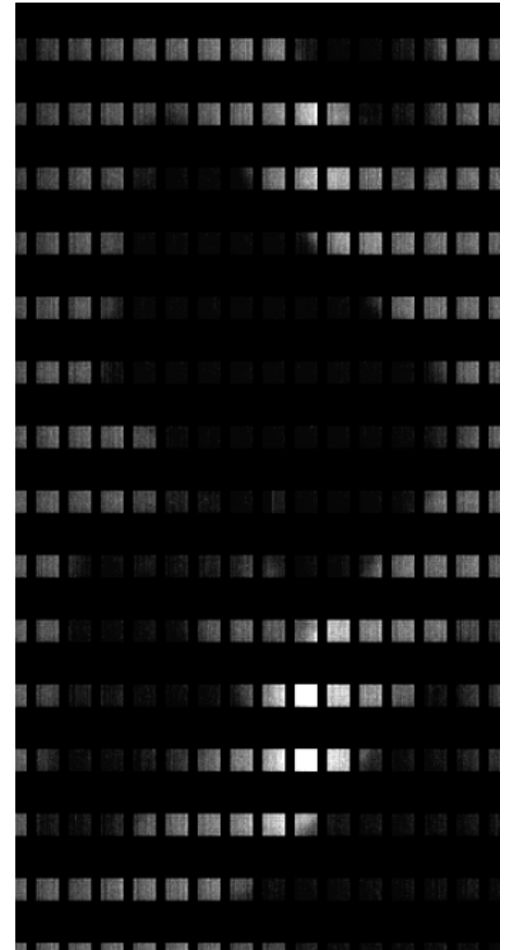
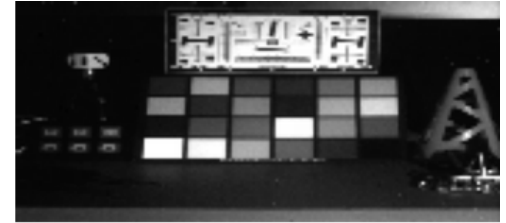


Temporal  
(10-b LSBs)



Column Number

# Sample Image



# Summary

- Designed and characterized the first integrated multi-aperture image sensor
- Achieved good imaging performance with  $0.7\mu\text{m}$  pixels
  - FT-CCD structure in deep submicron CMOS
  - Ripple charge transfer
- Extensible architecture well suited for ultra-high pixel count imagers
- Many potential applications or benefits
  - Depth
  - Close proximity imaging
  - Color imaging with good spectral separation
  - High defect tolerance
  - Relaxed external optical requirements
- Results suggest that further scaling while maintaining performance is possible

# Acknowledgements

- TSMC
  - The authors thank C.H. Tseng, David Yen, C.Y. Ko, J.C. Liu, Ming Li, and S.G. Wu for process customization and fabrication
- Hertz Foundation
  - Fellowship support for Keith Fife
- Lane Brooks, MIT EECS
  - Collaboration on the design of the testing platform and software system