A 0.5µm Pixel Frame-Transfer CCD Image Sensor in 110nm CMOS

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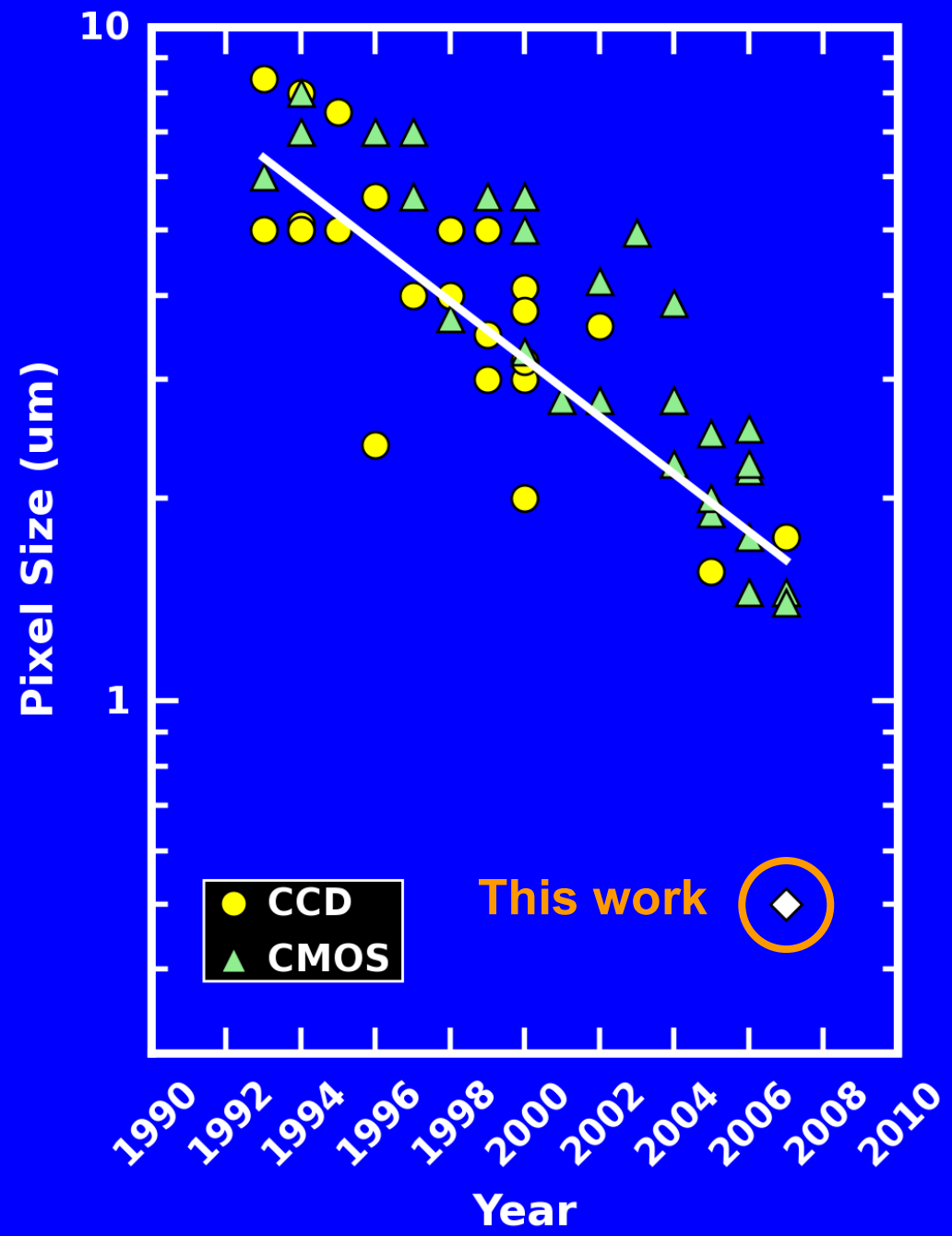
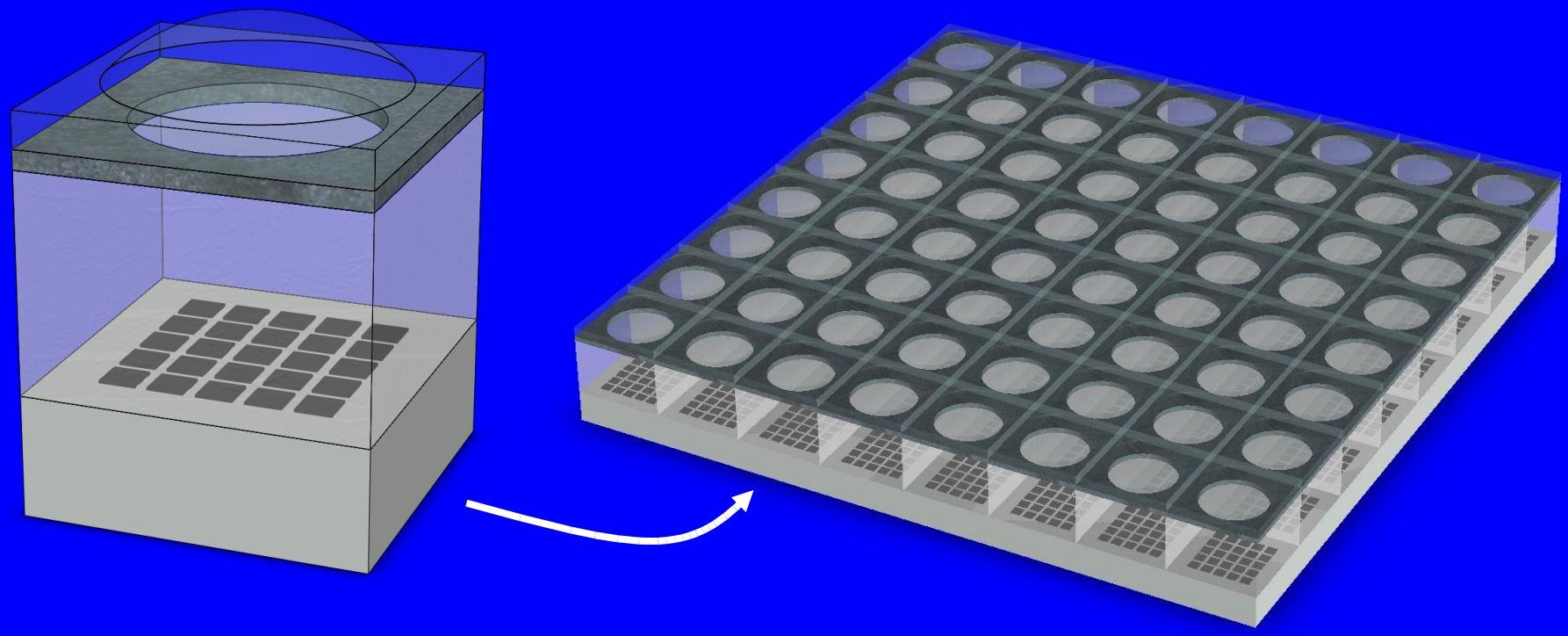
Pixel Scaling

- Increase spatial resolution
- Decrease format size



Pixel Sizes reported at IEDM, ISSCC, IISW

Image Sensor with Multiple Apertures

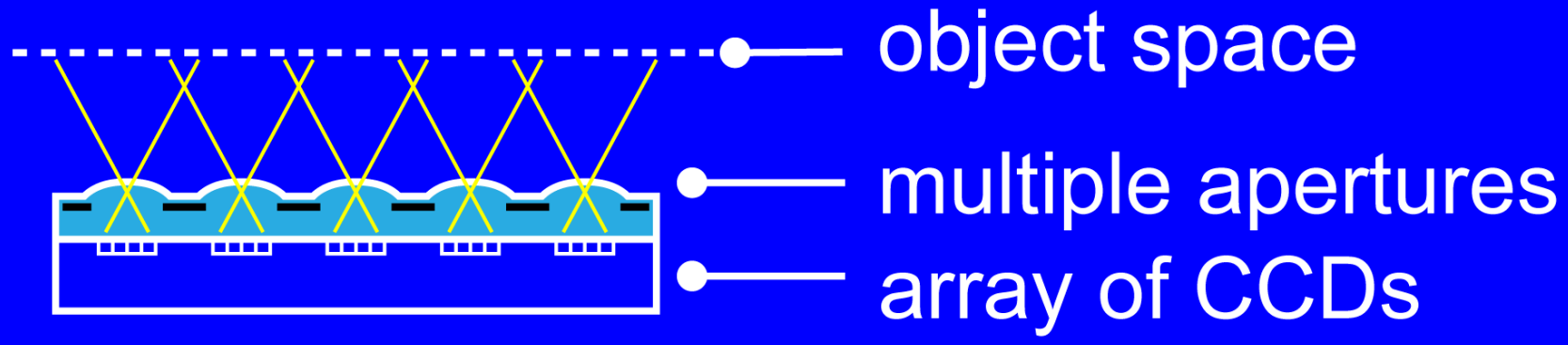


Small Image Sensor
with integrated optics

Small Image Sensors integrated
into large array

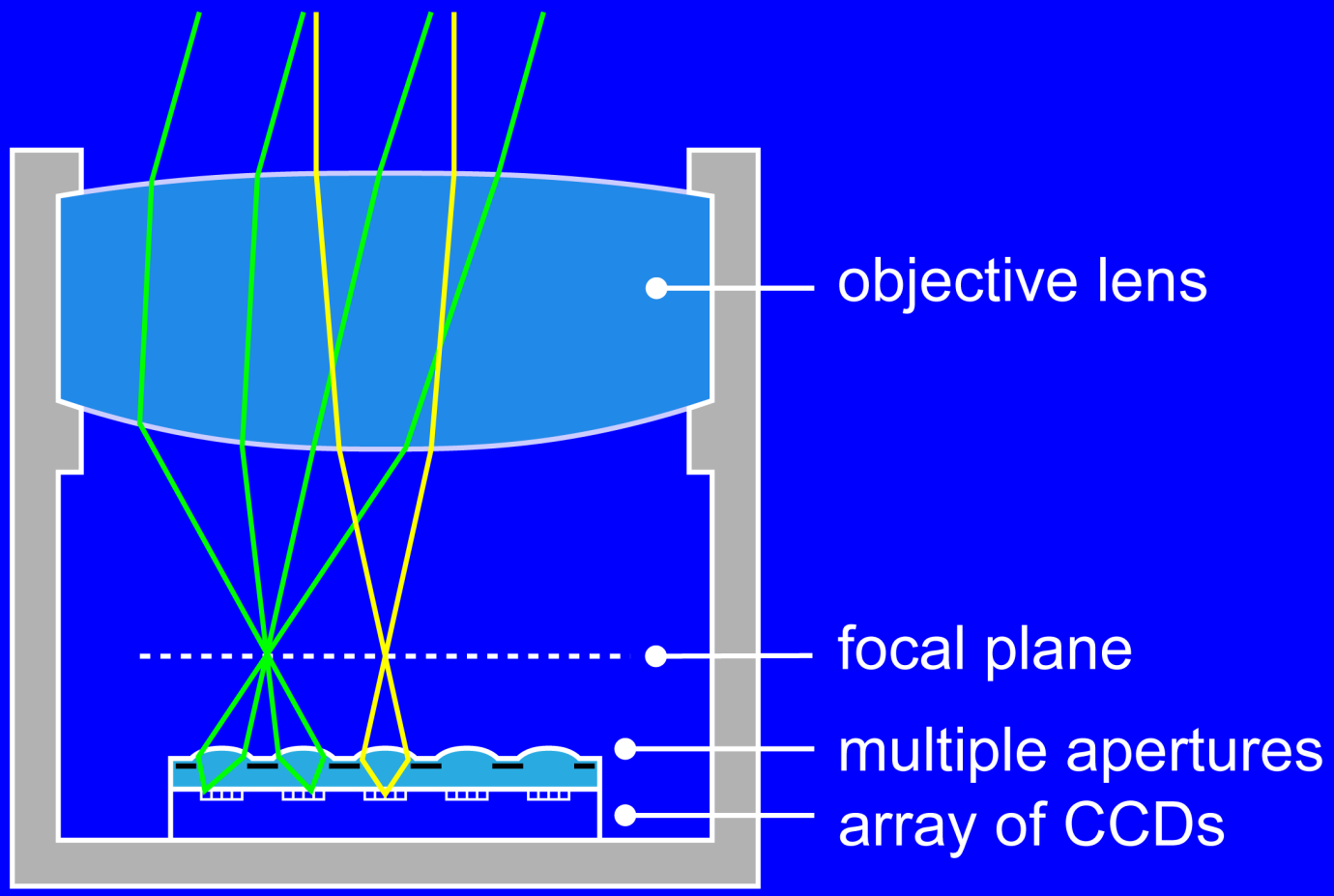
Multi-Aperture Imaging

- Object space in close proximity to image sensor
- Each array of pixels captures a portion of the object space
- Image is computationally reconstructed



Multi-Aperture with Objective Lens

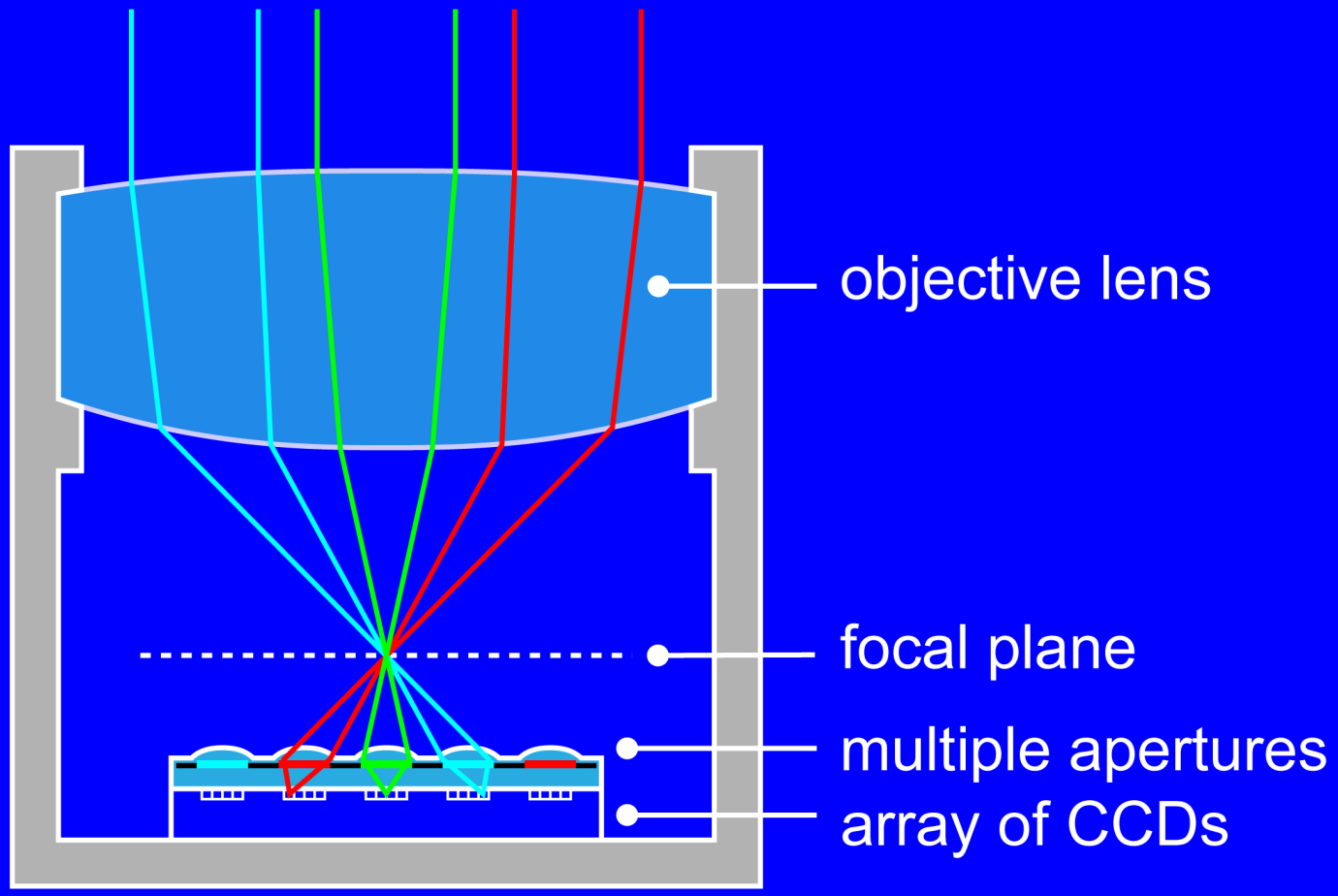
- 3D imaging
  - Stereoscopic views of focal plane



** K. Fife, A. El Gamal and H.-S. P. Wong, CICC 2006, p281-284*

Multi-Aperture for Color Separation

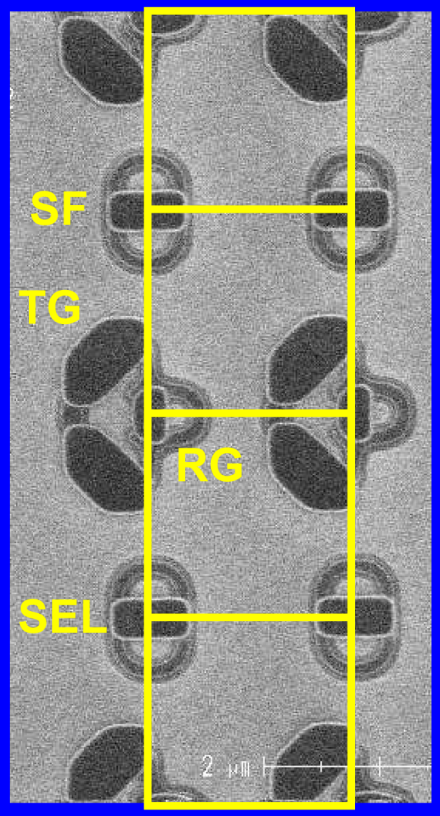
- Color separation by aperture
  - Improve crosstalk
  - Reduce color aliasing

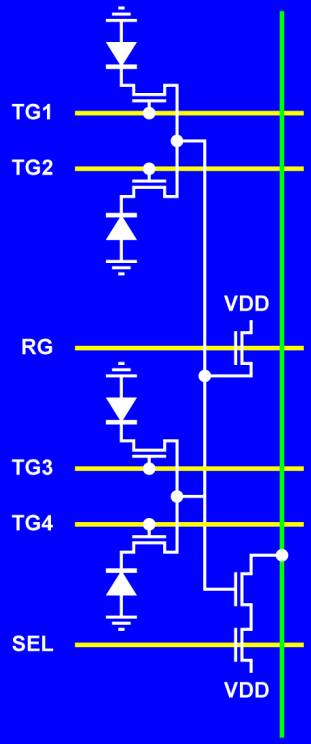


** K. Fife, A. El Gamal and H.-S. P. Wong, CICC 2006, p281-284*

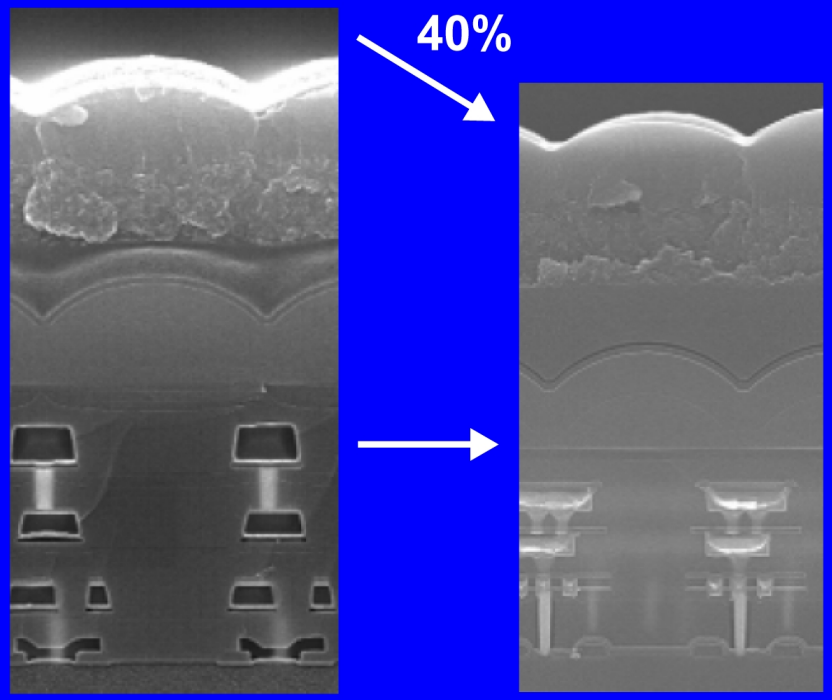
Recent Pixel Scaling

4T sharing





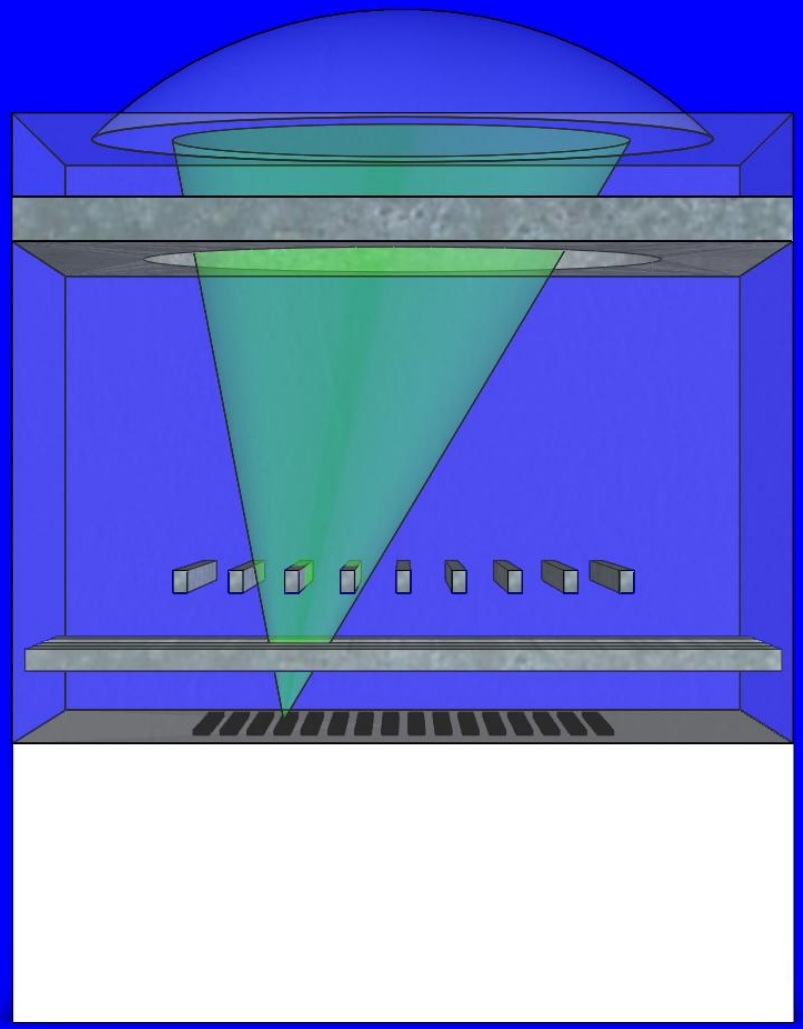
Stack height reduction



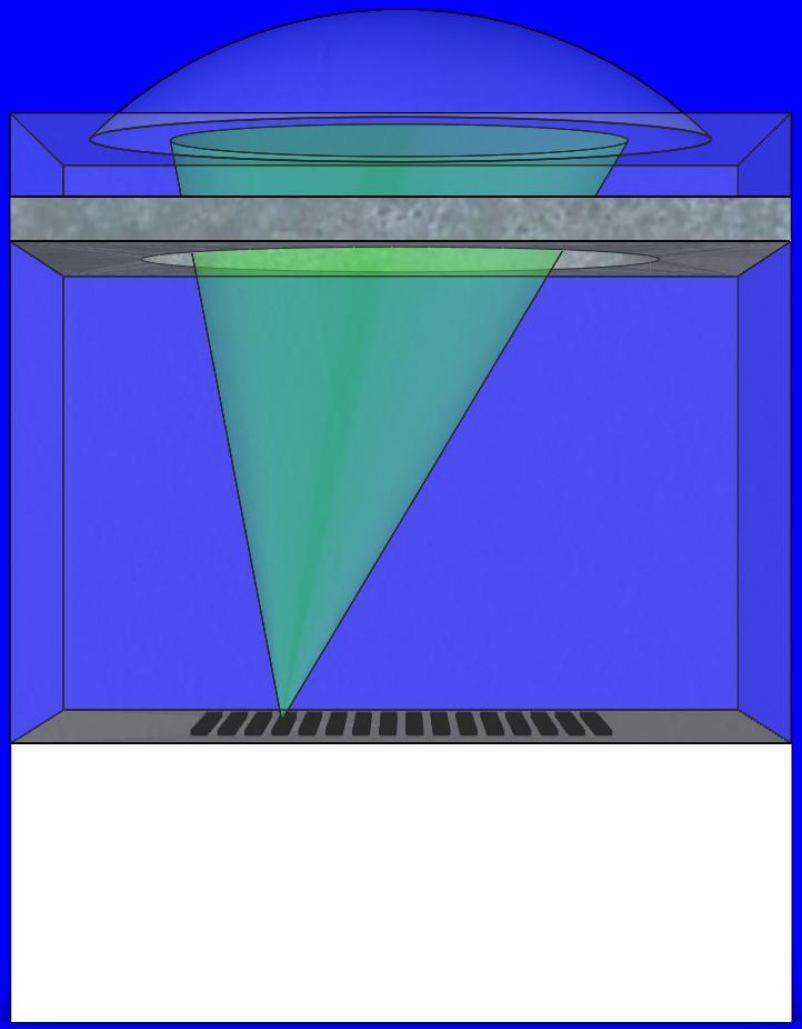
** J. Kim, J. Shin, C.R. Moon, et. al., IEDM 2006, p123-126*

** H. Sumi, IEDM 2006, p119-122*

Optical Stack



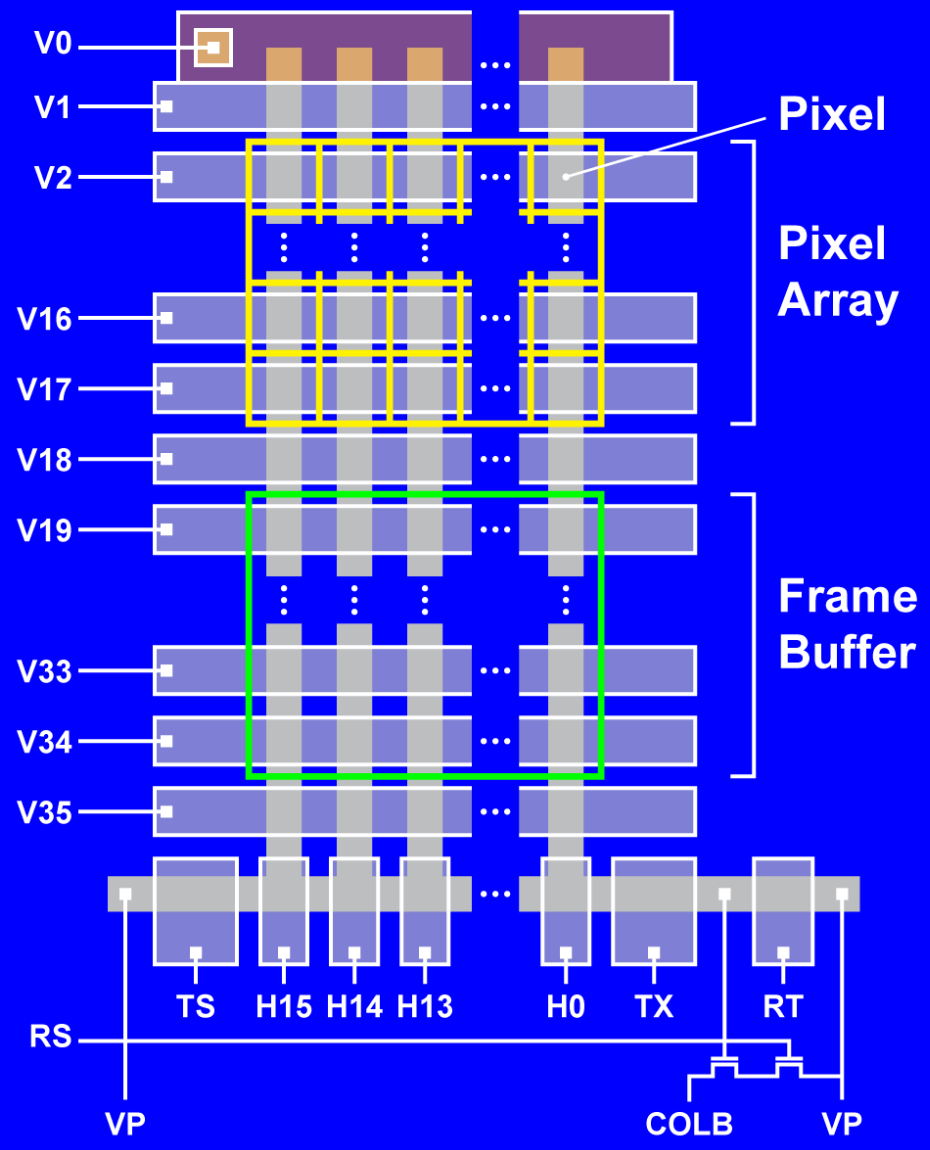
Metal wire occlusions



Metal free

FT-CCD Architecture

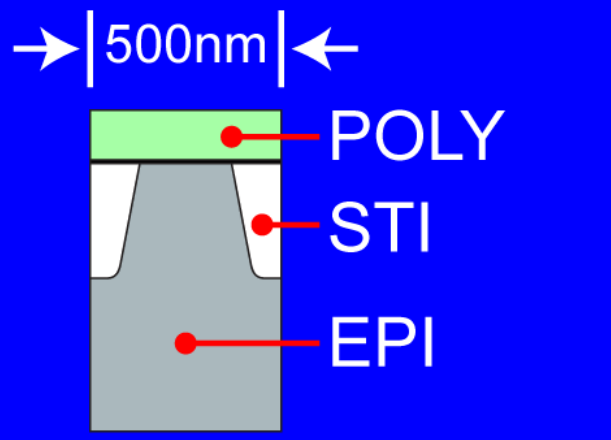
- 16 x 16 Pixel Array
- 16 x 16 Frame Buffer
- 16 stage H-CCD
- Floating diffusion with source follower readout



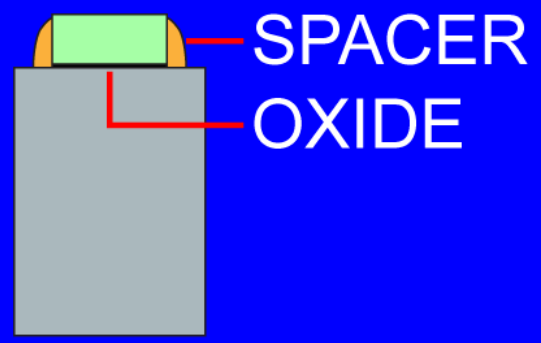
Outline

- Design and Fabrication
- Operation
- Characterization
- Scaling Issues
- Conclusion

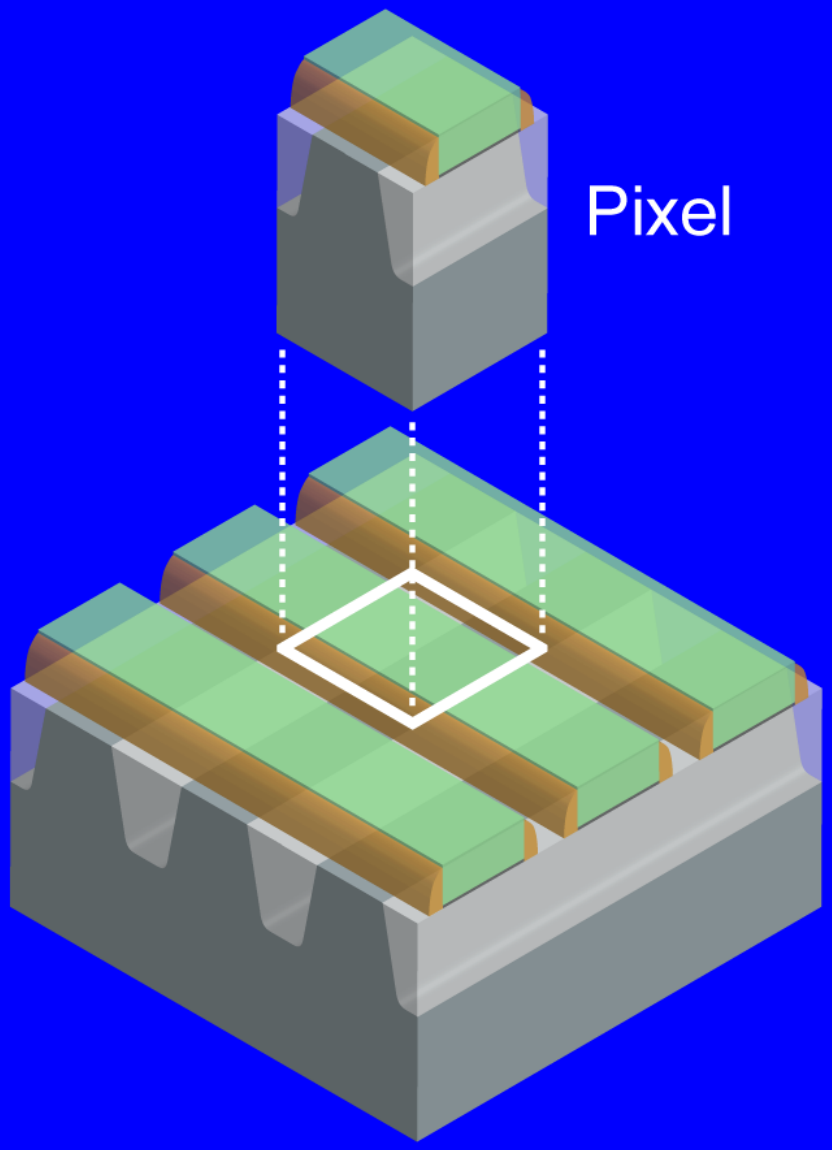
The 0.5µm Pixel



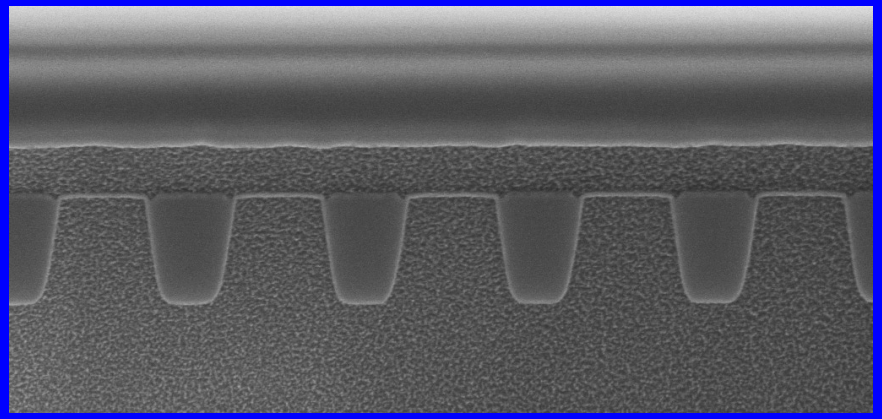
Across Channel



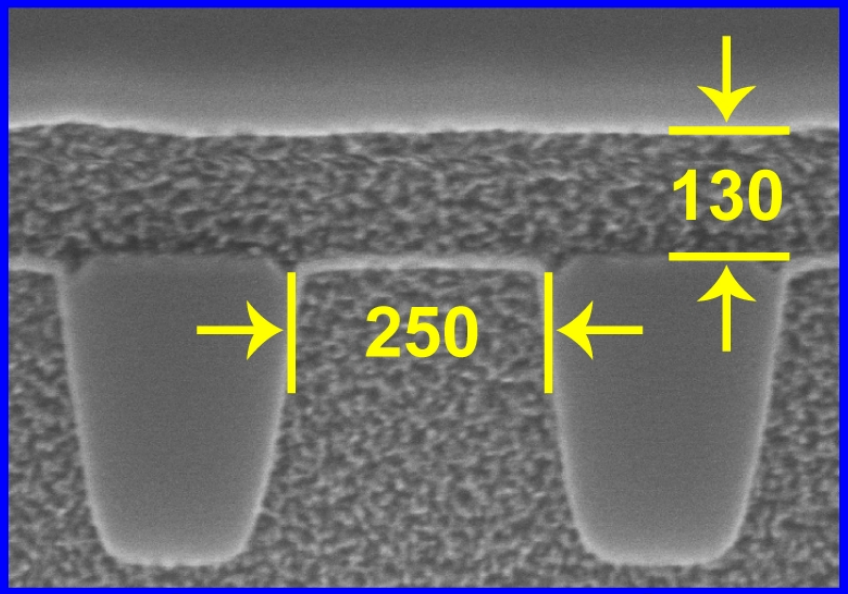
Along Channel



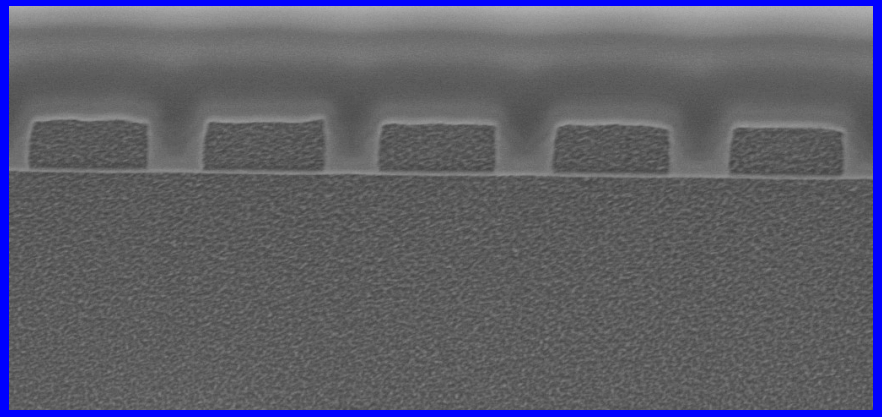
CCD Structure



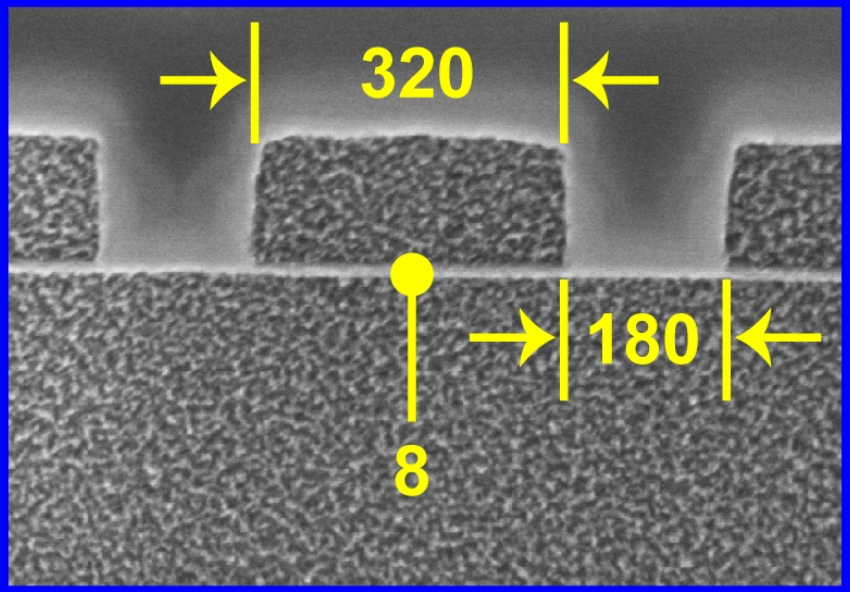
STI forms the channel stop



500 (nm)

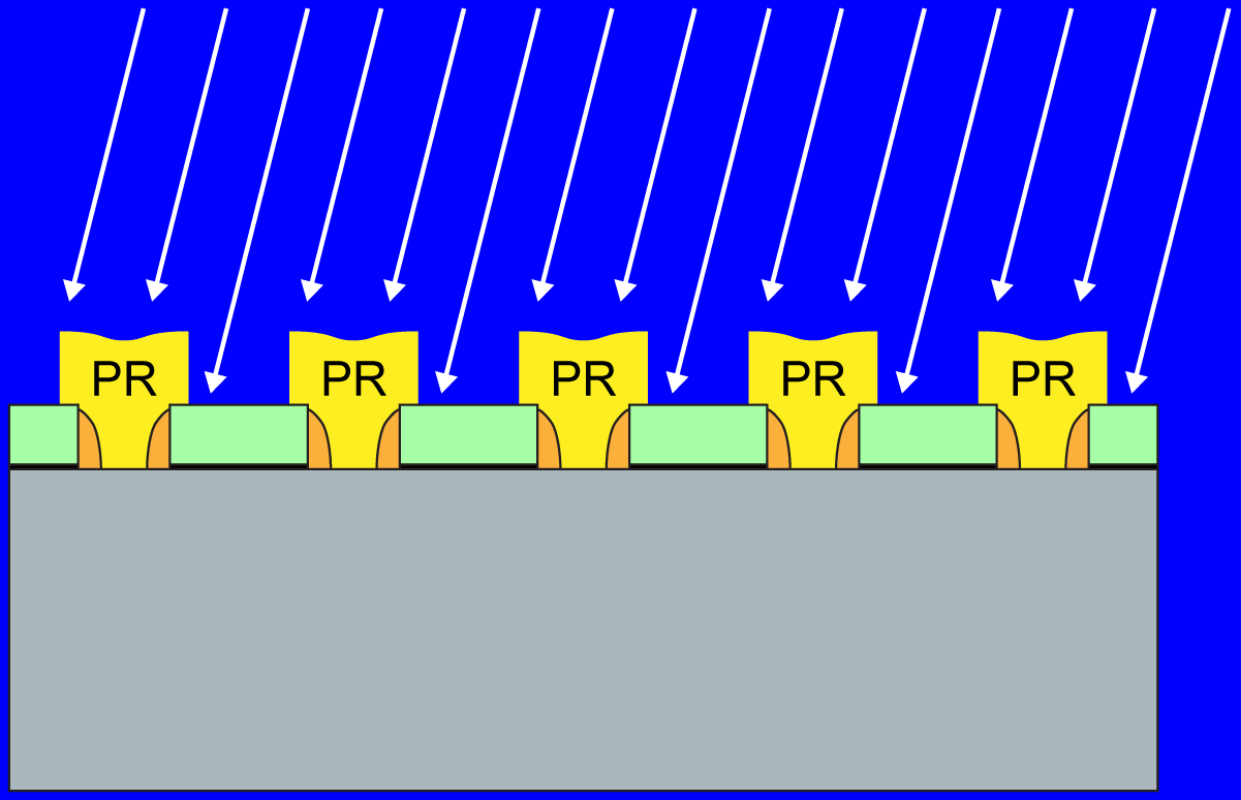


Single-level poly electrodes



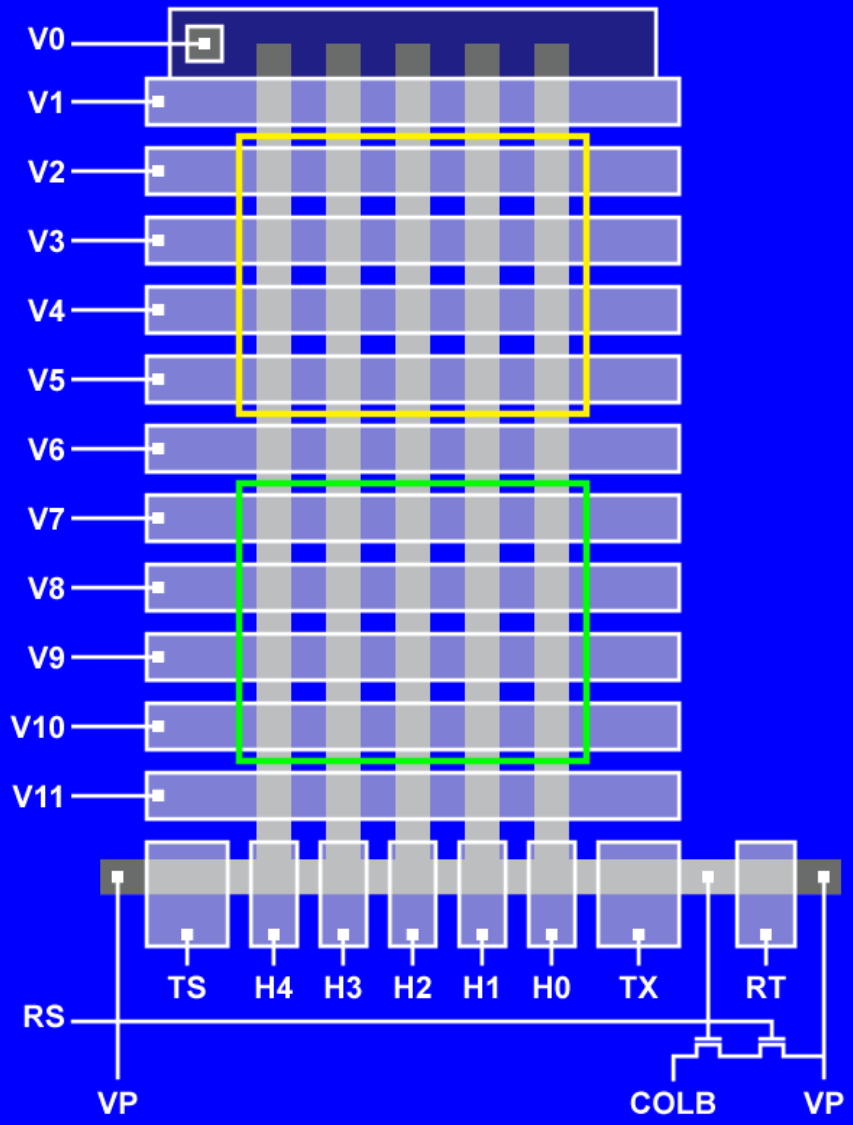
CMOS Fabrication

- S/D Implant mask is used to avoid dopant between electrodes (not self-aligned)

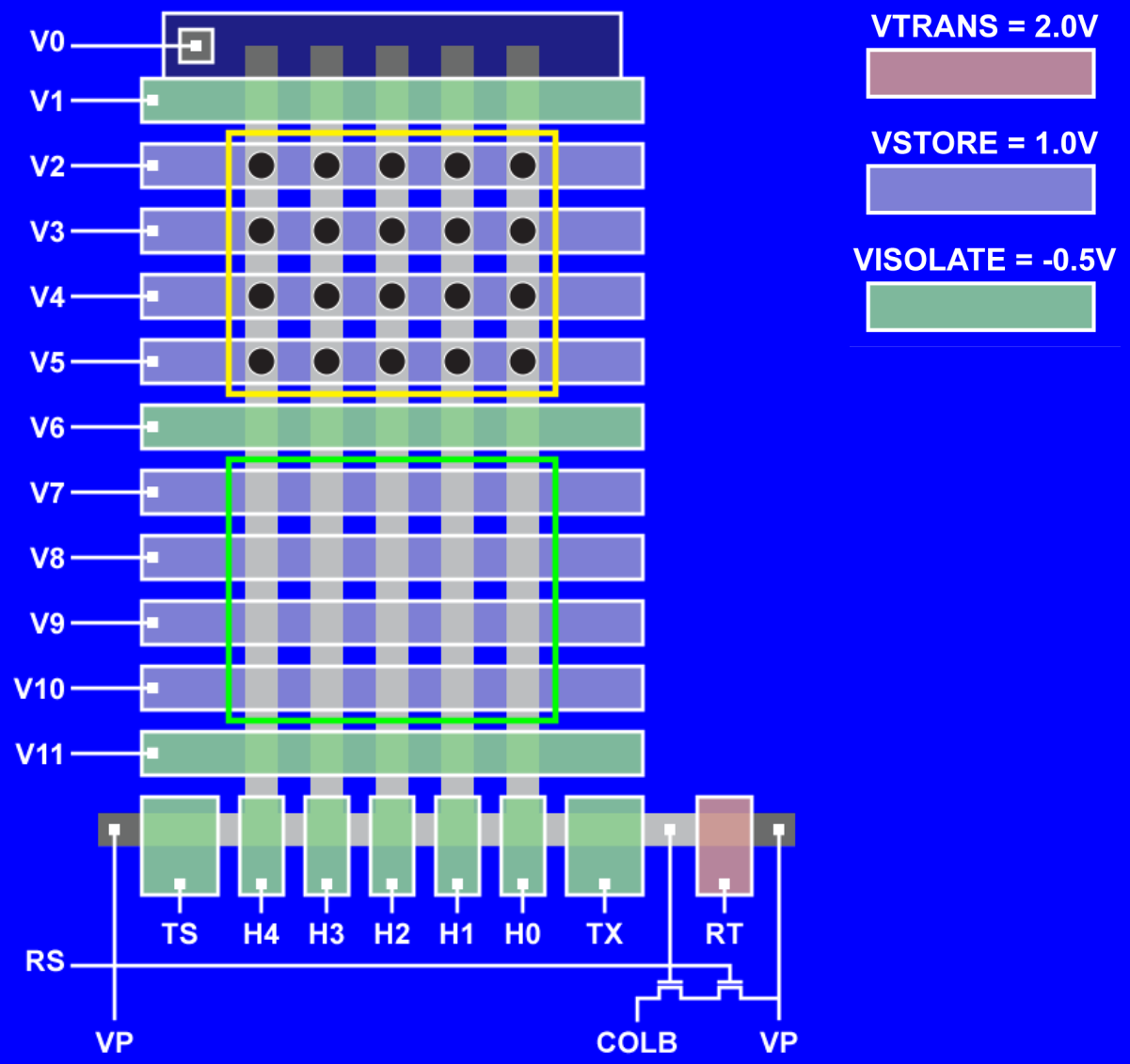


Operation

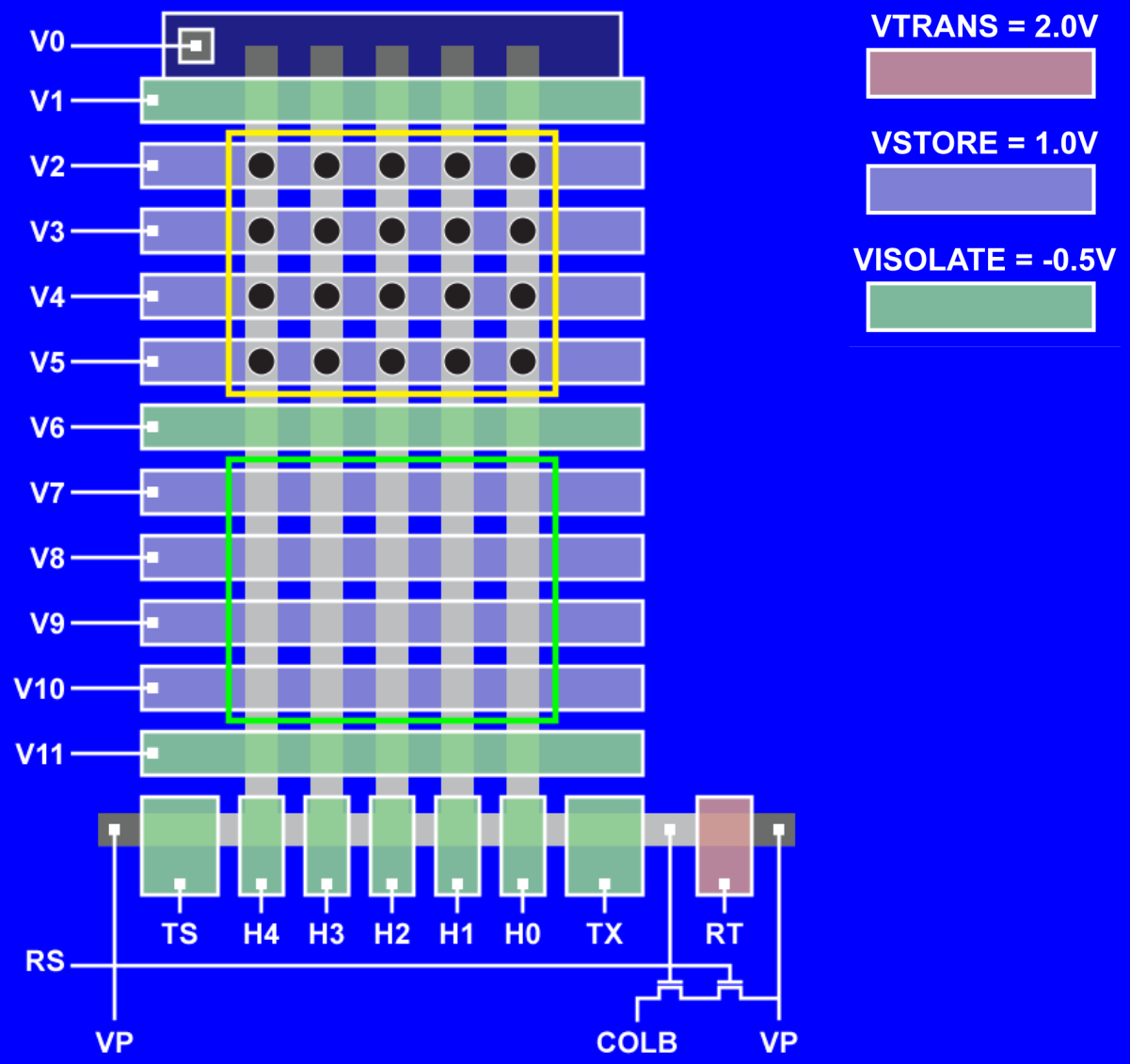
- **Flush**
  - Initial charge depletion
- **Integrate**
  - Pixel region collects charge
- **Buffer Transfer**
  - charge shifted to shielded region
- **Horizontal Readout**
  - Charge shifted to H-CCD followed by sampling on floating diffusion



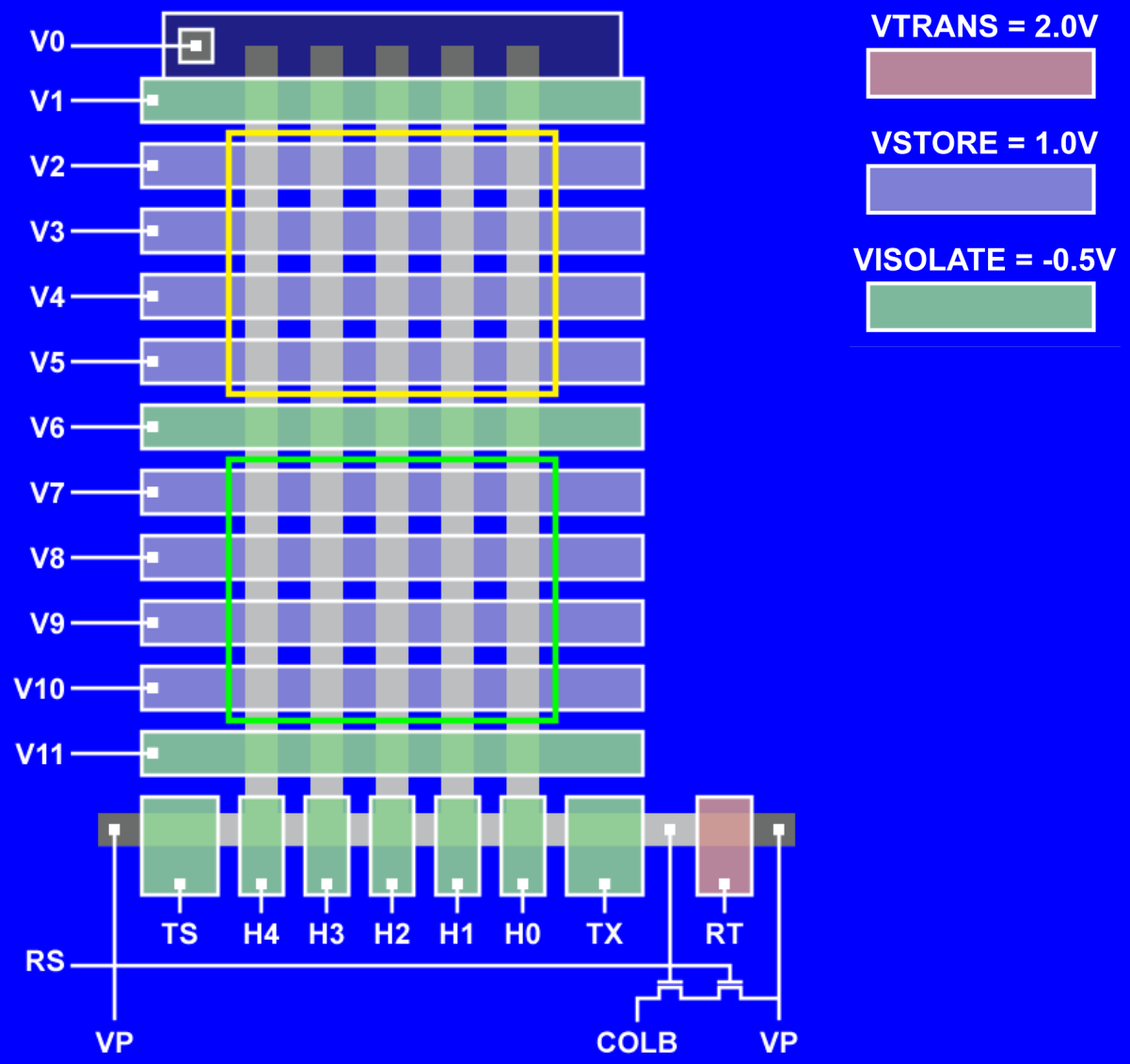
Operation (Flush)



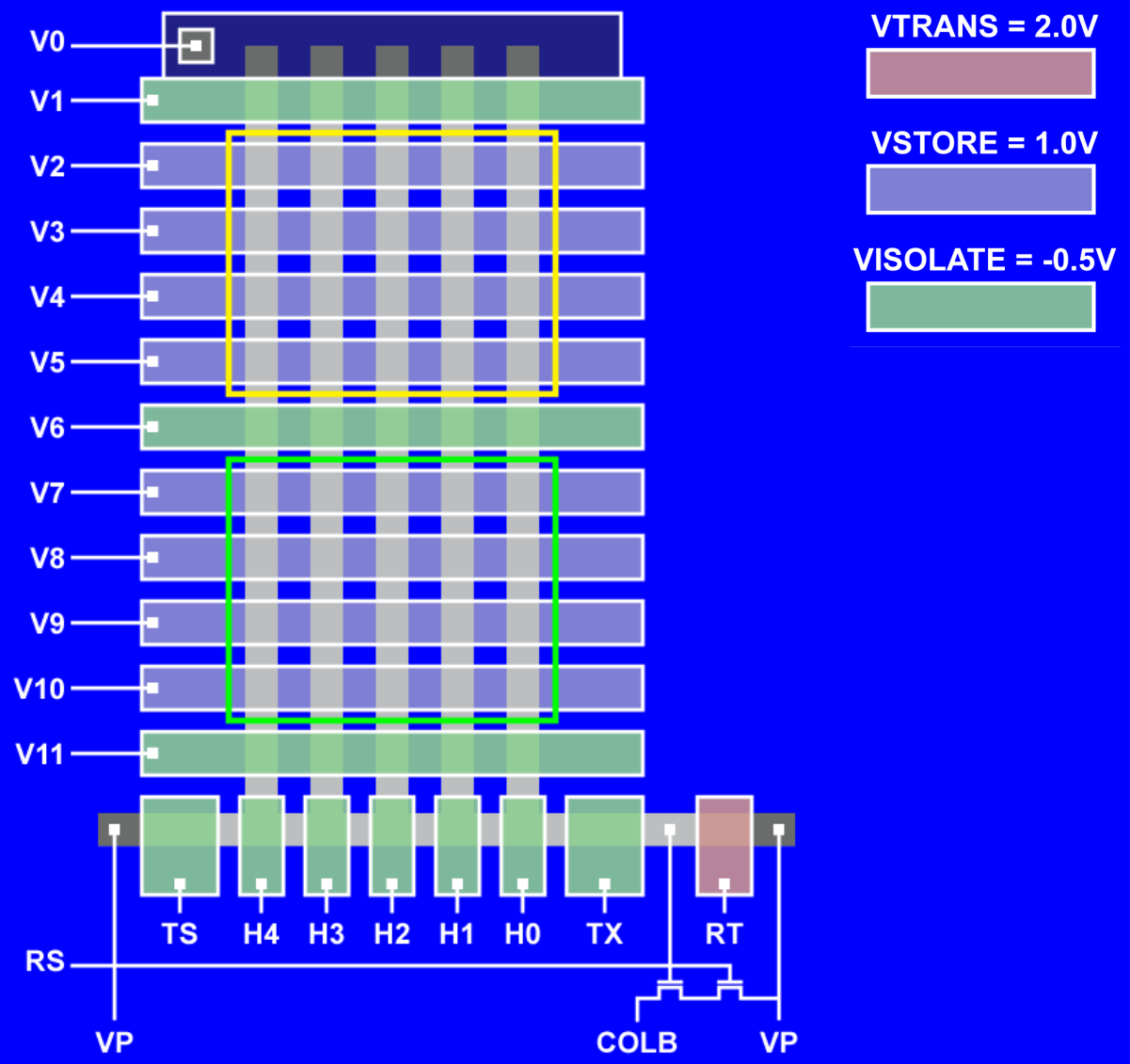
Operation (Flush)



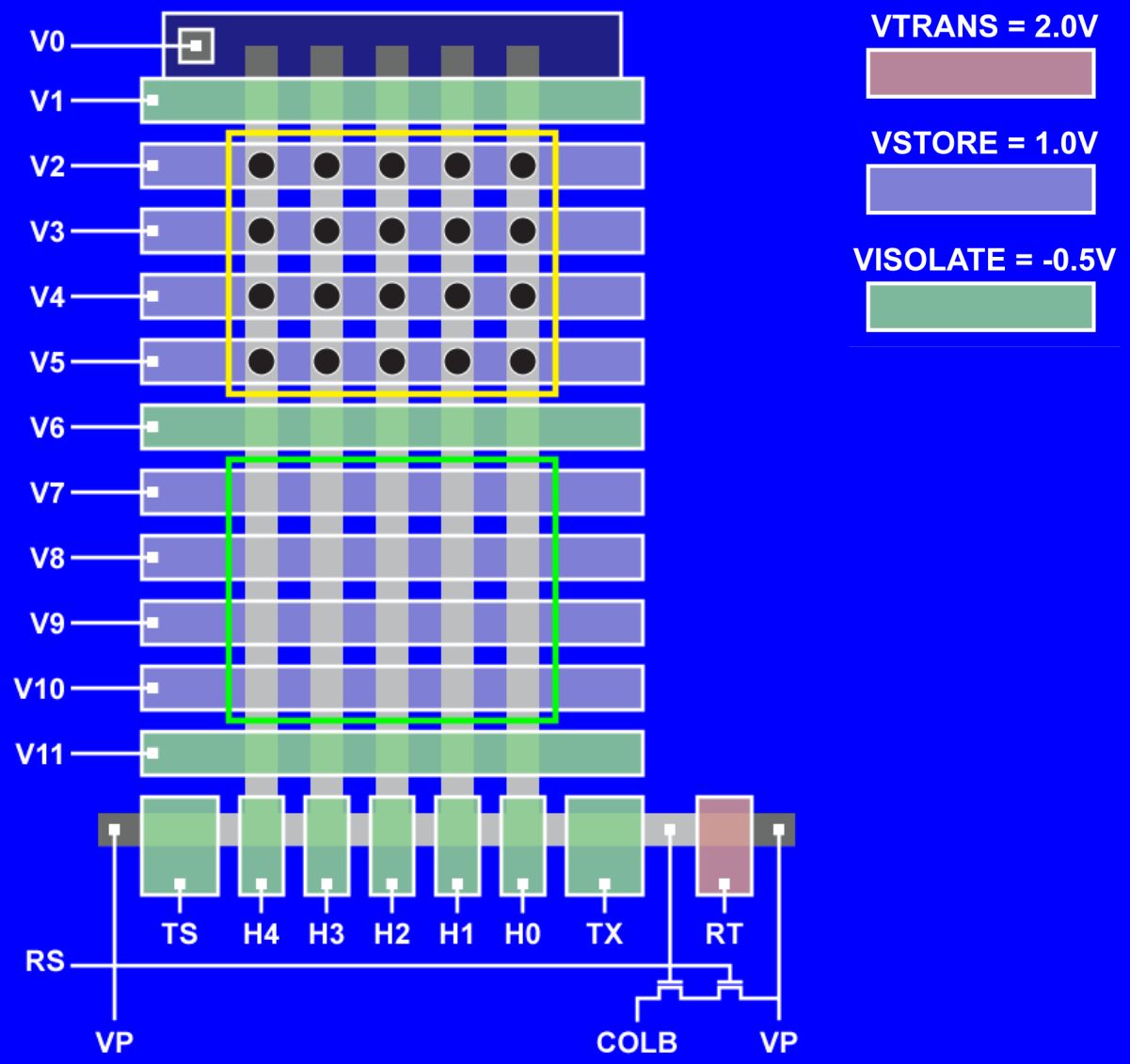
Operation (Integrate)



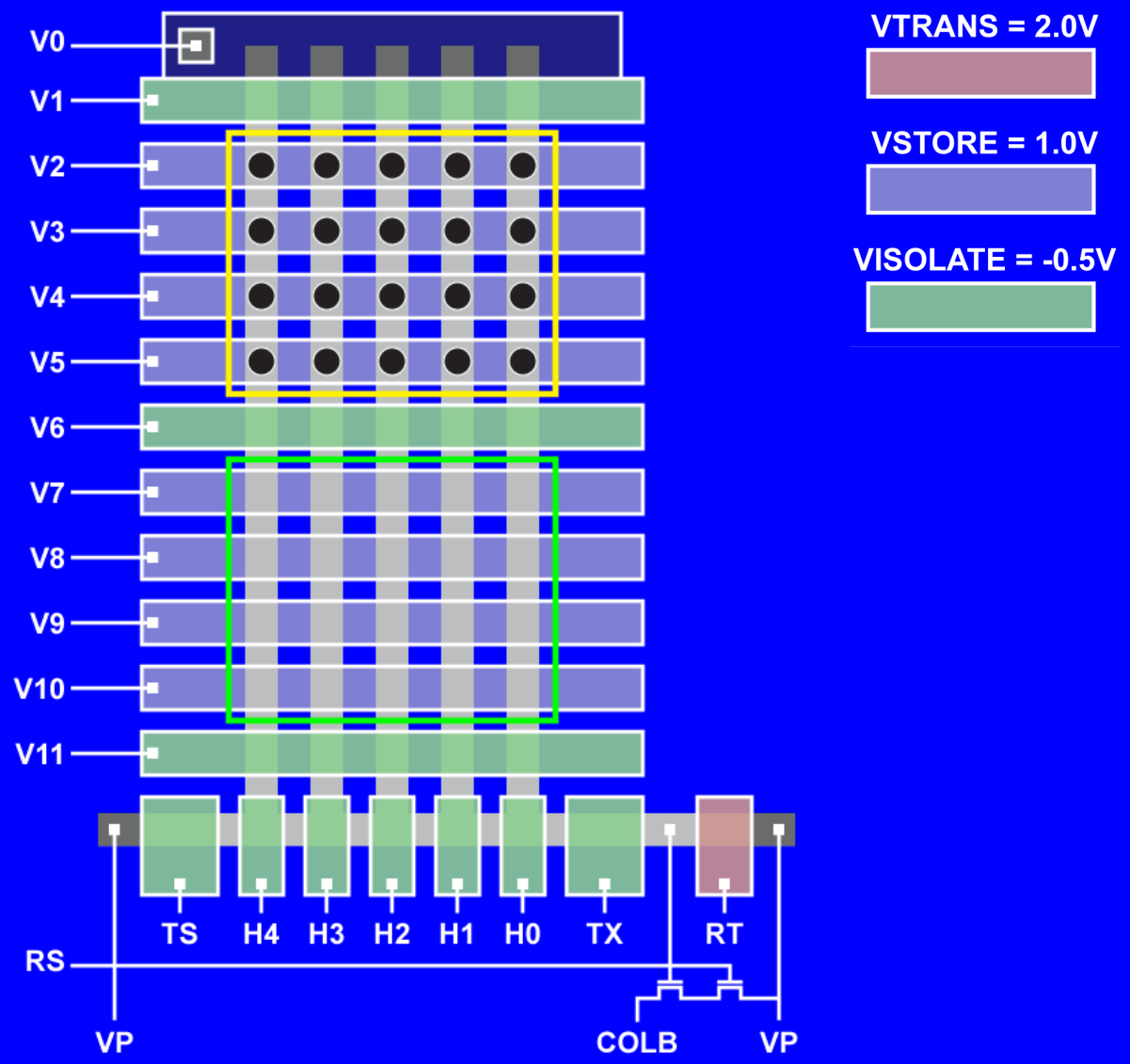
Operation (Integrate)



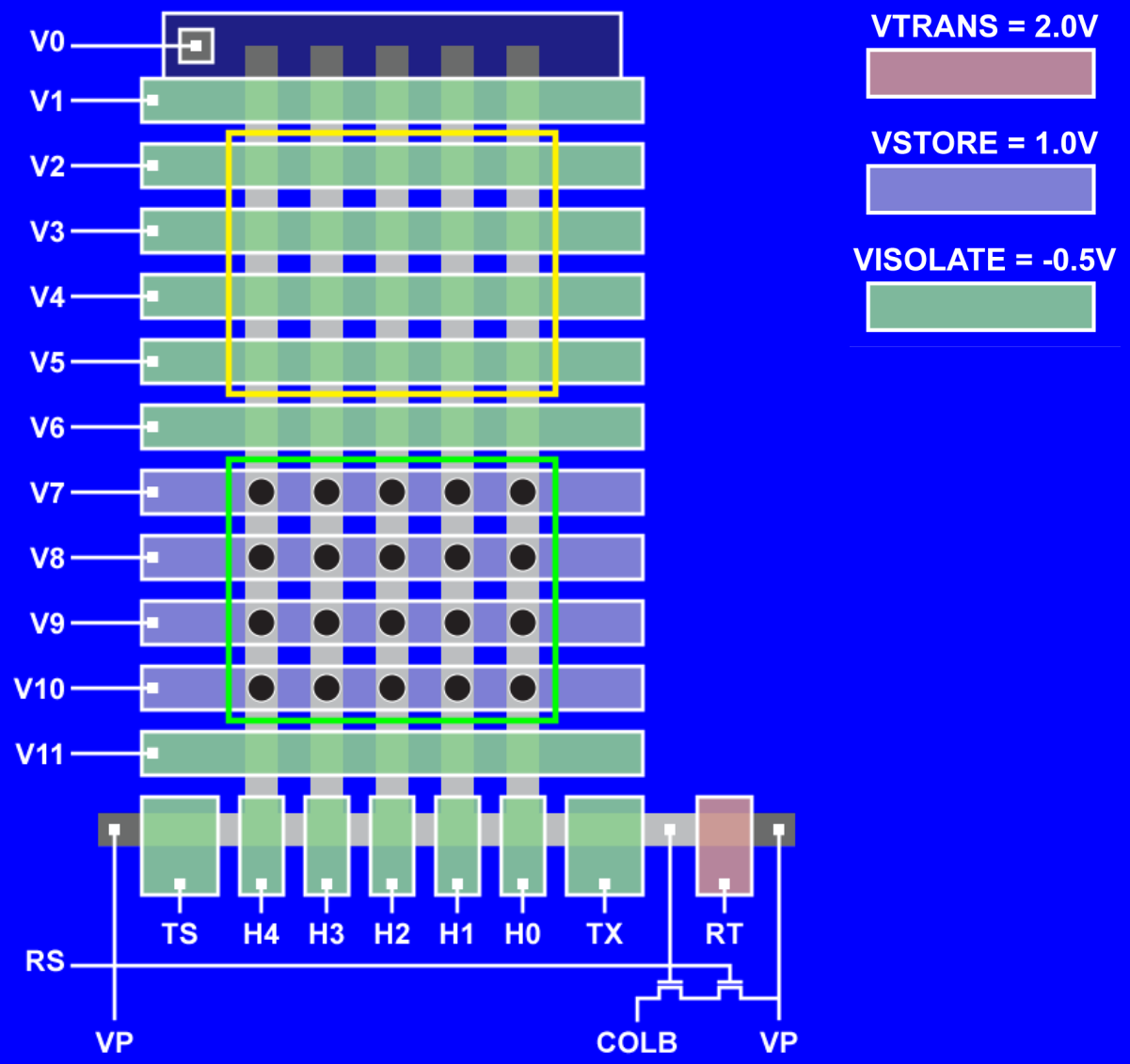
Operation (Buffer Transfer)



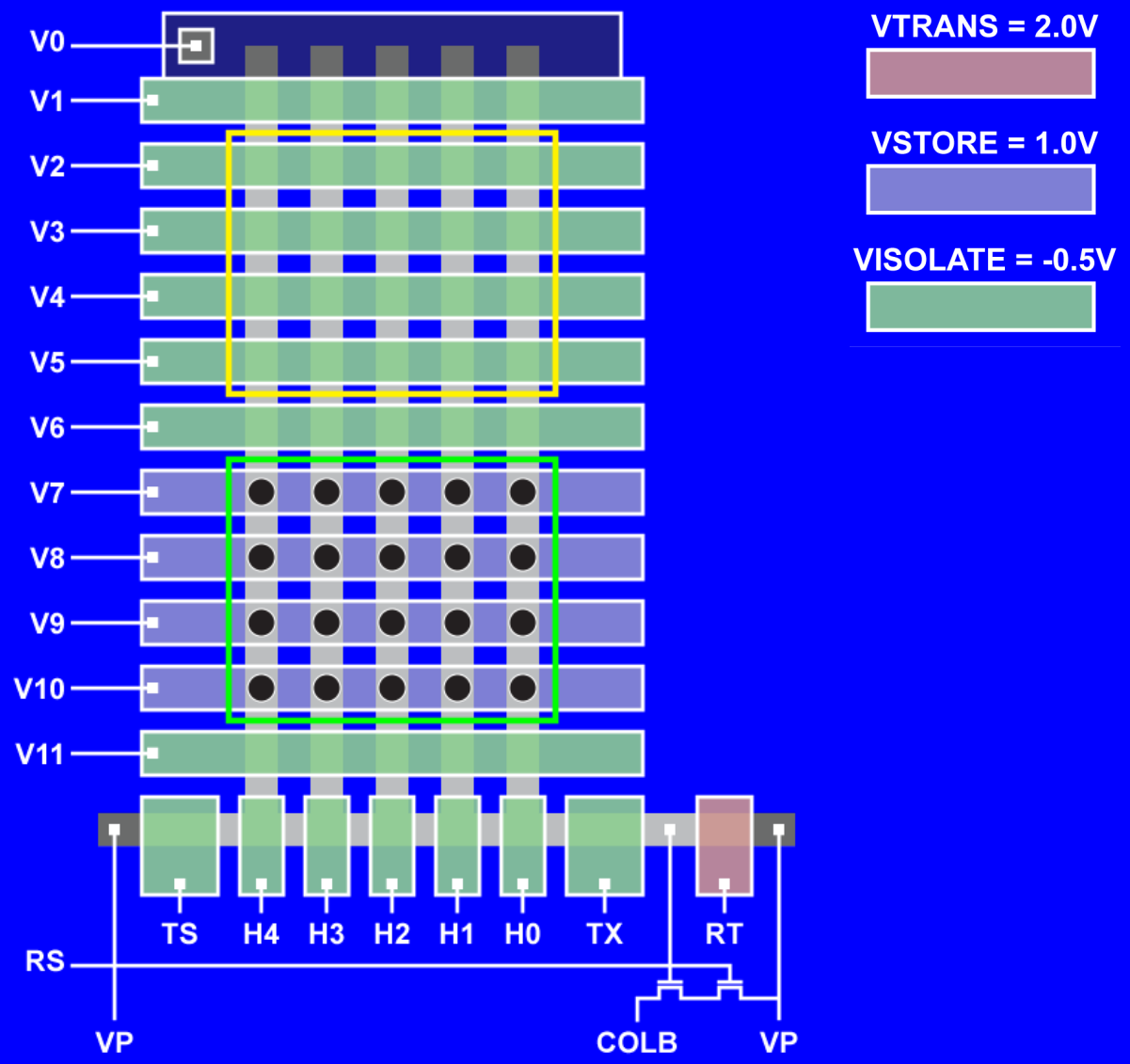
Operation (Buffer Transfer)



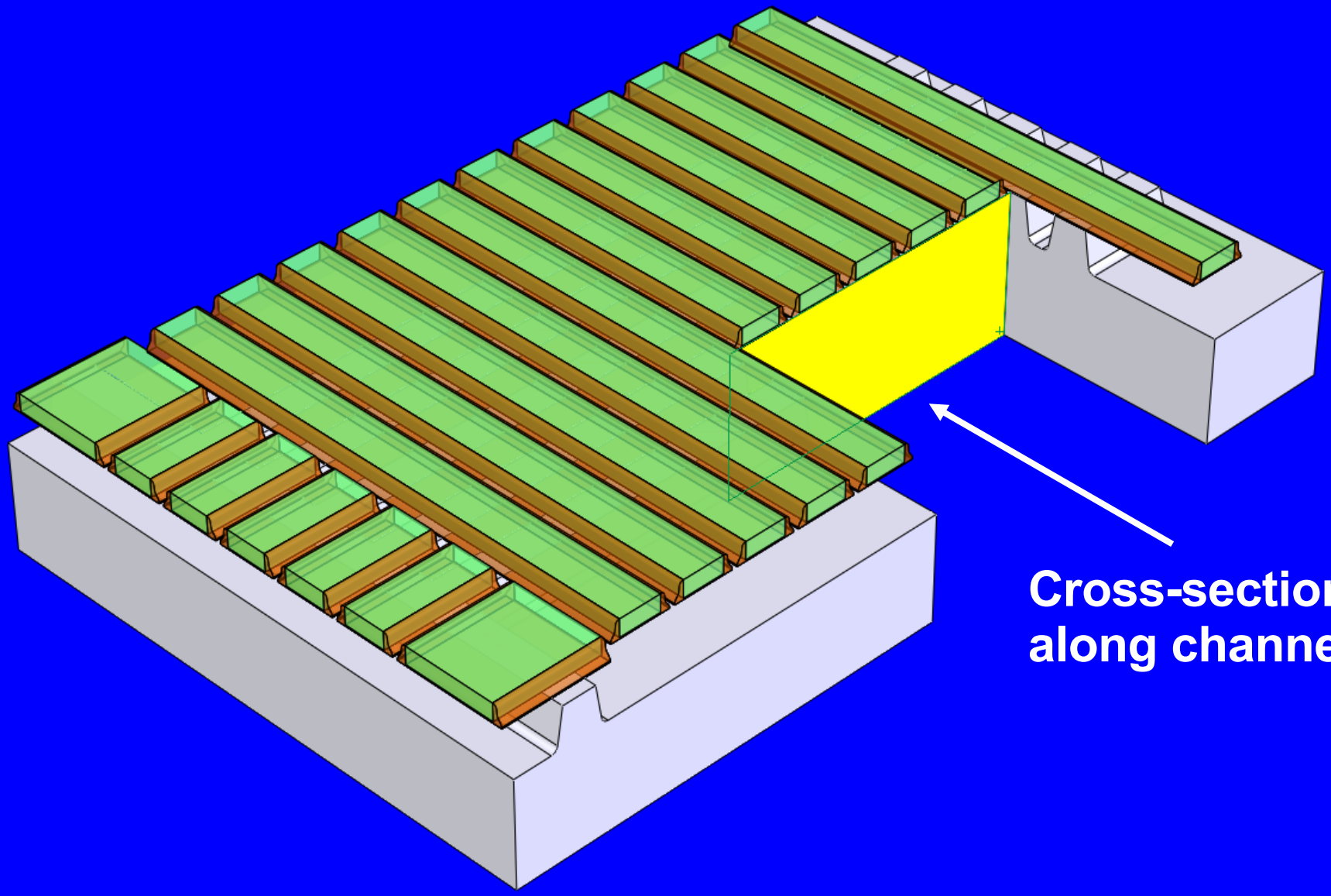
Operation (Horizontal Transfer)



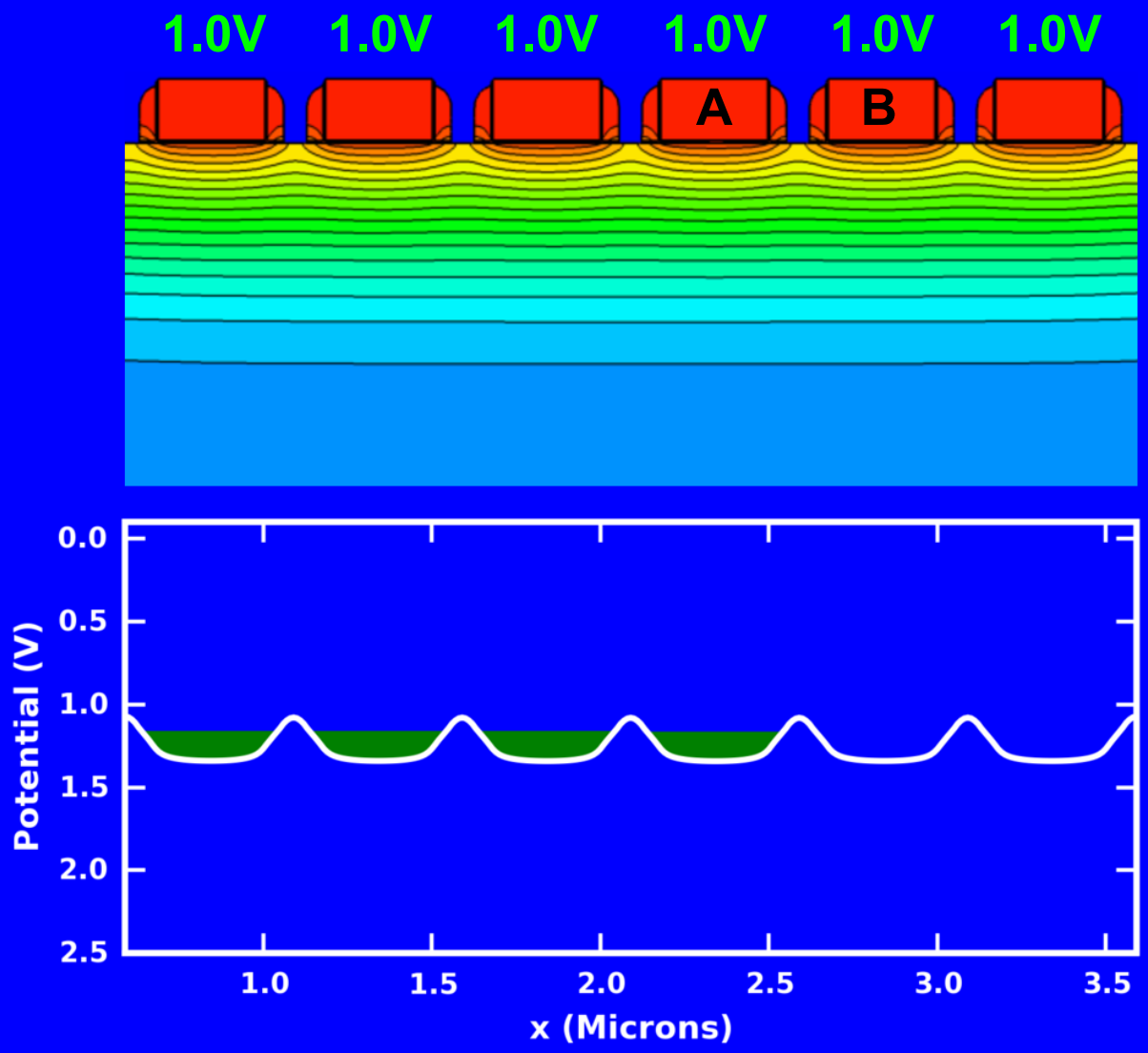
Operation (Horizontal Transfer)



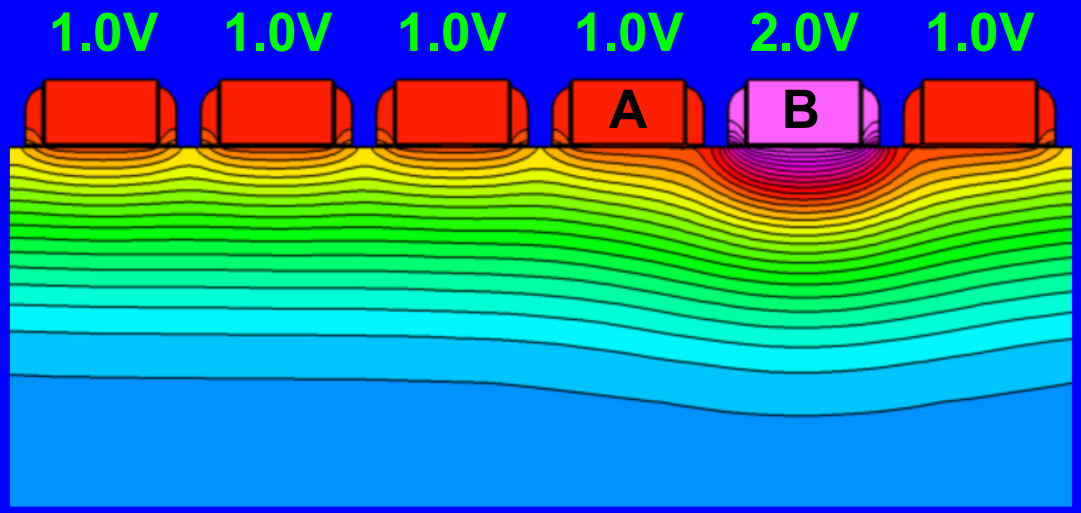
Simulation Along Channel

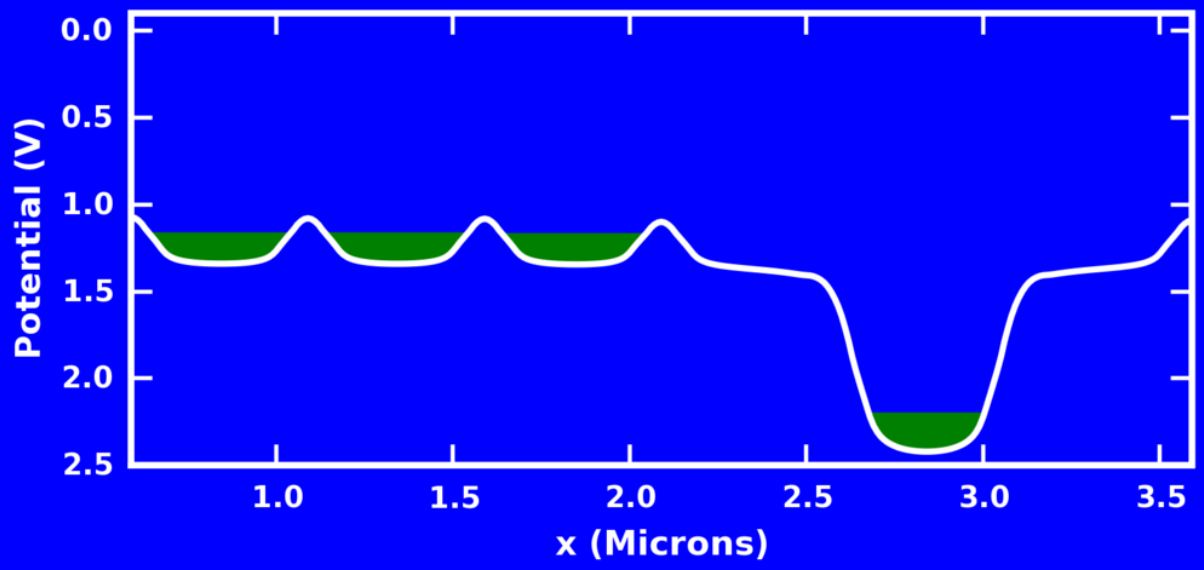


Potential Profile Along Channel

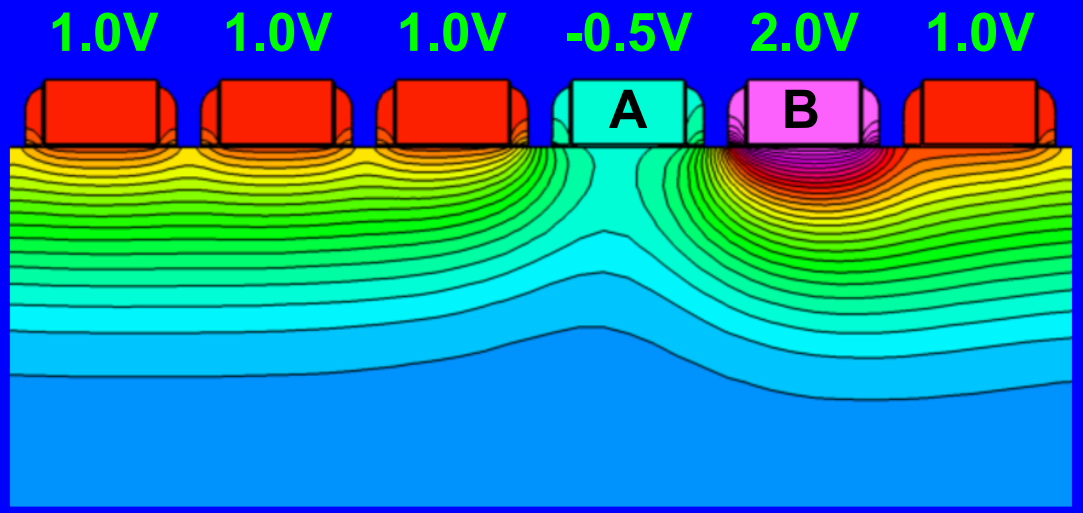


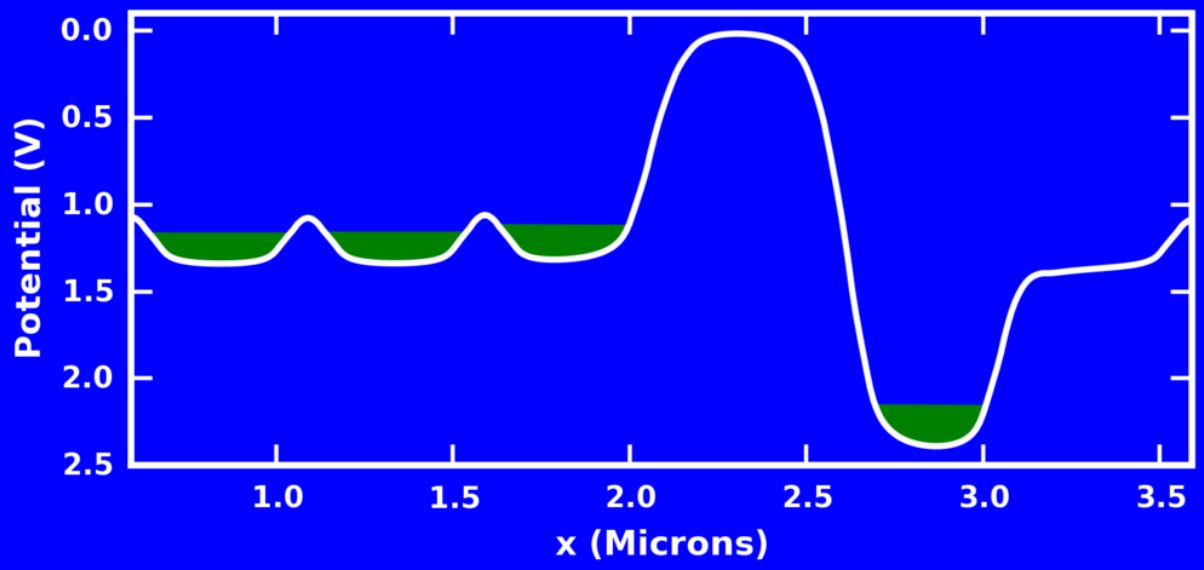
Potential Profile Along Channel



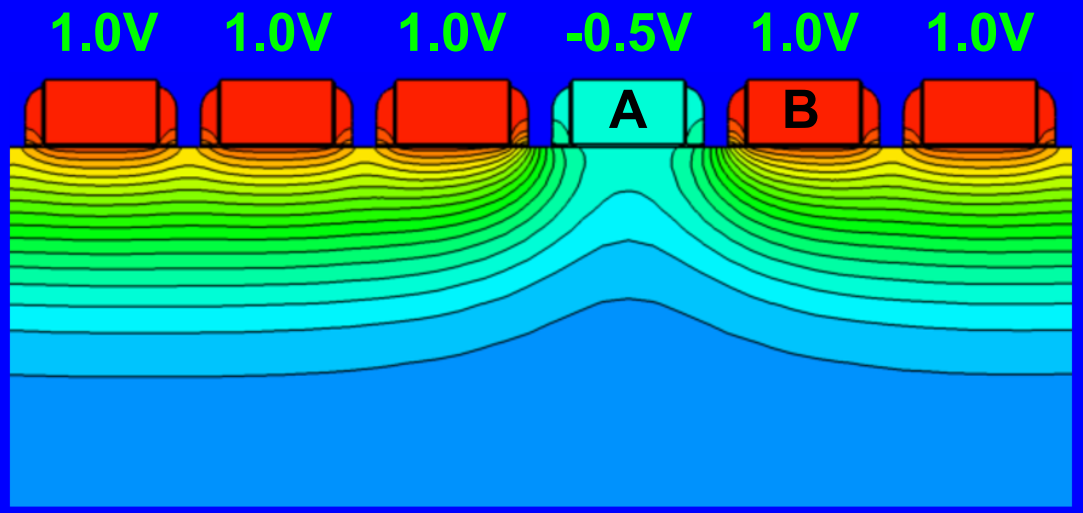


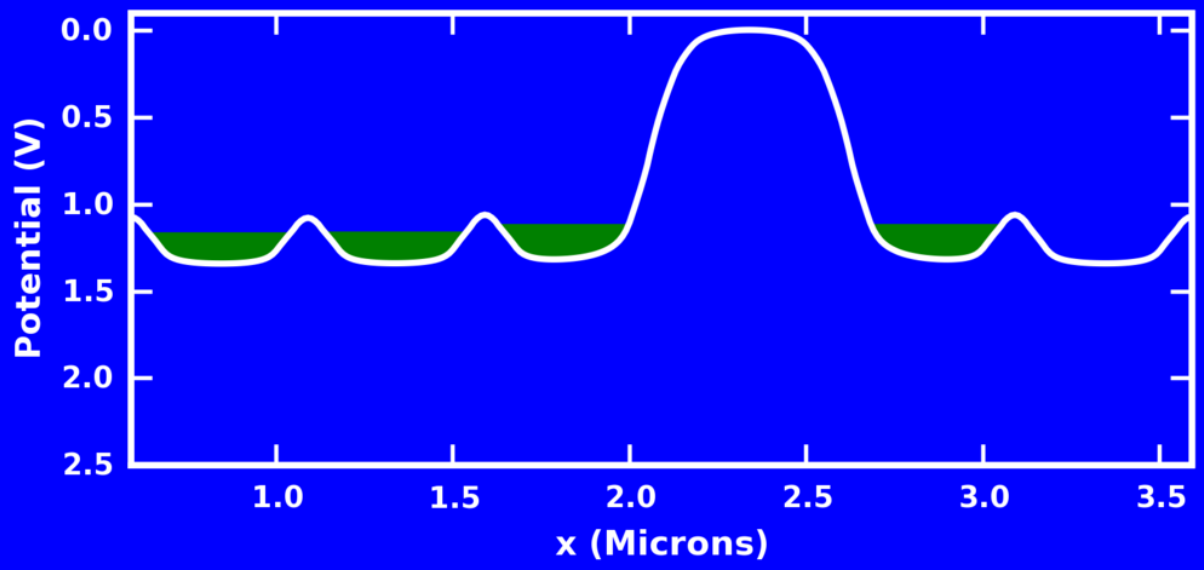
Potential Profile Along Channel



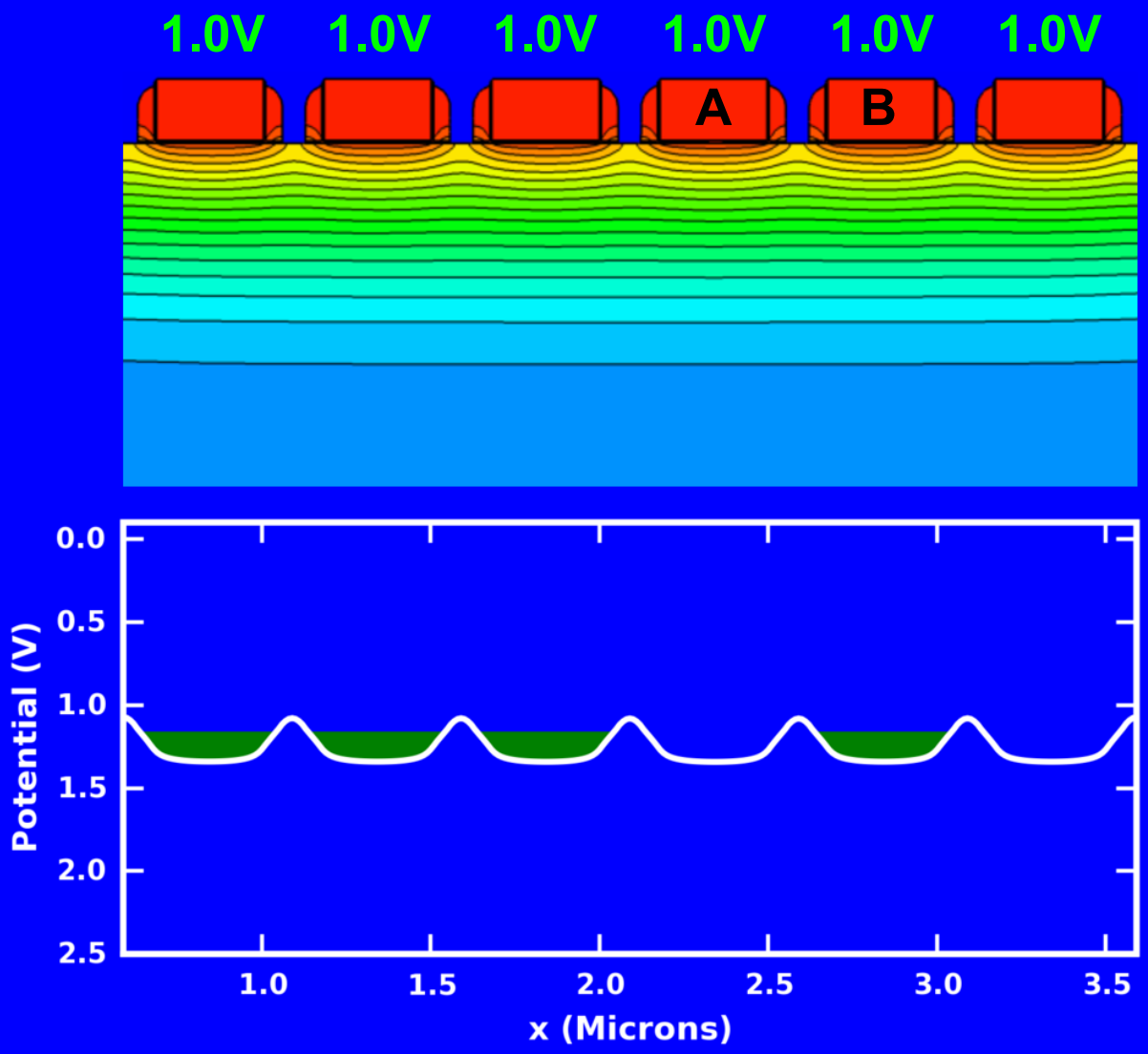


Potential Profile Along Channel



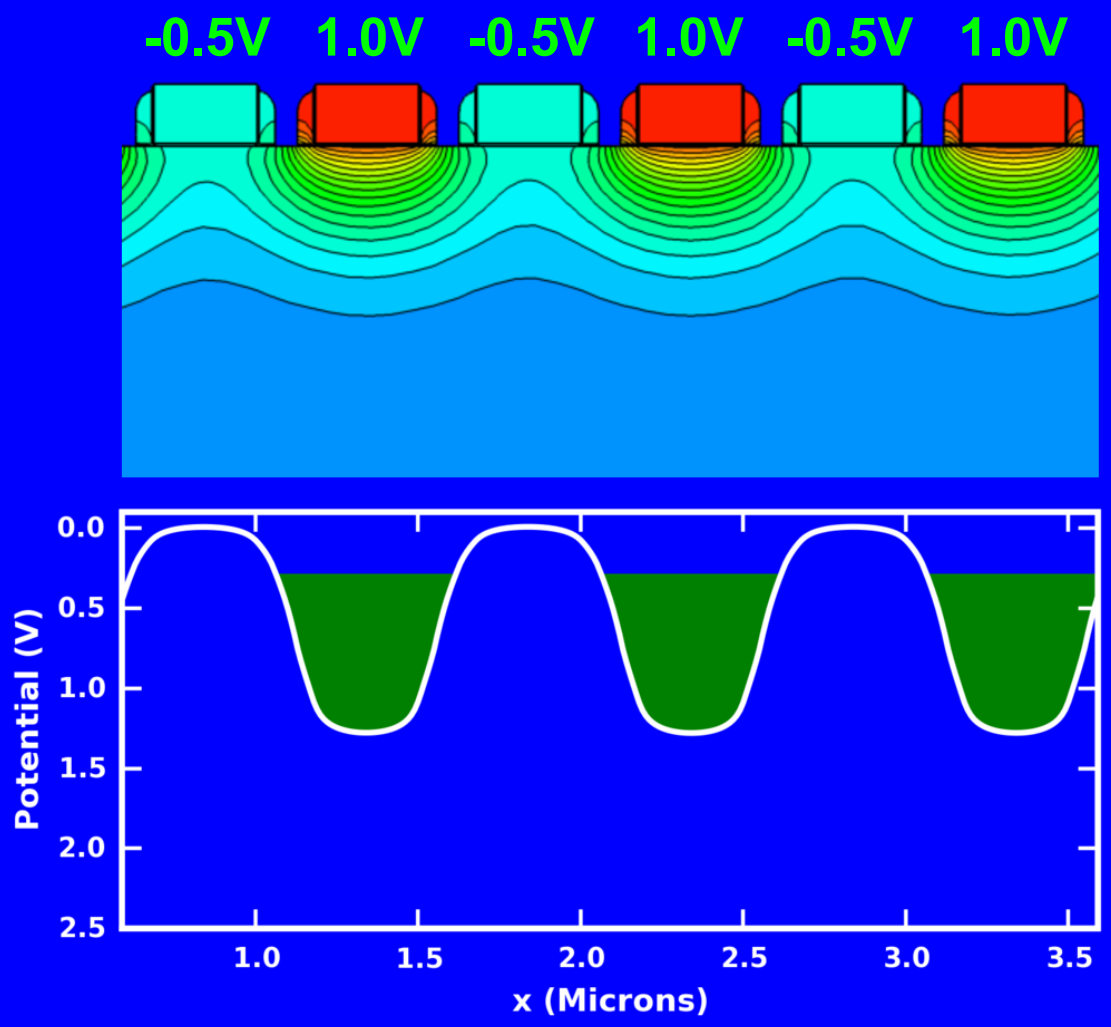


Potential Profile Along Channel



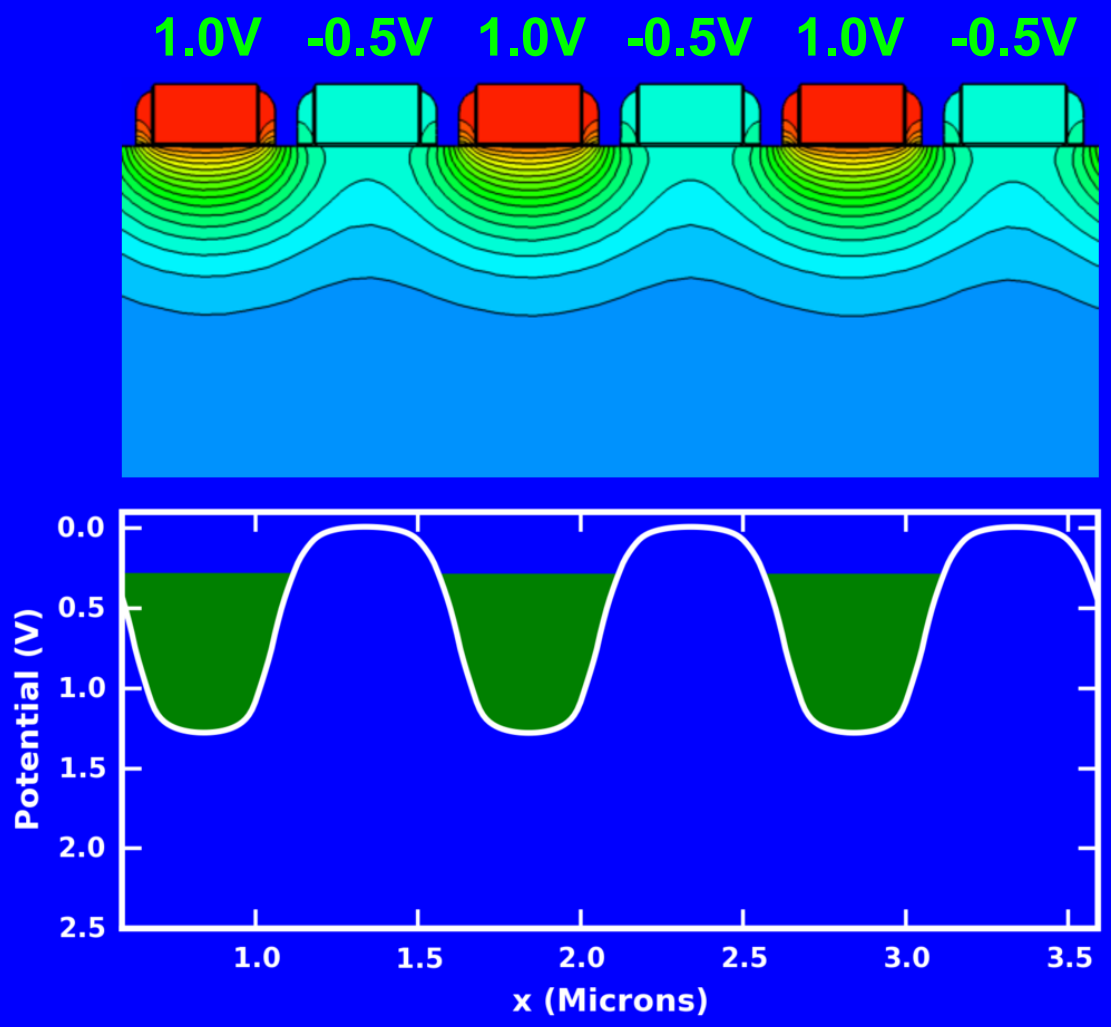
Potential Profile Along Channel

- Interlaced Mode (even field)

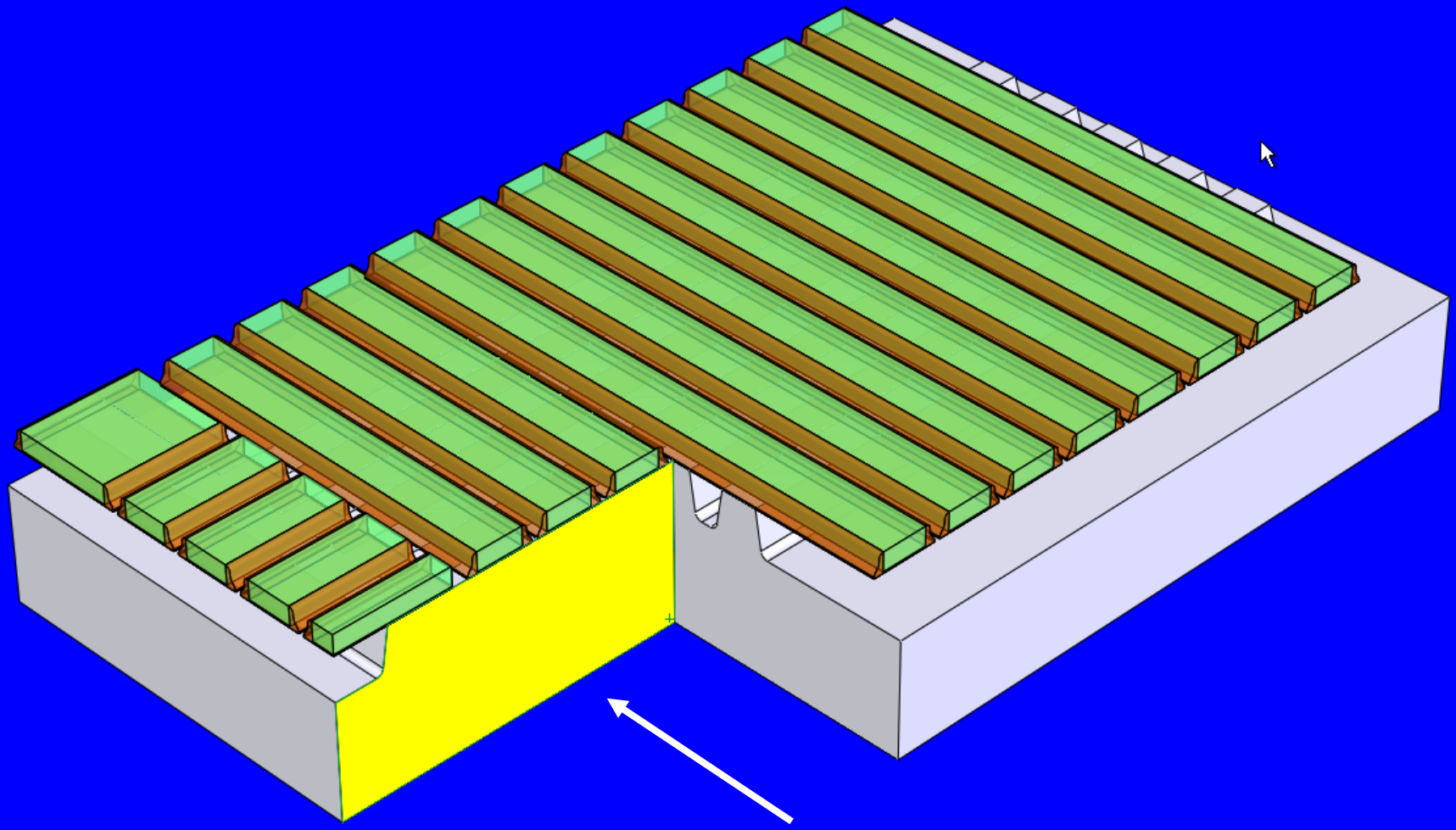


Potential Profile Along Channel

- Interlaced Mode (odd field)



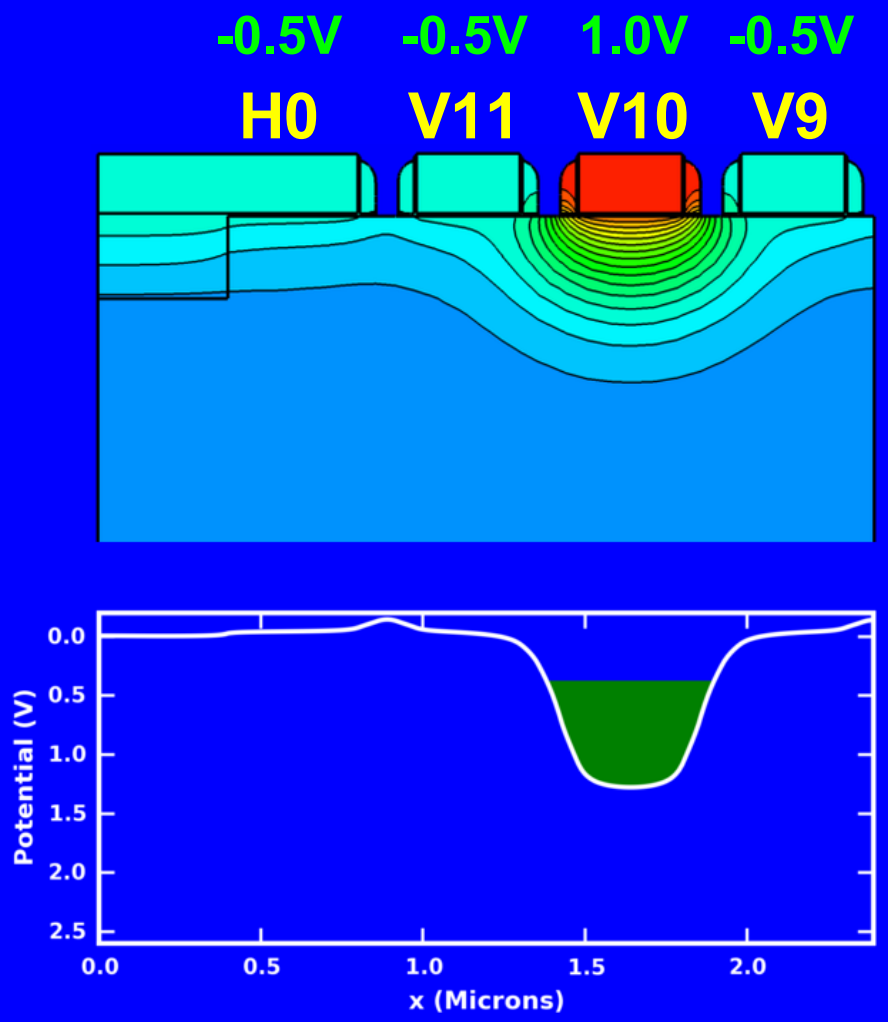
Simulation Into H-CCD



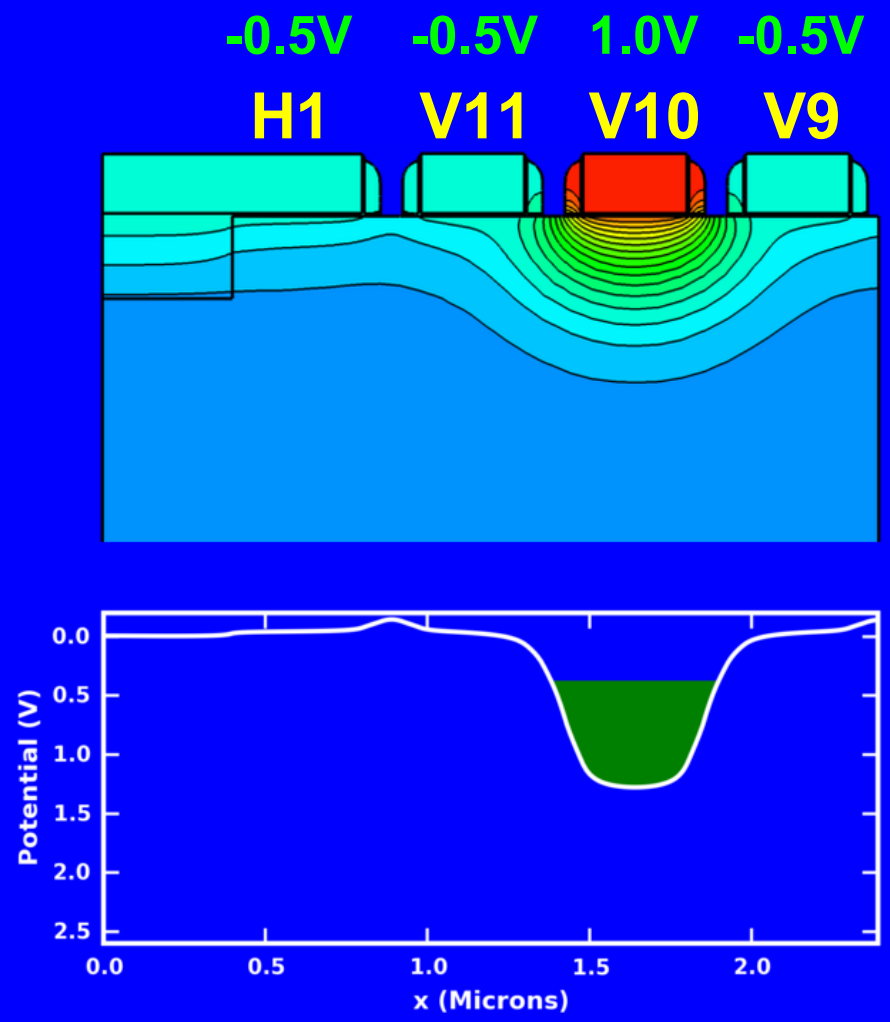
Cross-section
into H-CCD

Vertical to Horizontal Transfer

Even column

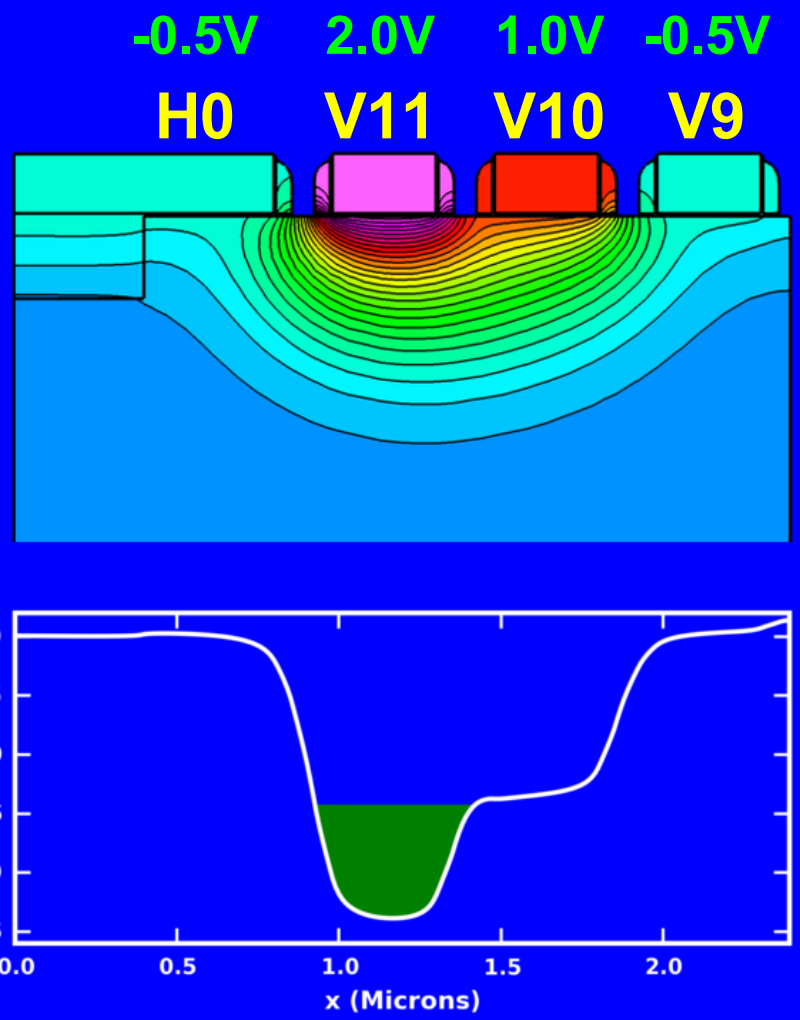


Odd column

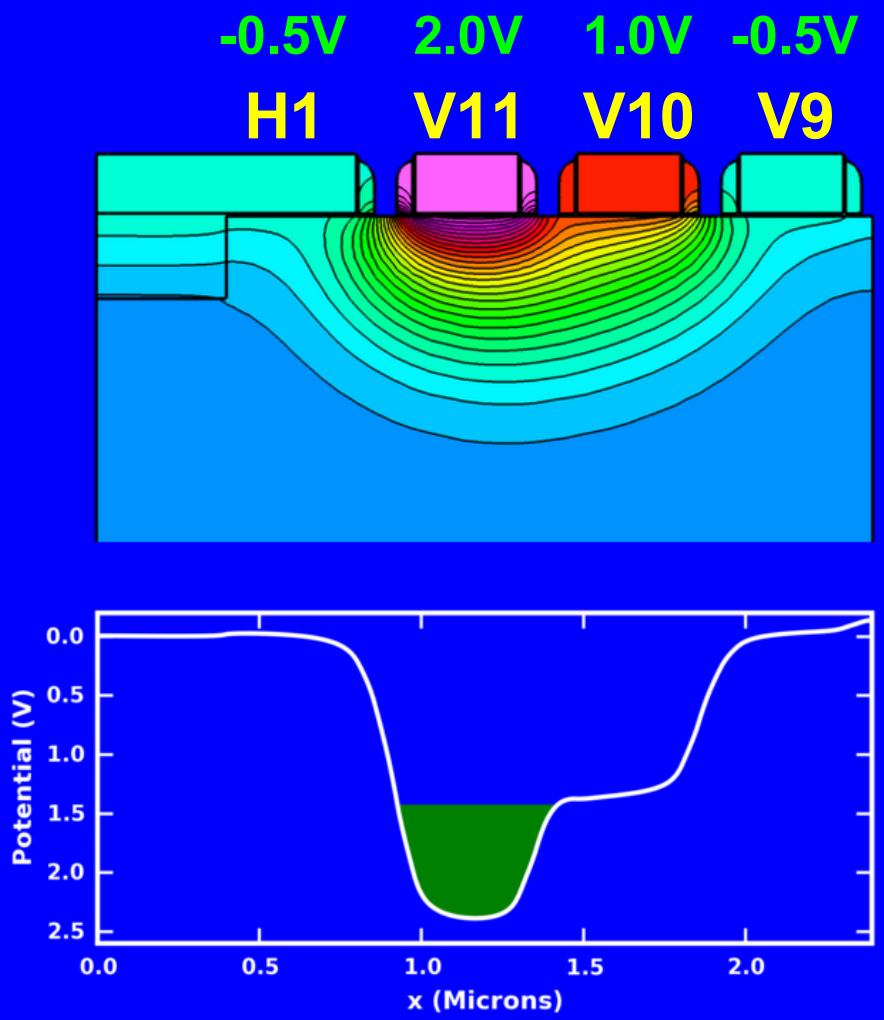


Vertical to Horizontal Transfer

Even column

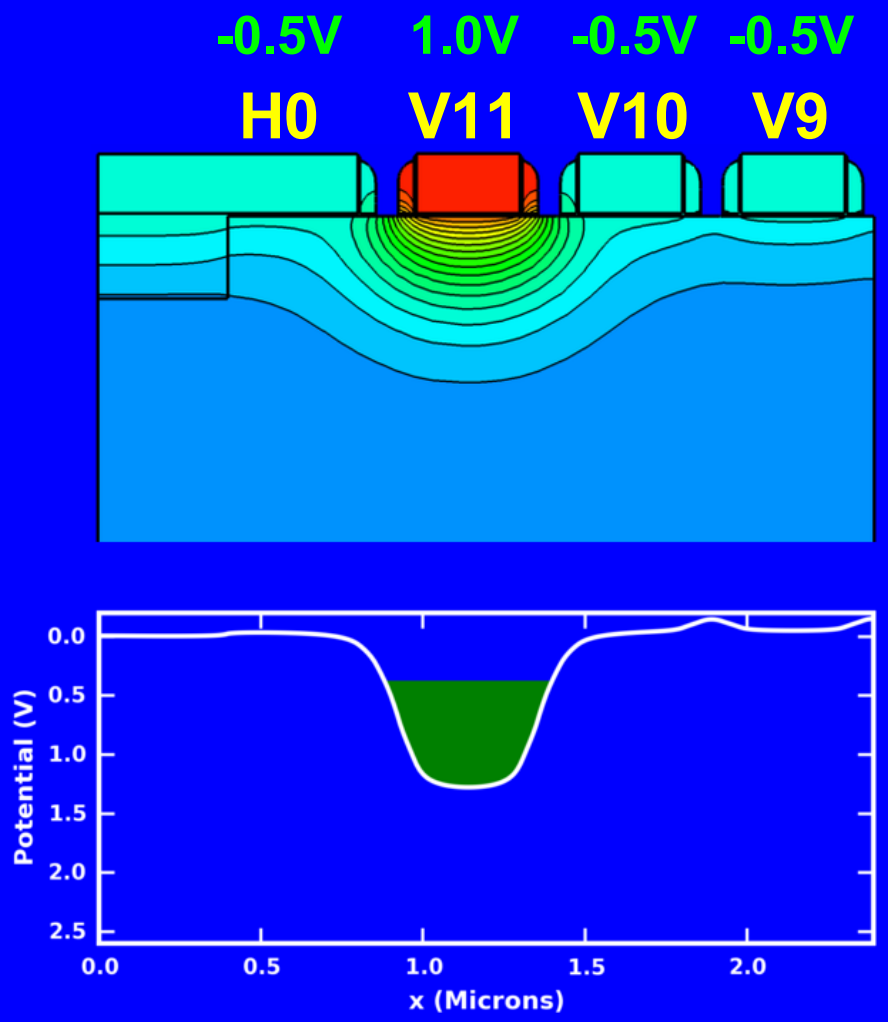


Odd column

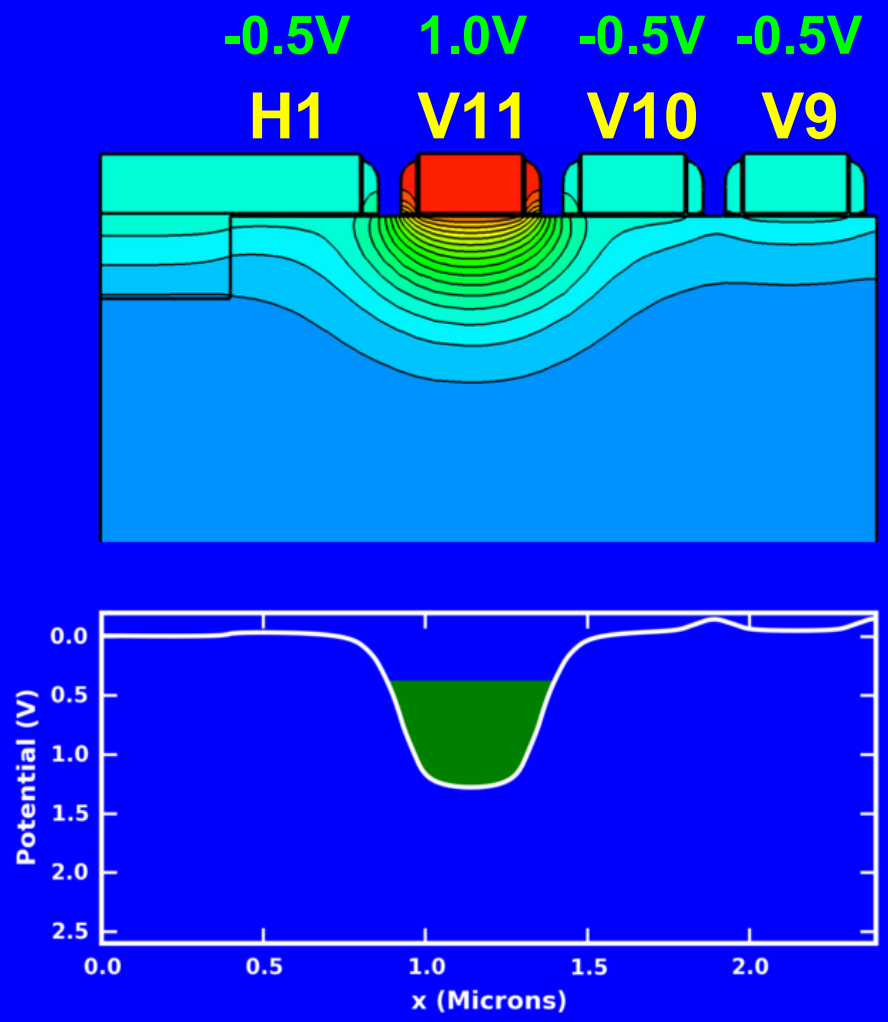


Vertical to Horizontal Transfer

Even column

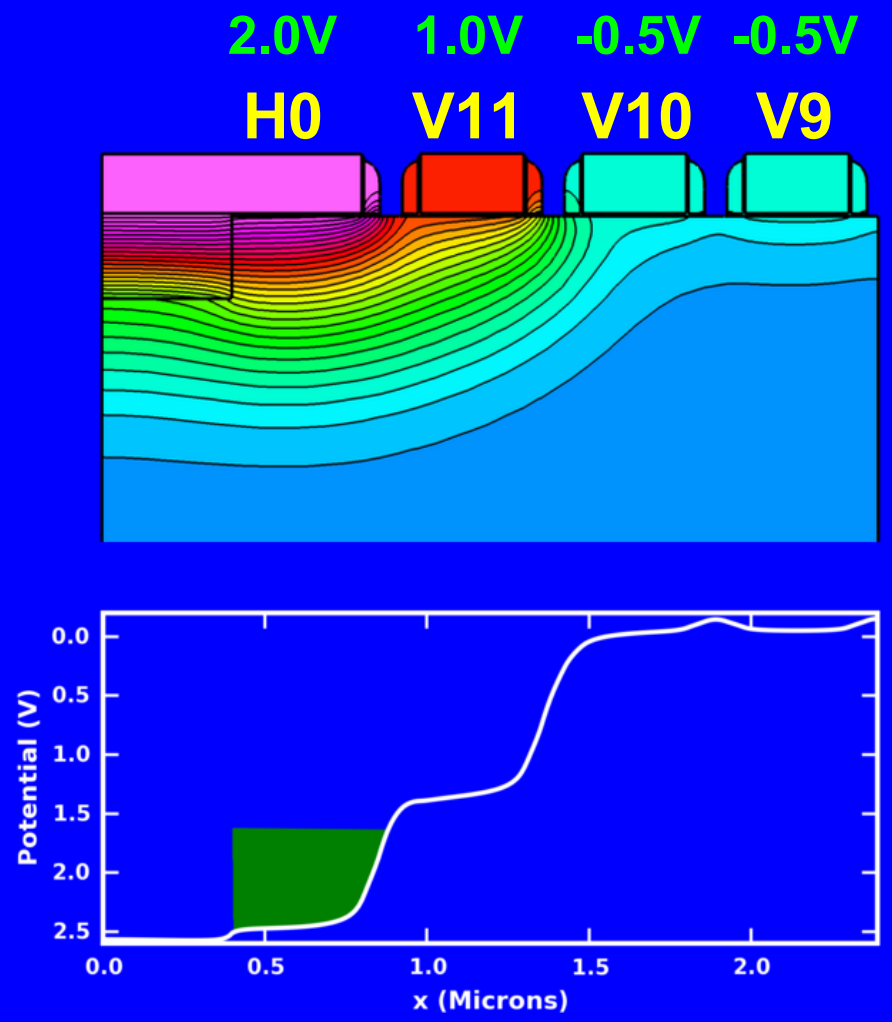


Odd column

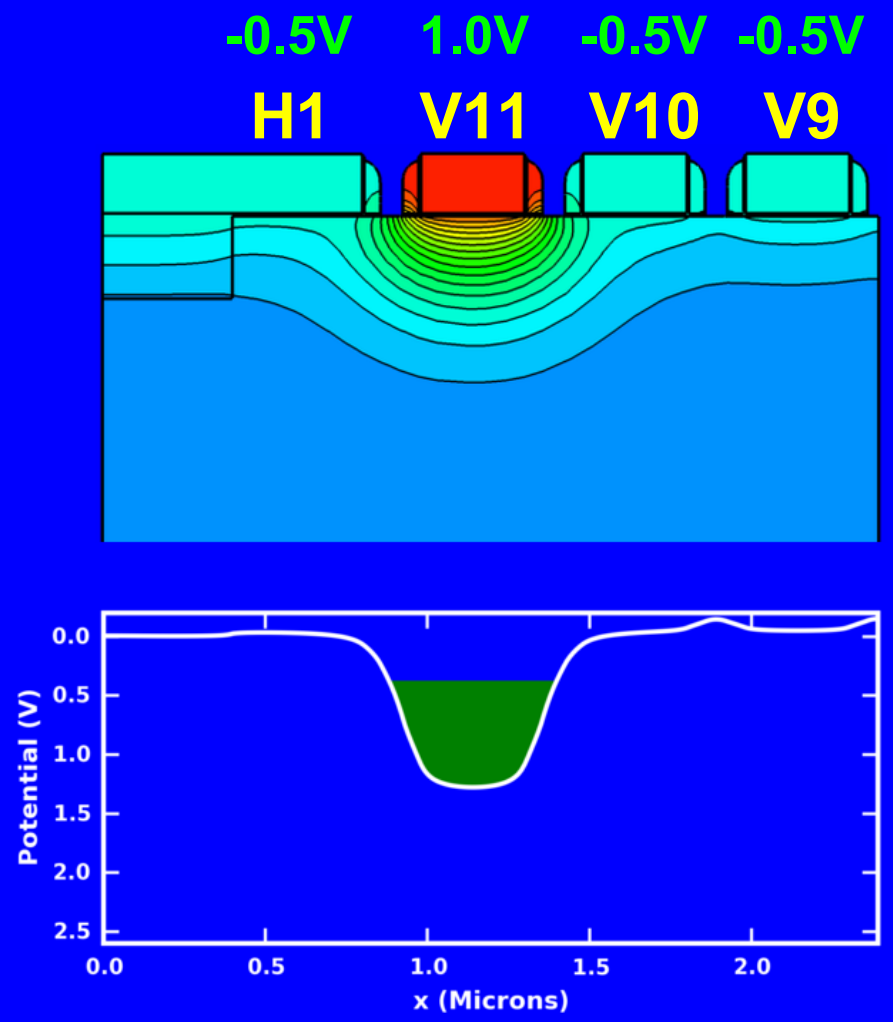


Vertical to Horizontal Transfer

Even column

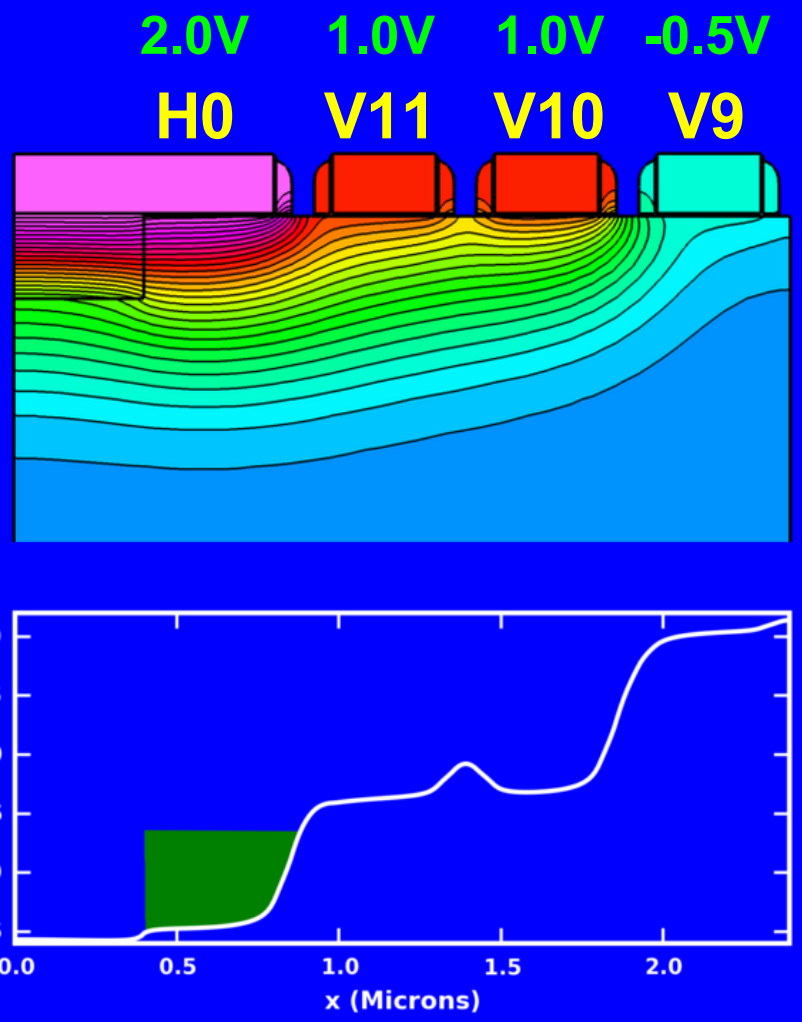


Odd column

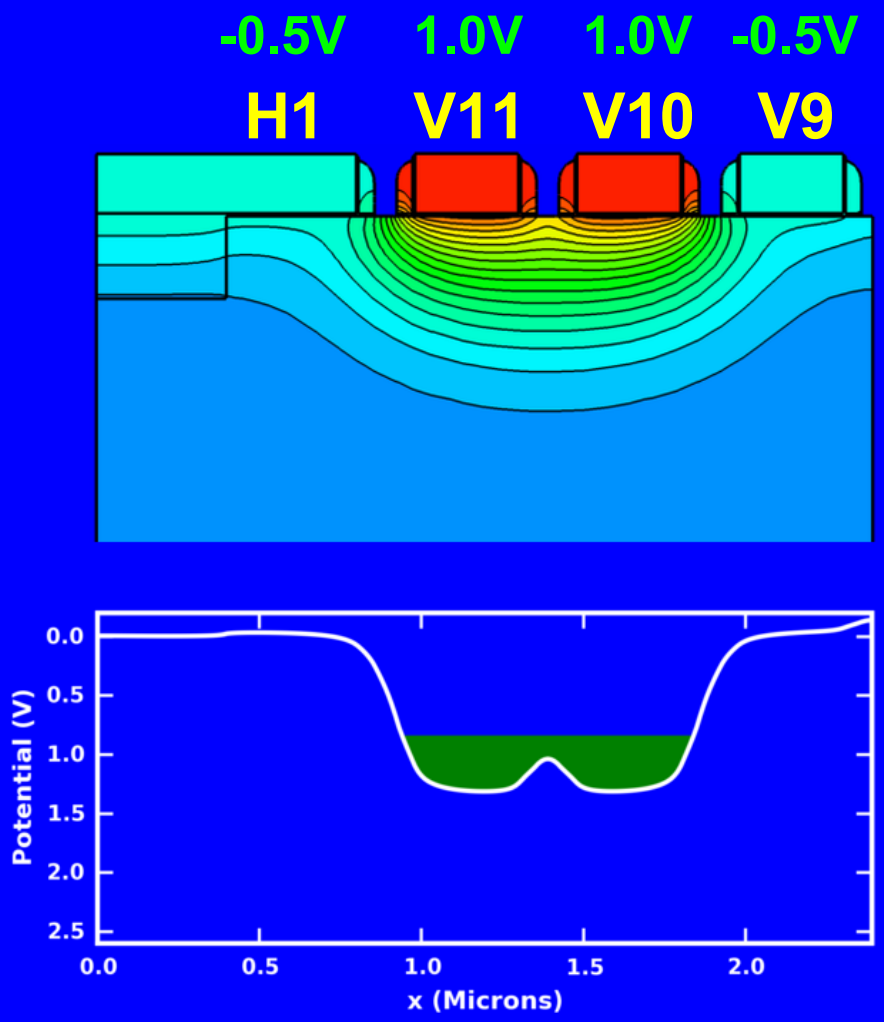


Vertical to Horizontal Transfer

Even column

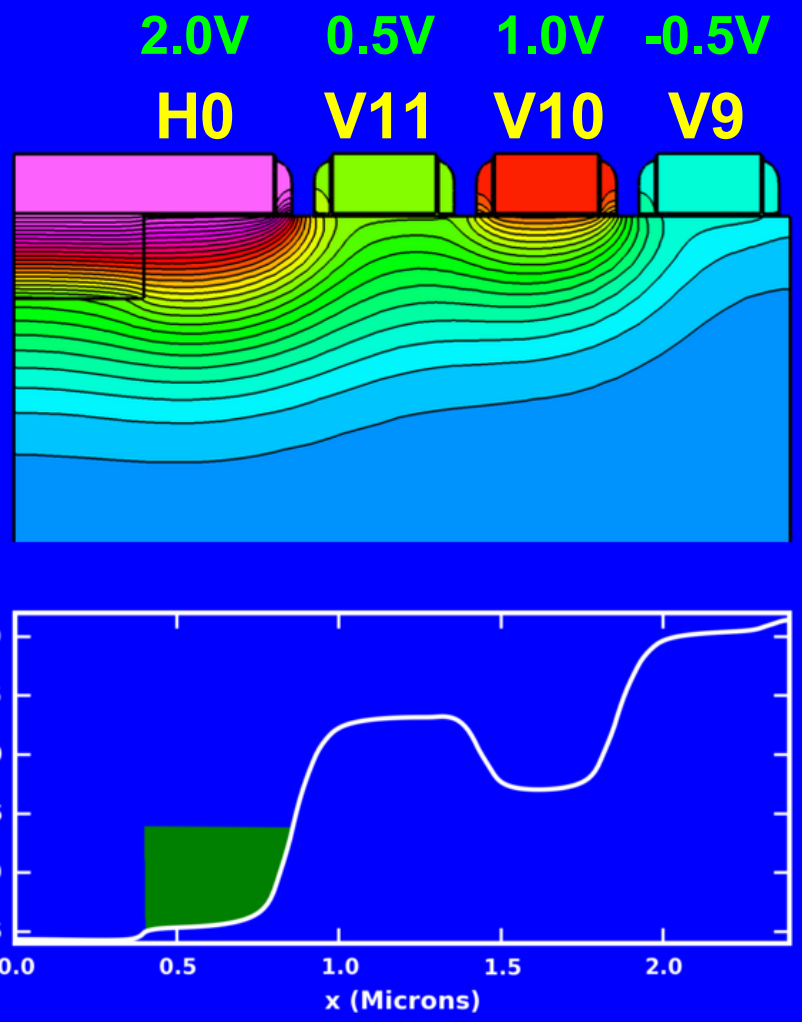


Odd column

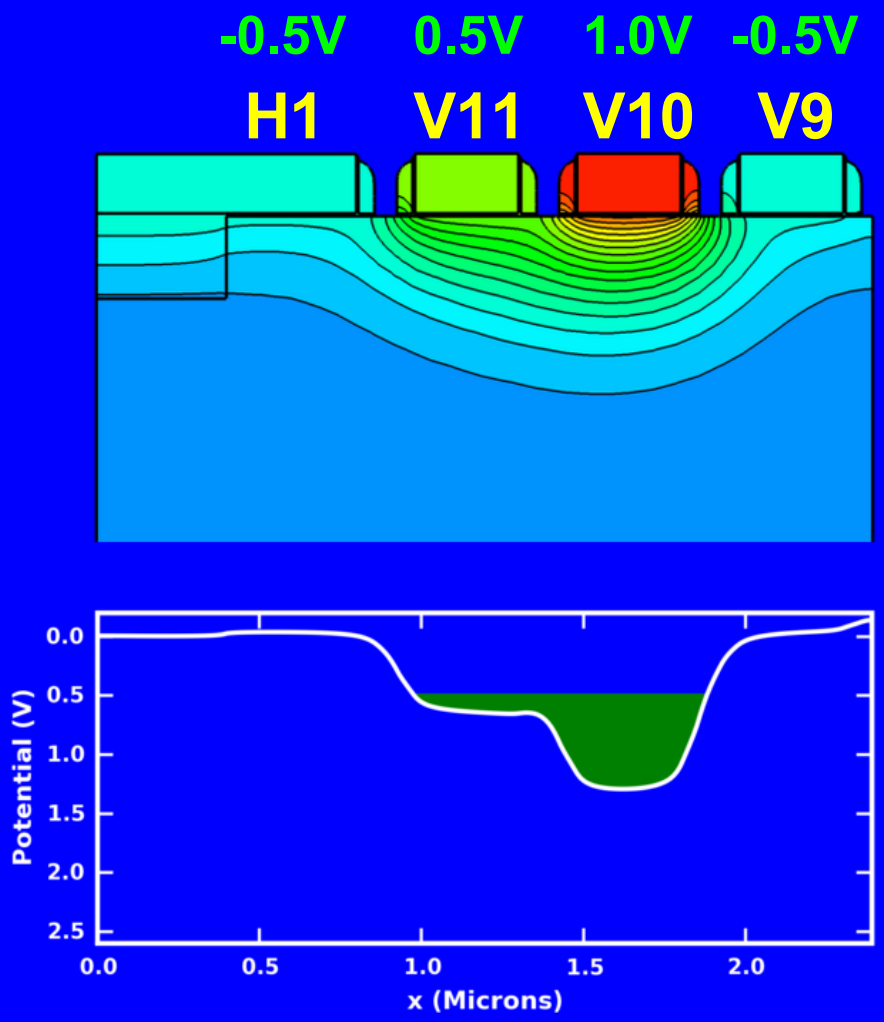


Vertical to Horizontal Transfer

Even column

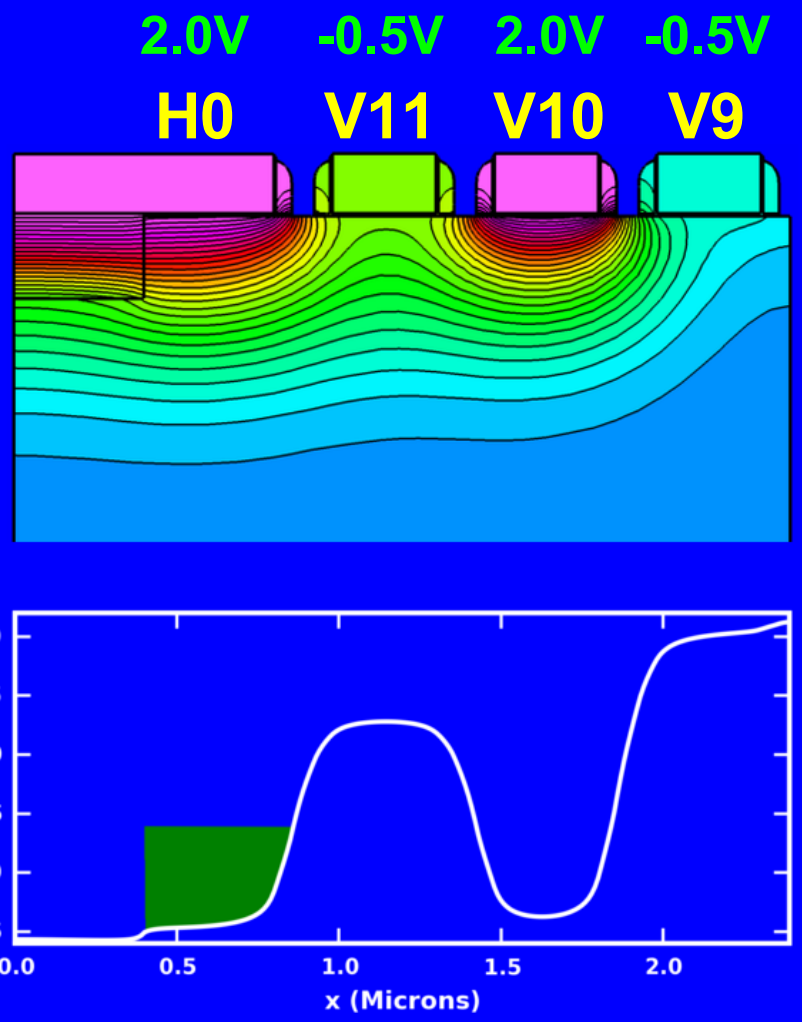


Odd column

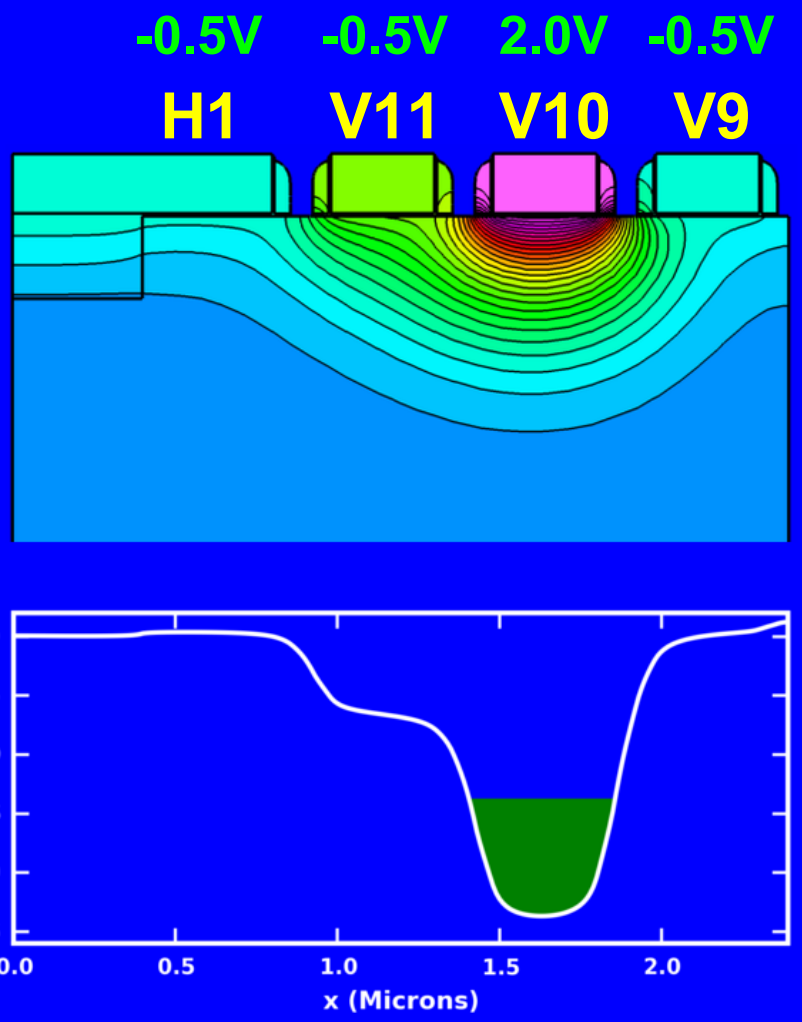


Vertical to Horizontal Transfer

Even column

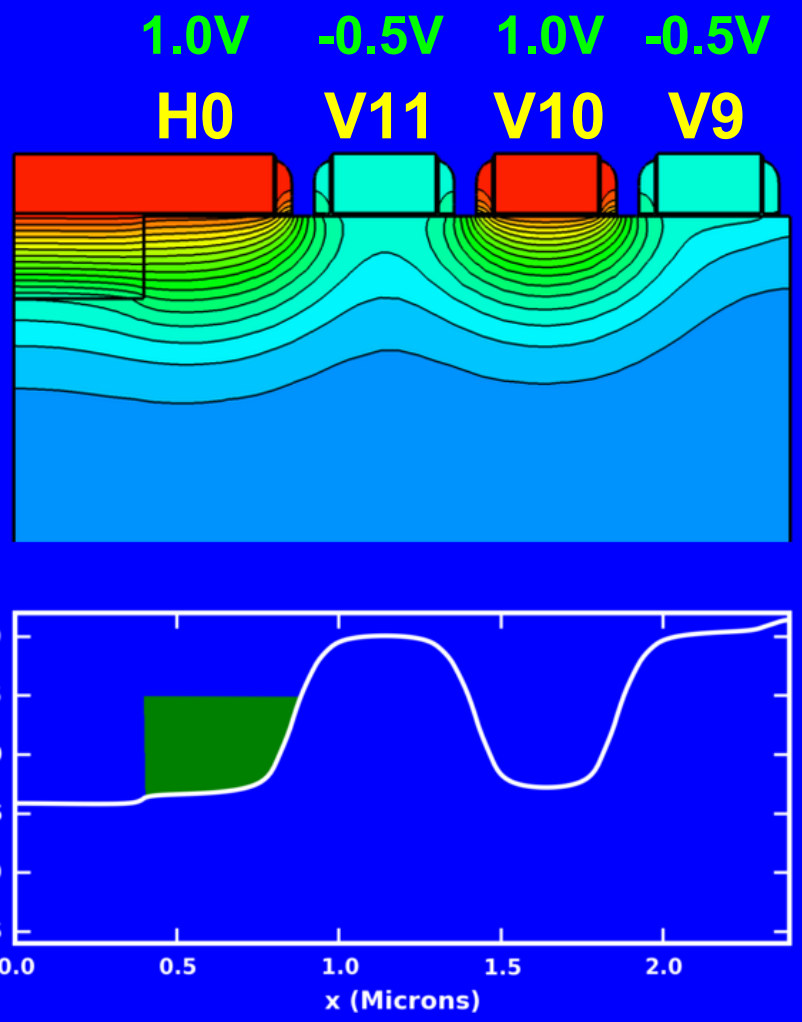


Odd column

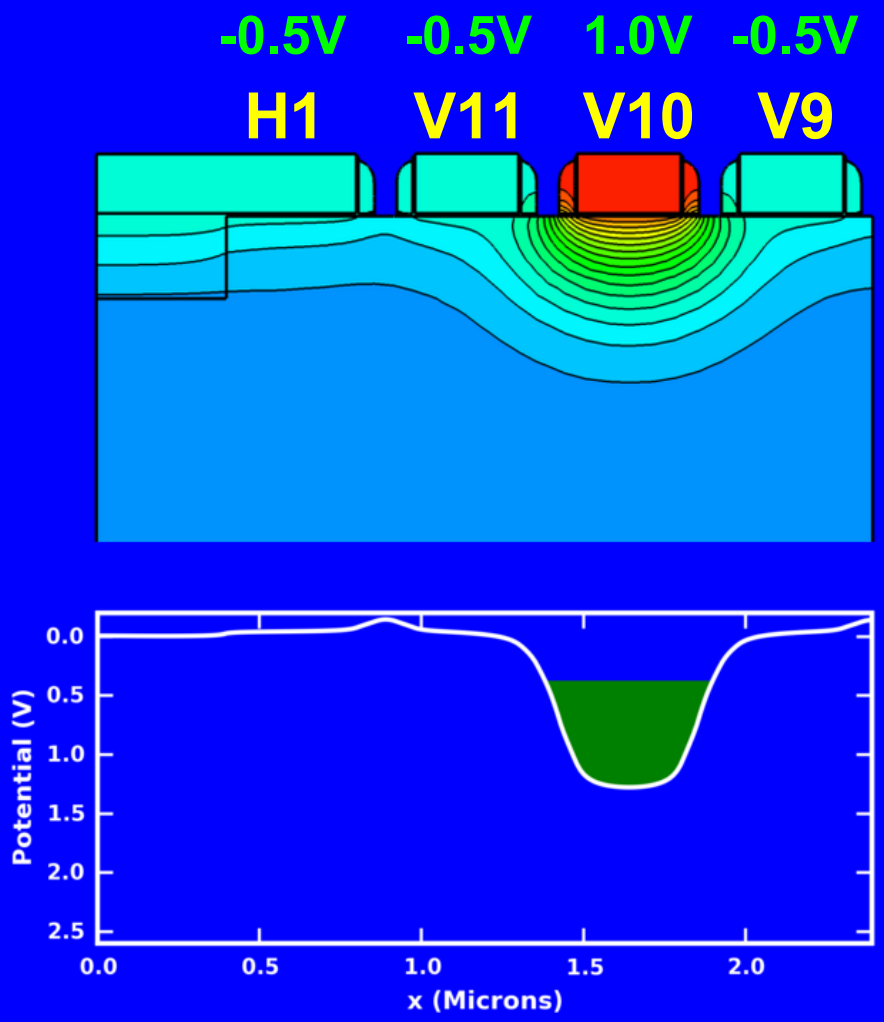


Vertical to Horizontal Transfer

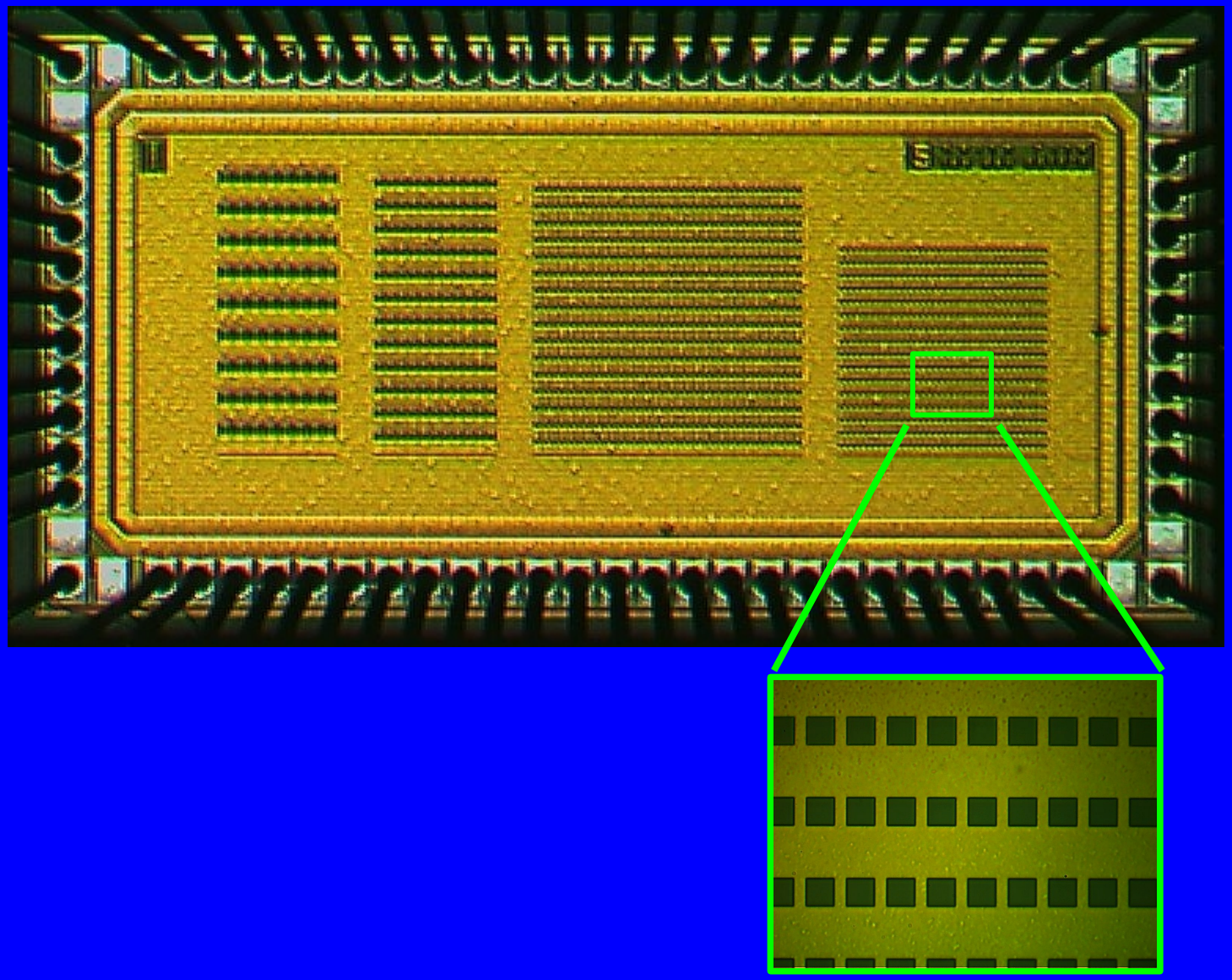
Even column



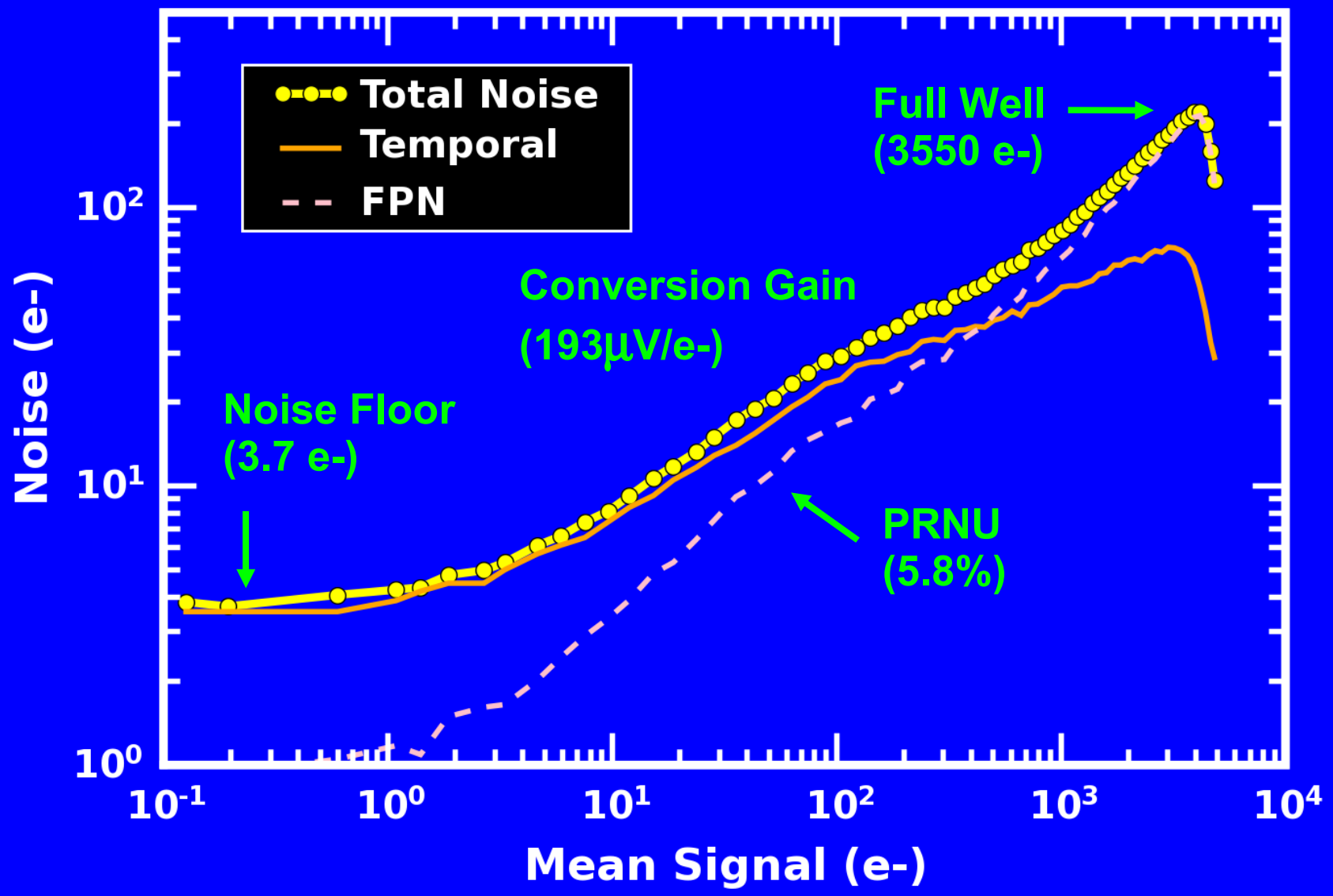
Odd column



Test Chip



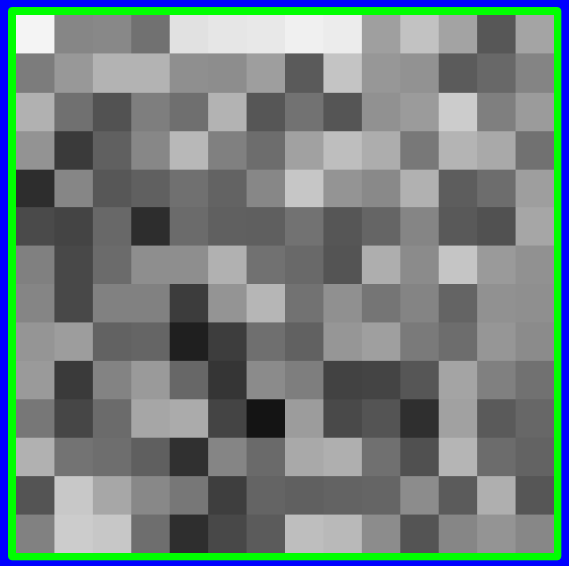
Measured Photon Transfer Curve



Measured Dark Current

- 50-100 e-/sec
- Non-uniformity of 25% rms
- Main source of DC comes from surface states

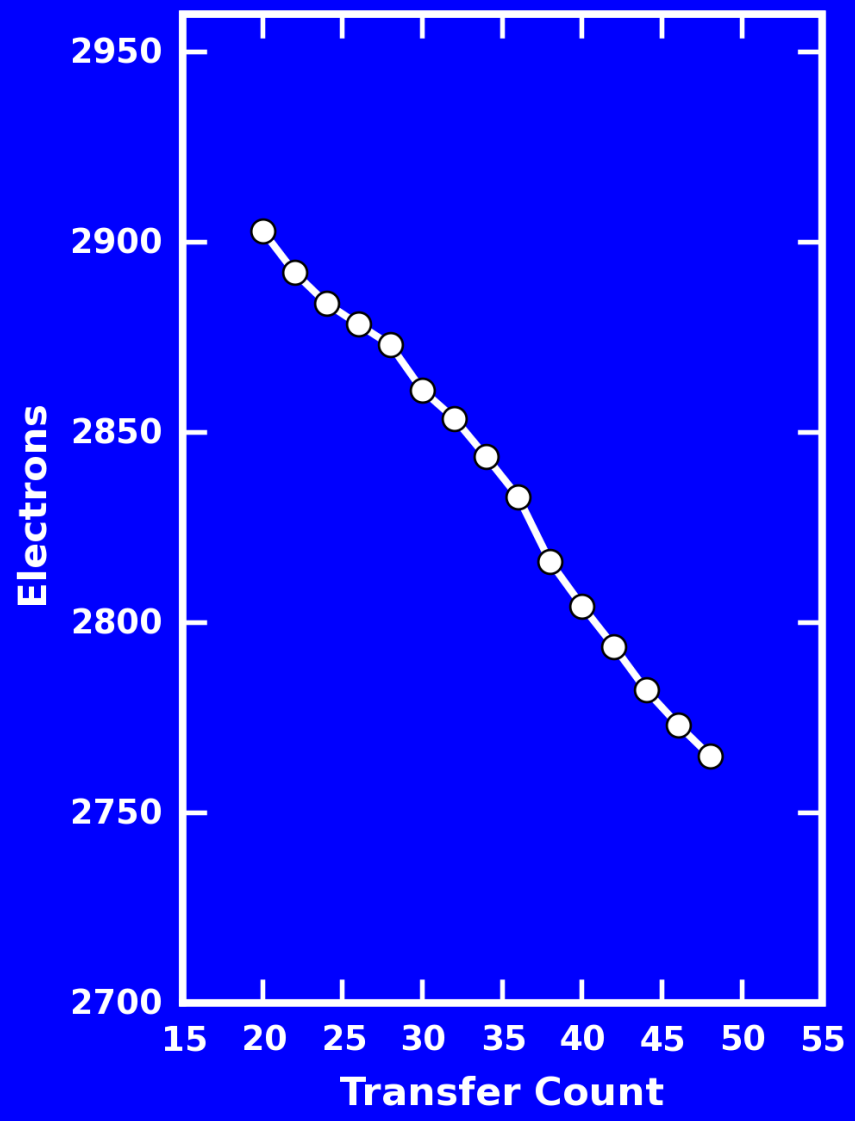
1 Second Integration



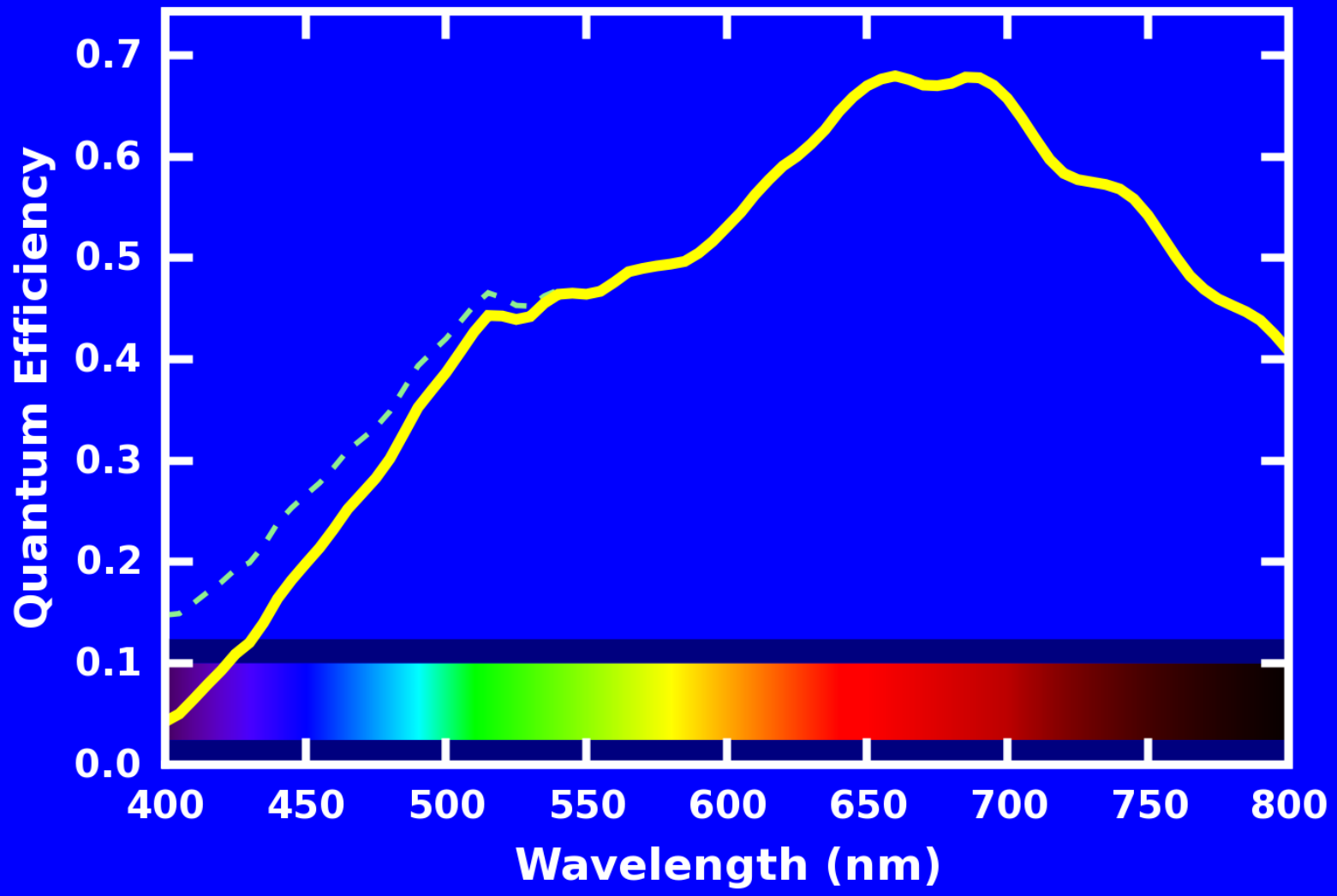
20 Second Integration

Measured Charge Transfer Efficiency

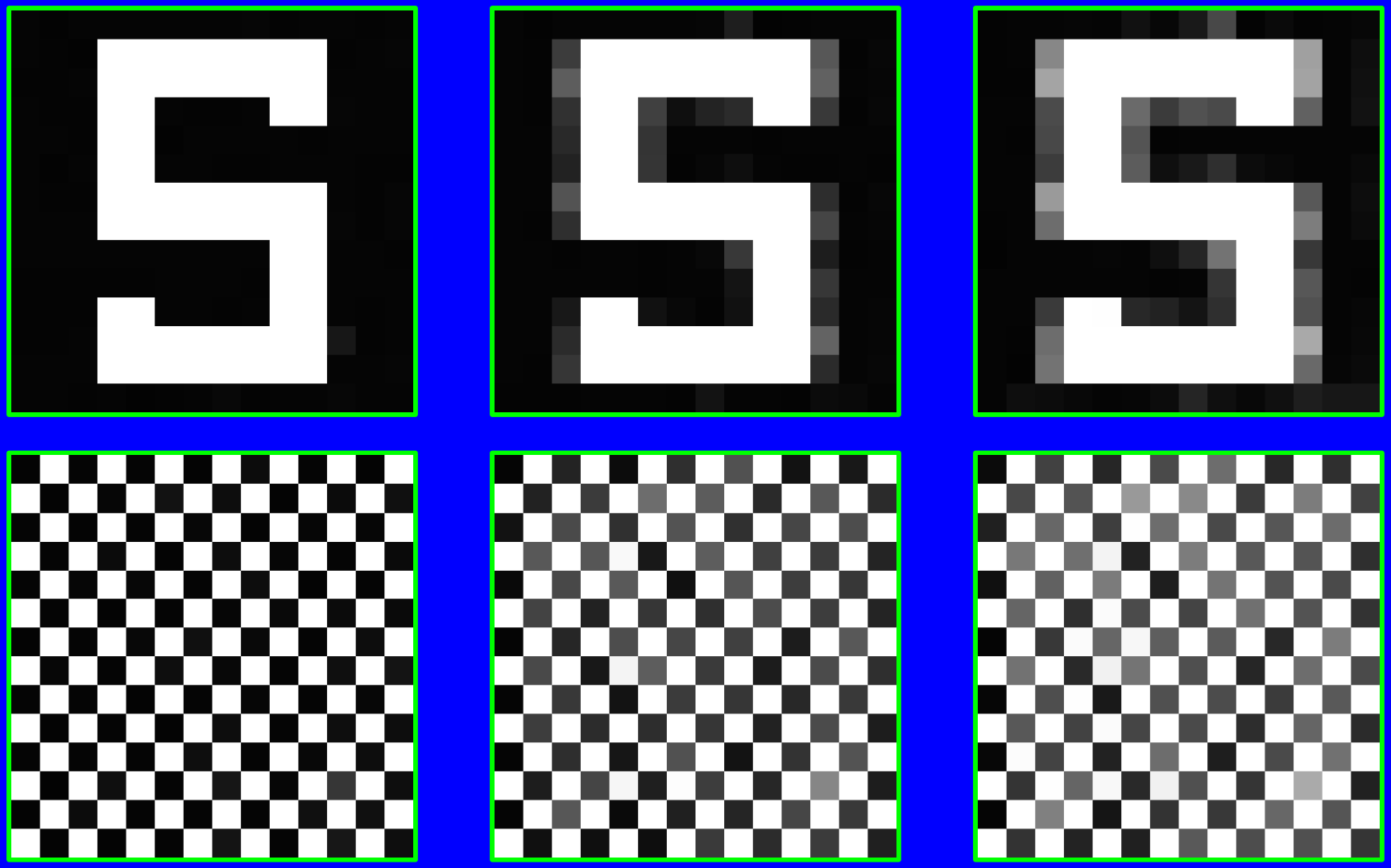
- CTE is 99.9% with 3000 electron charge packets
- CTE limited by surface interface traps
- CTE is reduced to 98% if holes are accumulated between storage electrodes.



Measured Quantum Efficiency



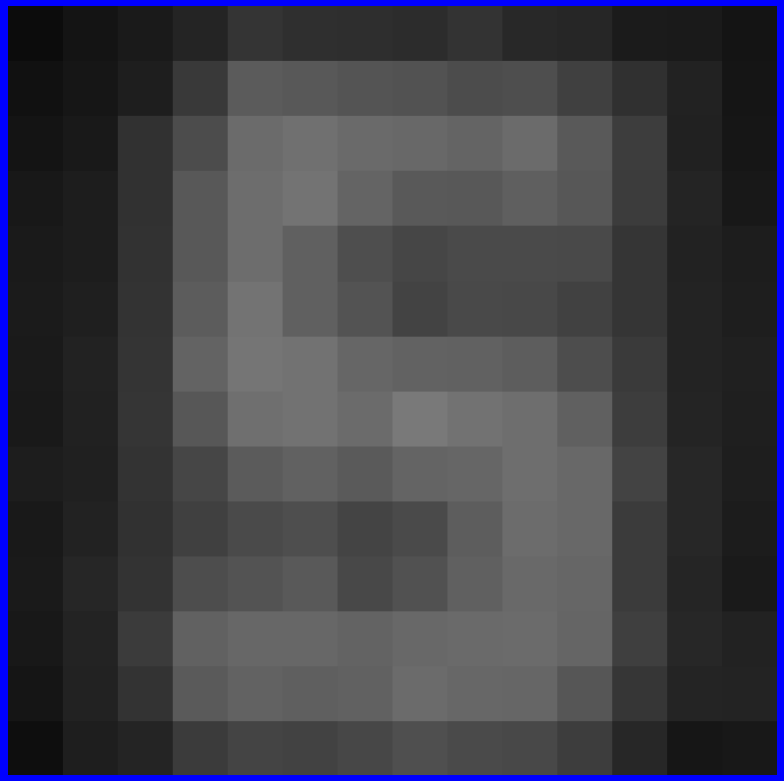
Electrical Images



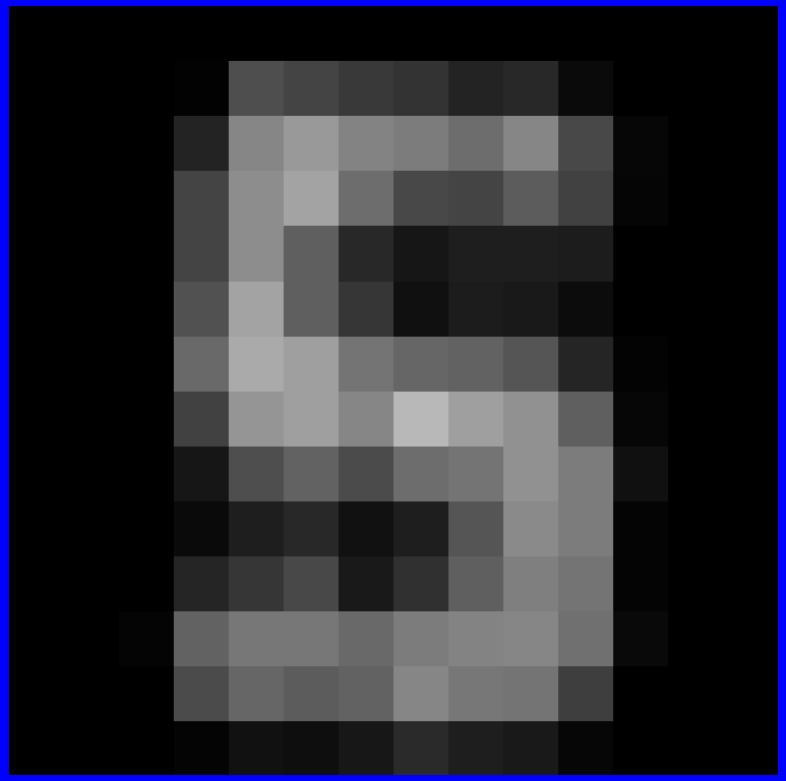
0.1 sec | 1.0 sec | 10.0 sec

Optical Images

Captured with F/2.8, f=6mm lens at 1/10 sec



Raw data



Added contrast

Performance Summary

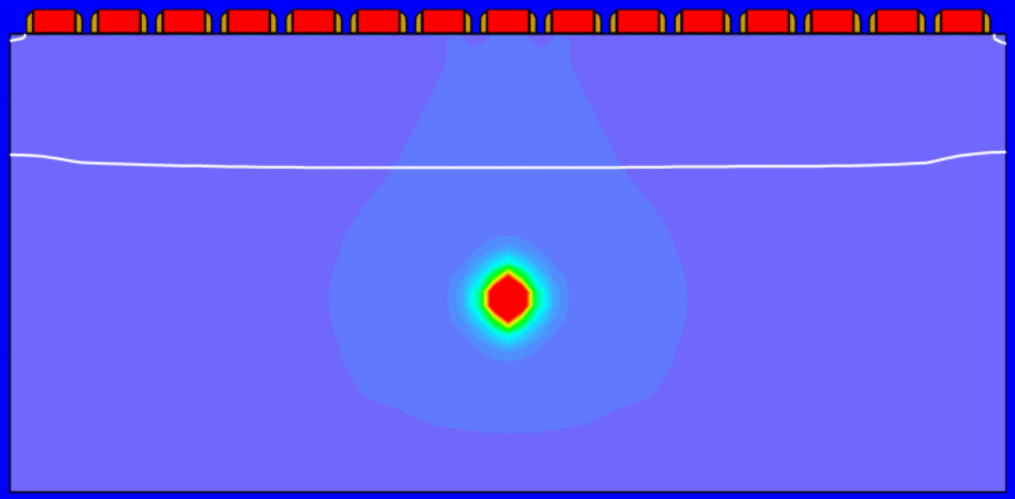
Well Capacity	3550e-
Conversion Gain	193uV/e-
Responsivity	480e-/lux-s
Read Noise	3.7e- rms
Dark Current	50e-/sec
DSNU	25%
PRNU	5.8%
Dynamic Range	60dB
Peak SNR	28dB

Scaling Issues

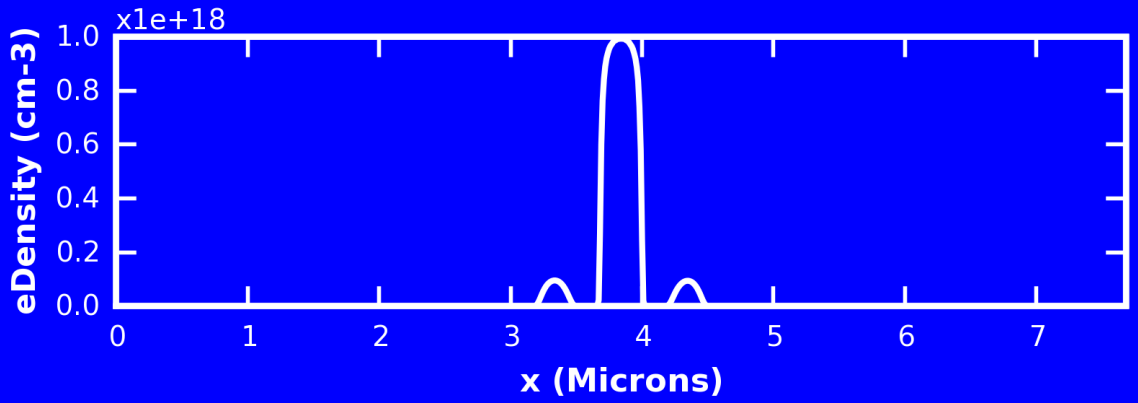
- Crosstalk
- Well capacity
- Dark current

Crosstalk

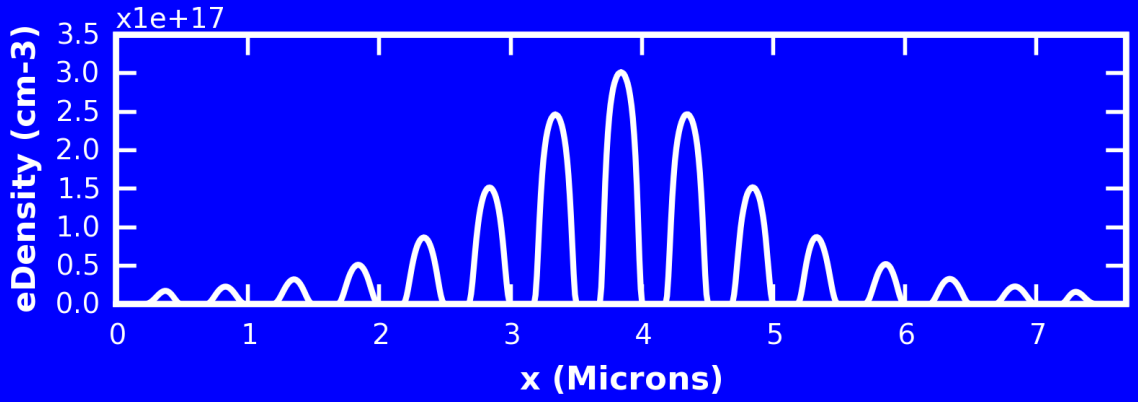
Simulation of charge induced at several depths



Depth - 0.5µm
Result - 85% correct

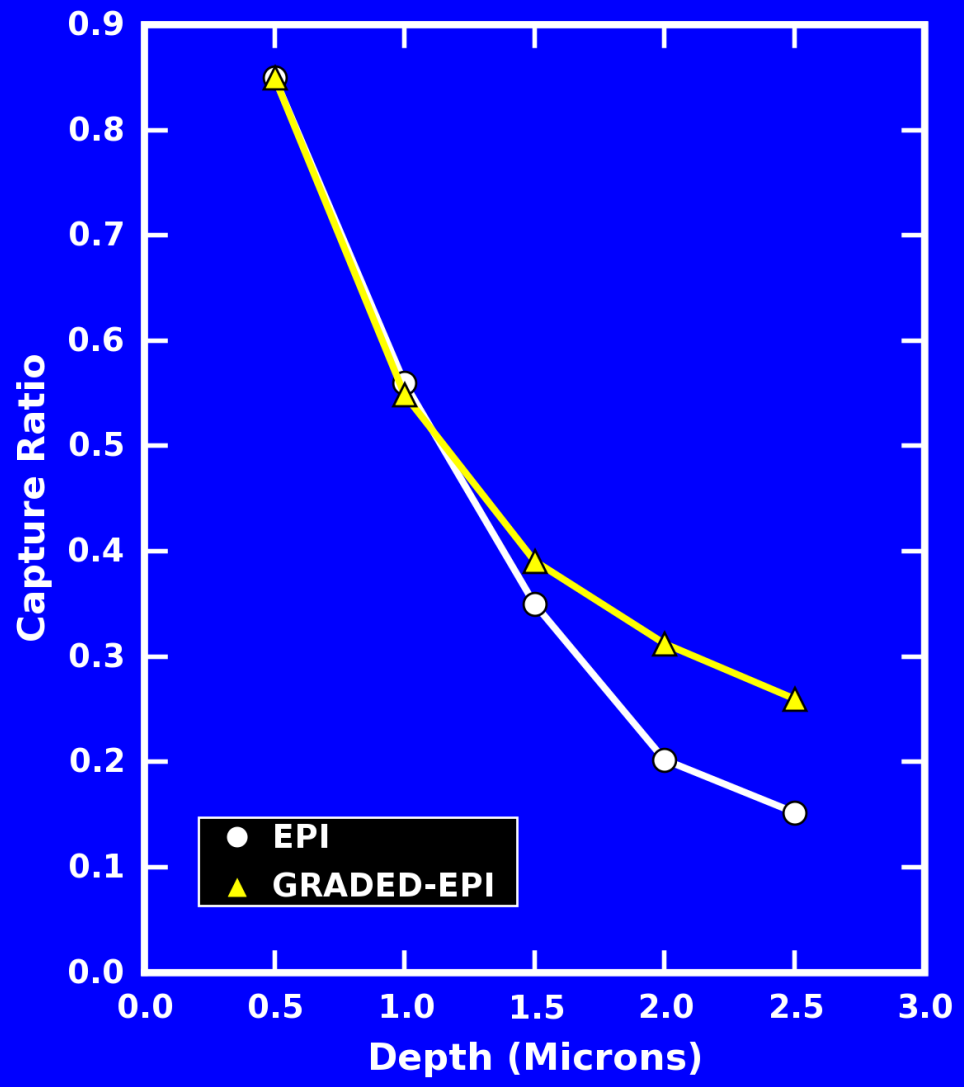


Depth - 2.0µm
Result - 20% correct



Simulated Crosstalk Improvement

- Weak electric field beyond the depletion region
- Graded-epi layer increases electric field beyond depletion region



Well Capacity

Small well capacity with single electrode storage (500 e-)

Solutions:

- Interlaced operation (3500 e-)
- Double electrode pixel
- Increase inter-gate barriers
  - Substrate doping
  - Electrode gap spacing
  - Implants between electrodes

Dark Current

Dark Current Density is high ($3.22 nA/cm^2$)

Potential Solutions:

- Buried channel implant
- Use inverted (pinned) surface during integration time

Summary

- 0.5µm pixels implemented in single poly CMOS process
- 16 x 16 FT-CCD architecture demonstrates 0.5µm pitch charge confinement
- Dark Current, CTE, and QE measurements indicate further pixel scaling is possible

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