A 0.5µm Pixel Frame-Transfer CCD Image Sensor in 110nm CMOS

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Pixel Scaling

- Increase spatial resolution
- Decrease format size

Pixel Sizes reported at IEDM, ISSCC, IISW
Image Sensor with Multiple Apertures

Small Image Sensor with integrated optics

Small Image Sensors integrated into large array
Multi-Aperture Imaging

- Object space in close proximity to image sensor
- Each array of pixels captures a portion of the object space
- Image is computationally reconstructed
Multi-Aperture with Objective Lens

• 3D imaging
  - Stereoscopic views of focal plane

Multi-Aperture for Color Separation

- Color separation by aperture
  - Improve crosstalk
  - Reduce color aliasing

Recent Pixel Scaling

4T sharing

Stack height reduction


* H. Sumi, IEDM 2006, p119-122
Optical Stack

Metal wire occlusions

Metal free
FT-CCD Architecture

- 16 x 16 Pixel Array
- 16 x 16 Frame Buffer
- 16 stage H-CCD
- Floating diffusion with source follower readout
Outline

• Design and Fabrication
• Operation
• Characterization
• Scaling Issues
• Conclusion
The 0.5 μm Pixel

Across Channel

Poly
STI
EPI

SPACER
OXIDE

Along Channel

Pixel

500nm
CCD Structure

STI forms the channel stop

Single-level poly electrodes
CMOS Fabrication

- S/D Implant mask is used to avoid dopant between electrodes (not self-aligned)
Operation

- **Flush**
  - Initial charge depletion

- **Integrate**
  - Pixel region collects charge

- **Buffer Transfer**
  - Charge shifted to shielded region

- **Horizontal Readout**
  - Charge shifted to H-CCD followed by sampling on floating diffusion
Operation (Flush)
Operation (Flush)
Operation (Integrate)

V0
V1
V2
V3
V4
V5
V6
V7
V8
V9
V10
V11

RS
VP

TS
H4
H3
H2
H1
H0
TX

COLB
VP

VTRANS = 2.0V
VSTORE = 1.0V
VISOLATE = -0.5V
Operation (Integrate)

V0
V1
V2
V3
V4
V5
V6
V7
V8
V9
V10
V11

TS  H4  H3  H2  H1  H0  TX  COLB  RT  VP

VTRANS = 2.0V
VSTORE = 1.0V
VISOLATE = -0.5V
Operation (Buffer Transfer)
Operation (Buffer Transfer)
Operation (Horizontal Transfer)
Simulation Along Channel

Cross-section along channel
Potential Profile Along Channel

1.0V 1.0V 1.0V 1.0V 1.0V 1.0V

A B

Potential (V)

x (Microns)
Potential Profile Along Channel

Potential (V)

x (Microns)
Potential Profile Along Channel

1.0V  1.0V  1.0V  -0.5V  2.0V  1.0V

Potential (V)

x (Microns)
Potential Profile Along Channel

1.0V  1.0V  1.0V  -0.5V  1.0V  1.0V

A

B

Potential (V)

x (Microns)
Potential Profile Along Channel
Potential Profile Along Channel

- Interlaced Mode (even field)
Potential Profile Along Channel

• Interlaced Mode (odd field)
Simulation Into H-CCD

Cross-section into H-CCD
Vertical to Horizontal Transfer

Even column
-0.5V  -0.5V  1.0V  -0.5V
H0    V11    V10    V9

Odd column
-0.5V  -0.5V  1.0V  -0.5V
H1    V11    V10    V9

Graphs showing potential vs. x (microns) for even and odd columns.
Vertical to Horizontal Transfer

Even column

-0.5V  2.0V  1.0V  -0.5V
H0    V11   V10   V9

Odd column

-0.5V  2.0V  1.0V  -0.5V
H1    V11   V10   V9

Potential (V)

x (Microns)
Vertical to Horizontal Transfer

Even column

-0.5V  1.0V  -0.5V  -0.5V
H0     V11   V10   V9

Odd column

-0.5V  1.0V  -0.5V  -0.5V
H1     V11   V10   V9
Vertical to Horizontal Transfer

Even column

<table>
<thead>
<tr>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.0V</td>
</tr>
<tr>
<td>1.0V</td>
</tr>
<tr>
<td>-0.5V</td>
</tr>
<tr>
<td>-0.5V</td>
</tr>
</tbody>
</table>

H0
V11
V10
V9

Odd column

<table>
<thead>
<tr>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>-0.5V</td>
</tr>
<tr>
<td>1.0V</td>
</tr>
<tr>
<td>-0.5V</td>
</tr>
<tr>
<td>-0.5V</td>
</tr>
</tbody>
</table>

H1
V11
V10
V9

Potential (V) vs. x (Microns)
Vertical to Horizontal Transfer

Even column

2.0V  0.5V  1.0V  -0.5V
H0    V11   V10   V9

Odd column

-0.5V  0.5V  1.0V  -0.5V
H1    V11   V10   V9

Potential (V)

0.0  0.5  1.0  1.5  2.0
x (Microns)
Vertical to Horizontal Transfer

Even column

2.0V  -0.5V  2.0V  -0.5V
H0    V11    V10    V9

Odd column

-0.5V  -0.5V  2.0V  -0.5V
H1    V11    V10    V9

Potential (V)

x (Microns)
Vertical to Horizontal Transfer

Even column

1.0V  -0.5V  1.0V  -0.5V
H0    V11   V10   V9

Odd column

-0.5V  -0.5V  1.0V  -0.5V
H1    V11   V10   V9
Test Chip
Measured Photon Transfer Curve

- **Total Noise**
- **Temporal**
- **FPN**

- **Noise Floor**: 3.7 e-
- **Full Well**: 3550 e-
- **Conversion Gain**: 193µV/e-
- **PRNU**: 5.8%
**Measured Dark Current**

- 50-100 e-/sec
- Non-uniformity of 25% rms
- Main source of DC comes from surface states
Measured Charge Transfer Efficiency

- CTE is 99.9% with 3000 electron charge packets
- CTE limited by surface interface traps
- CTE is reduced to 98% if holes are accumulated between storage electrodes.
Measured Quantum Efficiency

![Graph showing Measured Quantum Efficiency vs Wavelength (nm)](image)
Optical Images

Captured with F/2.8, f=6mm lens at 1/10 sec

Raw data

Added contrast
## Performance Summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Well Capacity</td>
<td>3550e-</td>
</tr>
<tr>
<td>Conversion Gain</td>
<td>193uV/e-</td>
</tr>
<tr>
<td>Responsivity</td>
<td>480e-/lux-s</td>
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<tr>
<td>Read Noise</td>
<td>3.7e- rms</td>
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<tr>
<td>Dark Current</td>
<td>50e-/sec</td>
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<tr>
<td>DSNU</td>
<td>25%</td>
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<tr>
<td>PRNU</td>
<td>5.8%</td>
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<tr>
<td>Dynamic Range</td>
<td>60dB</td>
</tr>
<tr>
<td>Peak SNR</td>
<td>28dB</td>
</tr>
</tbody>
</table>
Scaling Issues

- Crosstalk
- Well capacity
- Dark current
Crosstalk

Simulation of charge induced at several depths

Depth - 0.5µm
Result - 85% correct

Depth - 2.0µm
Result - 20% correct
Simulated Crosstalk Improvement

- Weak electric field beyond the depletion region
- Graded-epi layer increases electric field beyond depletion region
Well Capacity

Small well capacity with single electrode storage (500 e-)

Solutions:
- Interlaced operation (3500 e-)
- Double electrode pixel
- Increase inter-gate barriers
  - Substrate doping
  - Electrode gap spacing
  - Implants between electrodes
Dark Current Density is high (3.22nA/cm$^2$)

Potential Solutions:
- Buried channel implant
- Use inverted (pinned) surface during integration time
Summary

- 0.5µm pixels implemented in single poly CMOS process
- 16 x 16 FT-CCD architecture demonstrates 0.5µm pitch charge confinement
- Dark Current, CTE, and QE measurements indicate further pixel scaling is possible
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