

A Nyquist-Rate Pixel-Level ADC for CMOS Image Sensors

David X. D. Yang, Boyd Fowler, and Abbas El Gamal

Abstract—A multichannel bit-serial (MCBS) analog-to-digital converter (ADC) is presented. The ADC is ideally suited to pixel-level implementation in a CMOS image sensor. The ADC uses successive comparisons to output one bit at a time simultaneously from all pixels. It is implemented using a 1-bit comparator/latch pair per pixel or per group of neighboring pixels, and a digital-to-analog-converter/controller shared by all pixels. The comparator/latch pair operates at very slow speeds and can be implemented using simple robust circuits. The ADC's can be fully tested by applying electrical signals without any optics or light sources. A CMOS 320×256 sensor using the MCBS ADC is described. The chip measures $4.14 \times 5.16 \text{ mm}^2$. It achieves $10 \times 10 \text{ } \mu\text{m}^2$ pixel size at 28% fill factor in 0.35- μm CMOS technology. Each 2×2 pixel block shares an ADC. The pixel block circuit comprises 18 transistors. It operates in subthreshold to maximize gain and minimize power consumption. The power consumed by the sensor array is 20 mW at 30 frames/s. The measured integral nonlinearity is 2.3 LSB, and differential nonlinearity is 1.2 LSB at eight bits of resolution. The standard deviation of the gain and offset fixed pattern noise due to the ADC are 0.24 and 0.2%, respectively.

Index Terms—Analog-to-digital conversion, cameras, CMOS image sensors, image sensors, mixed analog-digital integrated circuits, pixel-level analog-to-digital converter (ADC), video cameras.

I. INTRODUCTION

CMOS technology holds out the promise of integrating image sensing and image processing into a single-chip digital camera. Recent papers [1], [2] report on the integration of an active pixel sensor (APS) with an analog-to-digital converter (ADC), color processing, and control on a single CMOS chip. In [1], Loinaz *et al.* describe a PC-based single-chip digital color camera, which integrates a photogate APS, automatic gain control, an 8-bit full flash ADC, and all the compute-intensive pixel-rate tasks such as color interpolation, color correction, and image statistics computation. Frame-rate tasks, such as exposure control and white balance, are implemented in software on the host PC. In [2], Smith *et al.* describe a single-chip CMOS National Television Systems Committee (NTSC) video camera that integrates an APS, a

half-flash subranging ADC, and all the processing necessary to produce color NTSC video with only an external power supply and a crystal oscillator. This “system-on-chip” approach of combining the functional blocks of a multichip digital camera onto a single chip reduces the imaging system's cost and power. However, it does not fully exploit the potential of integrating image sensing and processing. Integration provides the opportunity to rethink the basic camera design. By redistributing the processing down to the pixel level, new imaging capabilities, higher image quality, and more significant reduction in system cost and power can be achieved.

In this paper, we focus on the integration of analog-to-digital (A/D) conversion with an image sensor at the pixel level. A/D conversion can be integrated at the chip level [1]–[3], at the column level [4]–[9], or at the pixel level [10]–[16]. The chip-level approach is, at present, the most commonly used. A single conventional high-speed ADC, operating at about 10 Msamples/s for video, is integrated with the image sensor. To lower the ADC operating speed, the column-level approach is used. In this case, an array of ADC's, each dedicated to one or more columns of the sensor array, is employed. The ADC's are operated in parallel, and, therefore, low-to-medium-speed ADC architectures can be employed. For example, single-slope ADC's are used in [6] and [8], algorithmic ADC's are used in [8] and [9], successive approximation ADC's are used in [7], and oversampling $\Sigma\Delta$ ADC's are used in [7] and [17]. To lower ADC speeds even further, the pixel-level approach is used. Here, an ADC is dedicated for each pixel or each group of neighboring pixels, and the ADC's are operated in parallel. As a result, very low-speed converters operating at tens of samples per second can be used. Analysis by several authors [5], [18] shows that pixel-level A/D conversion should achieve the highest signal-to-noise ratio (SNR) and the lowest power consumption since it is performed in parallel, close to where the signals are generated, and can be operated at very low speeds. Another advantage of pixel-level A/D conversion is scalability. The same pixel and ADC design and layout can be readily used for a very wide range of sensor sizes. Pixel-level A/D conversion is also well suited for standard digital CMOS process implementation. Since the ADC's can be operated at very low speeds, very simple and robust circuits can be used. Unfortunately, none of the well-established A/D conversion techniques meets the stringent area and power requirements for a pixel-level implementation. As a result, most published work on ADC's for image sensors is focused on column- and chip-level implementations.

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A few authors have taken up the challenge of implementing a pixel-level ADC [10]–[14]. In [10], [11], and [13], a voltage-to-frequency converter is used at each pixel so that no analog signals need to be transported. However, since the A/D conversion is performed one row at a time, this method is essentially a column-level A/D conversion method and therefore cannot achieve the potential high SNR and low power of true pixel-level A/D conversion.

In [12] and [14], the first pixel-level A/D conversion technique is described. Each ADC employs a 1-bit $\Sigma\Delta$ modulator at each pixel. The ADC’s are implemented using very simple and robust circuits and operate in parallel. The implementation has several shortcomings, including large pixel size, high output data rate due to oversampling, poor low-light performance, high fixed pattern noise, and lag. The poor low-light performance is due to $\Sigma\Delta$ ADC’s relatively coarse quantization steps near the ends of the input range [19]. The high fixed pattern noise is due to the difficulty of implementing the precise feedback needed in the $\Sigma\Delta$ modulator at the pixel level. The lag is due to the fact that the photodetectors are not reset after each sample. The large pixel size problem quickly disappears with technology scaling, as we demonstrate in this paper. Since pixel size is set mainly by optical and dynamic range requirements, it does not scale with CMOS technology. Therefore, as technology scales, more transistors can be integrated at the pixel level without reduction in fill factor.

In this paper, we introduce the first viable Nyquist-rate pixel-level ADC, which we denote by multichannel bit-serial (MCBS) ADC. It uses successive comparisons to output one bit at a time simultaneously from all pixels. It can still be implemented using simple robust circuits and overcomes the shortcomings of the aforementioned $\Sigma\Delta$ ADC technique. Output data rate is reduced by using Nyquist-rate conversion instead of oversampling. Low-light performance is improved to the level of analog CMOS sensors by using direct integration instead of continuous sampling. Nonuniformity is significantly reduced by globally distributing the signals needed to operate the ADC’s and by performing local autozeroing. Lag is eliminated by resetting the photodetectors after A/D conversion is performed. The MCBS ADC has two other important advantages. It can readily implement variable step-size quantization, e.g., for gamma correction or logarithmic compression. Moreover, the pixel-level circuits can be fully tested by applying electrical signals without any optics or light sources.

The rest of this paper is organized as follows. In Section II, we describe the operation of the MCBS ADC. In Section III, we discuss pixel circuit design and layout. Last we present measured results from a 320×256 image sensor with an MCBS ADC.

II. MCBS ADC OPERATION

The severe constraints on pixel area, fill factor, and power consumption preclude the use of well-established ADC techniques for pixel-level implementation. A desirable pixel area is in the range of 4–15 μm on a side, with fill factors exceeding

TABLE I
GRAY-CODE QUANTIZATION TABLE FOR THE $m = 3$ EXAMPLE

ADC Input Range	Codeword
0 — 1/8	0 0 0
1/8 — 1/4	0 0 1
1/4 — 3/8	0 1 1
3/8 — 1/2	0 1 0
1/2 — 5/8	1 1 0
5/8 — 3/4	1 1 1
3/4 — 7/8	1 0 1
7/8 — 1	1 0 0

25%. Traditional bit-parallel ADC techniques such as single slope require an m -bit latch at each pixel to implement m -bit conversion, which is not feasible for typical m values (even at 0.25- μm technology). On the other hand, bit-serial Nyquist-rate ADC’s such as successive approximation or algorithmic ADC require complex circuits with very precise and matched analog components. As a result, they are also not suited to pixel-level implementation, especially in a standard digital process.

Before describing the operation of our MCBS ADC, we make the following important observation. Note that an ADC maps an analog signal S into a digital representation (codeword) according to a quantization table. A 3-bit Gray coded example is given in Table I, where S is assumed to take on values in the unit interval (0, 1]. The table lists the assignment of each input range to a 3-bit codeword. The observation is that we can generate each bit of the codeword independently. For example, consider the generation of the least significant bit (LSB). From the table, the LSB is a one when $S \in (1/8, 3/8] \cup (5/8, 7/8]$ and a zero otherwise. To generate the LSB, any bit-serial Nyquist-rate ADC must be able to answer the following question: is $S \in (1/8, 3/8] \cup (5/8, 7/8]$? Thus, the ADC is essentially a one-detector that indicates the input ranges resulting in a one. The most natural way to implement this quantization table is to use a flash ADC. Fig. 1 depicts a 3-bit Gray-code flash ADC in which each bit of the codeword is independently generated. The most significant bit (MSB) is generated by comparing with a value of 1/2, whereas the LSB is generated by comparing with 1/8, 3/8, 5/8, and 7/8. Note that to generate the LSB, four clocked comparators and some decoding logic, which converts thermometer code into Gray code, are needed. This makes the flash ADC too large to fit in a pixel. Interestingly, a 1-bit comparator and a 1-bit latch can perform the same function as the seven clocked comparators in the flash ADC in a bit-serial fashion. The key to the operation is the judicious selection of the sequence of comparisons to be made.

A block diagram of a 1-bit comparator/latch pair is shown in Fig. 2. The waveforms in the figure illustrate how a comparator/latch pair performs bit-serial ADC. The analog signal S is connected to the positive terminal of the comparator, and the signal RAMP, which is an increasing staircase waveform, is connected to the negative terminal. The output of the comparator feeds into the gate of the latch, and the digital signal BITX connects to the data terminal of the latch. The

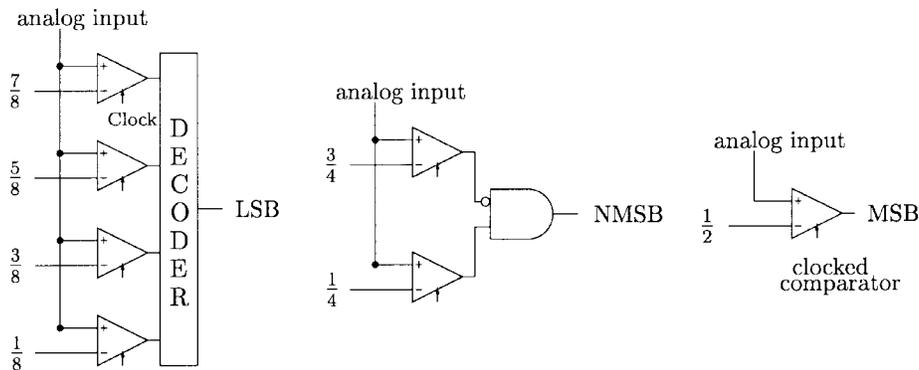


Fig. 1. Three-bit flash ADC.

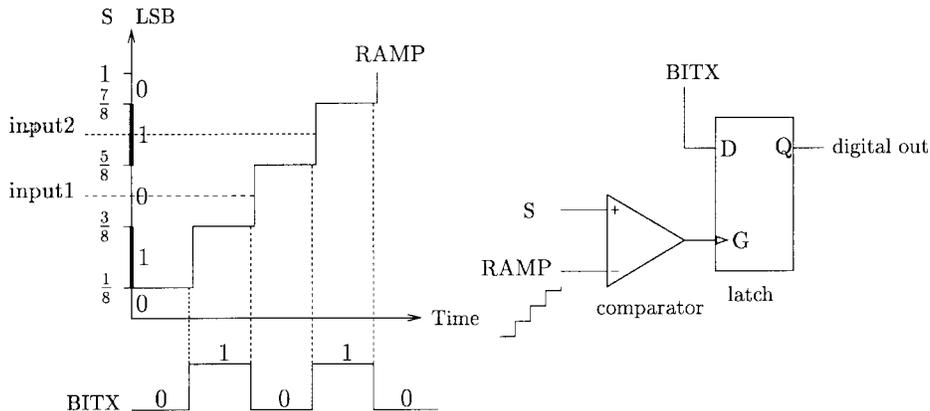


Fig. 2. Comparator/latch pair operation.

MSB can be generated in exactly the same manner as for the flash ADC by comparing S to a RAMP value of $1/2$. To generate the LSB, which requires four comparators in a flash ADC, is more challenging. We need to compare S to all four values ($1/8$, $3/8$, $5/8$, $7/8$) using a single comparator. To do so, RAMP starts at zero and monotonically steps through the boundary points ($1/8$, $3/8$, $5/8$, $7/8$). At the same time, as shown in the figure, BITX starts at zero and changes *whenever* RAMP changes.¹ As soon as RAMP exceeds S , the comparator flips, causing the latch to store the BITX value just after the RAMP changes. The stored value is the desired LSB. After the comparator flips, RAMP continues on, but since RAMP is monotonic, the comparator flips exactly once so that the latch keeps the desired value. For example, for input1, which is between $3/8$ and $5/8$, the comparator flips when RAMP steps to $5/8$, which is just above the input1 value, and BITX also changes to zero. When the comparator output goes low, a zero, which is the desired LSB, is latched. After that, RAMP continues to increase and BITX continues to change. Since the latch is closed, however, BITX can no longer influence the output. After RAMP completes stepping through the boundary points, the latched output is read out. Then RAMP and BITX are reset to zero in preparation for another sequence of comparisons. In this fashion, all bits from MSB to LSB are generated. The next most significant bit

(NMSB) is similarly generated by comparing input1 to $2/8$ and to $6/8$, which yields a one.

This 3-bit example can be easily generalized to perform any m -bit ADC. To quantize S to m bits of precision, the unit interval is divided into 2^m input ranges ($(i/2^m, (i+1)/2^m]$, $0 \leq i \leq 2^m - 1$), and each range is represented by an m -bit codeword. To determine the m -bit codeword for S , the ADC generates each bit serially (in any desired order). Each bit is generated by answering the question: is signal $S \in A$? where A is the set of input ranges that result in one. The ADC implements the question by successive comparisons at the boundary points of the ranges in A using the comparator/latch pair described. The RAMP signal steps through the boundary values monotonically, while BITX indicates the value (zero or one) of the particular range. At the end of each sequence of comparisons, the latched value is read out.

The number of comparisons performed for each bit varies, e.g., in the 3-bit example, generating the LSB requires four comparisons, the NMSB two comparisons, and the MSB only a single comparison. In general, for m bits of resolution, a total of at least $2^m - 1$ comparisons are needed. This is the case since for m bits of resolution, there are $2^m - 1$ boundary points. Clearly, the signal needs to be compared to each of these boundary points. The Gray code achieves this lower bound. Thus, in addition to being robust against single errors, the Gray code also minimizes the number of comparisons needed. Note that the MCBS ADC can easily implement virtually any quantization table, e.g., tables corresponding to logarithmic

¹To meet the setup time requirement of the latch, BITX must transition slightly before RAMP changes.

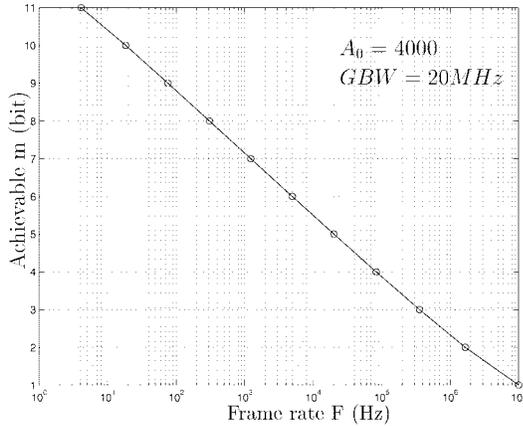


Fig. 3. Achievable bit resolution m versus frame rate F .

or gamma correction functions. The ADC operation remains exactly the same, except for the boundary points' being unequally spaced.²

The fundamental speed/resolution limit of the MCBS ADC is dictated by the comparator design. Assuming uniform quantization, the gain A_0 of the comparator must be at least 2^m . If the ADC sample rate is F Hz, then the time available for digitizing a sample is at most $1/F$ s, i.e., $1/F(2^m - 1)$ s per comparison. Therefore, the bandwidth (BW) of the comparator must be at least $F(2^m - 1)$, and the gain-bandwidth product (GBW) of the comparator must exceed $F(2^m - 1)2^m$. The achievable m values are plotted as a function of F in Fig. 3 for a comparator with gain $A_0 = 4000$ and $GBW = 20$ MHz. For this example, the comparator can achieve nine bits of resolution at 30 frames/s.

Thus far, we have shown that with only a single comparator/latch pair, full m -bit Nyquist-rate ADC can be implemented. However, we still need to generate the RAMP and the BITX signals using an m -bit digital-to-analog converter (DAC) and digital signal generation logic. If these complex circuits are included as part of the ADC, it would be too complex and too area consumptive to be of practical use. This ADC approach is, however, ideally suited for digitizing a very large number of signals in parallel, where the RAMP and BITX generation circuits can be shared. This is exactly the case for pixel-level ADC in an image sensor. In this application, we need to digitize hundreds of thousands of input channels in parallel, and we can only afford to have very simple circuits located at each pixel. The shared DAC and logic can reside at the periphery of the sensor where the area constraint is far less severe.

A block diagram of our MCBS ADC is shown in Fig. 4. It comprises multiple channels, each having its own comparator/latch pair. The m -bit DAC and the logic needed to generate RAMP and BITX are shared among all channels. The RAMP and BITX signals are broadcast to all channels, and the resulting bits are read out of each channel.

Note that the DAC can be eliminated by operating the MCBS ADC in a bit-serial "single-slope" mode. The input to the latch is the output of a global m -bit counter. The m -bit

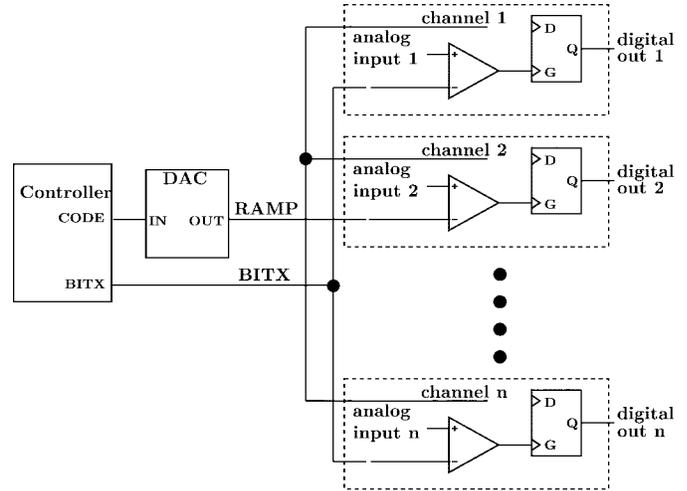


Fig. 4. MCBS ADC block diagram.

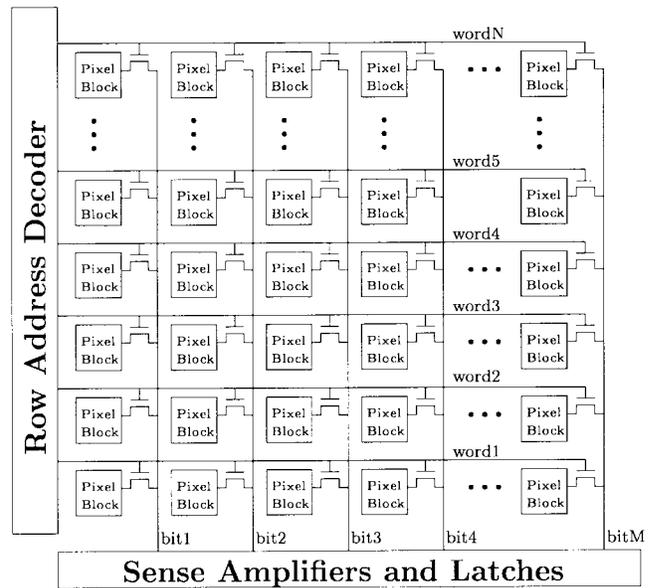


Fig. 5. Block diagram of an image sensor with pixel-level ADC.

latch in the standard single-slope implementation is replaced by a 1-bit latch and input (BITX) operating bit serially. In this mode, m continuous RAMP signals, simply generated using a current source and a capacitor, are provided. For each RAMP, BITX corresponds to the codeword values at a particular bit position in the quantization table. For the 3-bit Gray-code example discussed in Section II, to resolve the MSB, BITX sequences through 0-0-0-0-1-1-1-1; to resolve the second MSB, BITX sequences through 0-0-1-1-0-0-1-1; and to resolve the LSB, BITX sequences through 0-1-1-0-0-1-1-0. This single-slope variation of our MCBS ADC is slower and less programmable.

The readout architecture of an image sensor with MCBS ADC is shown in Fig. 5. It consists of a two-dimensional array of pixel blocks, a row decoder, and column sense amplifiers. Each pixel block comprises one or more photodetectors sharing an MCBS ADC channel. The RAMP and BITX generation circuitry, which lie outside the image sensor array, are not

²In this case, the RAMP signal should have higher precision than m .

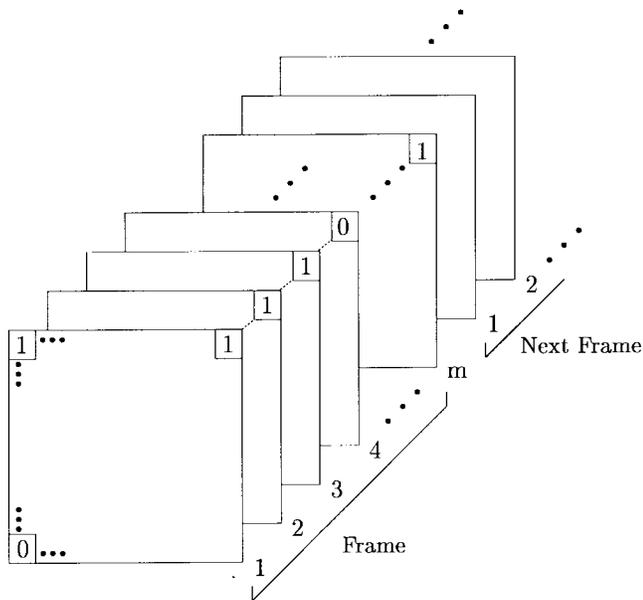


Fig. 6. Bit planes generated by pixel-level ADC.

TABLE II
320 × 256 AREA IMAGE SENSOR CHARACTERISTICS

Technology	0.35 μm , 4-layer metal, 1-layer poly, nwell CMOS
Sensor Area	3973 $\mu\text{m} \times 2921 \mu\text{m}$
Die size	4.14mm \times 5.16mm
Pixel Area	10.5 $\mu\text{m} \times 10.5 \mu\text{m}$
Transistors per pixel	4.5 (18 per four pixels)
Fill Factor	28%
Package	144 pin PGA
Supply Voltage	3.3 v
Sensor power consumption	20 mW
SNR (after quantization)	48dB

shown in the figure. The captured analog pixel values are digitized in parallel one bit at a time. Each latched set of bits forms a bit plane, which is read out in a manner similar to a standard digital memory, using the row decoder and the column sense amplifiers. A set of bit planes constituting an m -bit frame is depicted in Fig. 6, where the digitized upper right-hand-corner pixel value is 1110, \dots , 1. Note that this image output format is quite different from the raster-scan format commonly used in charge-coupled devices and analog CMOS image sensors, e.g., APS. However, it offers certain advantages such as programmable pixel resolution and region of interest windowing.

III. A 320 × 256 IMAGE SENSOR

A 320 × 256 image sensor with the MCBS ADC was designed and fabricated in a 0.35- μm CMOS process. The chip consists of a 160 × 128 array of 2 × 2 pixel blocks, each sharing a 1-bit comparator/latch pair circuit, a row decoder, column sense amplifiers, and multiplexers. The main characteristics of the chip are listed in Table II. Since each pixel-level ADC is multiplexed among four pixels, the sensor

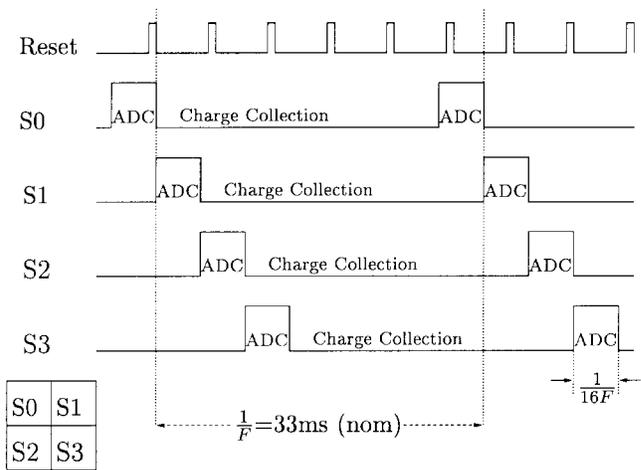


Fig. 7. A frame is converted one quarter frame at a time.

outputs one quarter frame at a time. Each quarter frame is read out one bit plane at a time as described in [14].

In the following section, we describe the pixel circuit design. Results obtained from the sensor are discussed in Section III-B.

A. Pixel Circuit Design

Before we describe the circuit design, we first discuss the design criteria used.

- We chose the pixel size to be 10 × 10 μm^2 with a fill factor of 25%. This severely limited the number of transistors per pixel to less than six, and the number of external wires (e.g., bias, control, supply) to around 14. This dictated that we multiplex each ADC among four neighboring pixels [14].
- We chose the maximum ADC resolution to be $m = 10$ bits for still imaging and $m = 8$ bits for video. This set a lower bound on the required comparator gain $3.3/2 \times 2^{10} = 1690$ for still and 423 for video assuming a 3.3-V power supply and a 2-V input swing. Thus, the minimum dc comparator gain needed is $A_0 = 1690$.
- We wanted the sensor to operate in video mode at a maximum frame rate of $F = 30$ frames per second. We also decided to limit the total conversion time, including the time required to read out a quarter bit plane, to $1/16F = 2.08$ ms, as illustrated in Fig. 7. Since the readout time for a quarter bit plane is on the order of a few microseconds, it can be neglected. Thus, the time per comparison is $1/16F(2^m - 1) = 8.17 \mu\text{s}$, which means that the bandwidth of the comparator must be at least 122 kHz. Combining this bandwidth requirement with the gain requirement, we get a GBW product for the comparator of at least 50 MHz.
- Since there are hundreds of thousands of ADC's operating simultaneously, albeit at very low speed, power consumption for each ADC must be minimized.
- To reduce offset fixed pattern noise (FPN) and $1/f$ noise, we decided that a form of correlated double sampling (CDS) must be used.

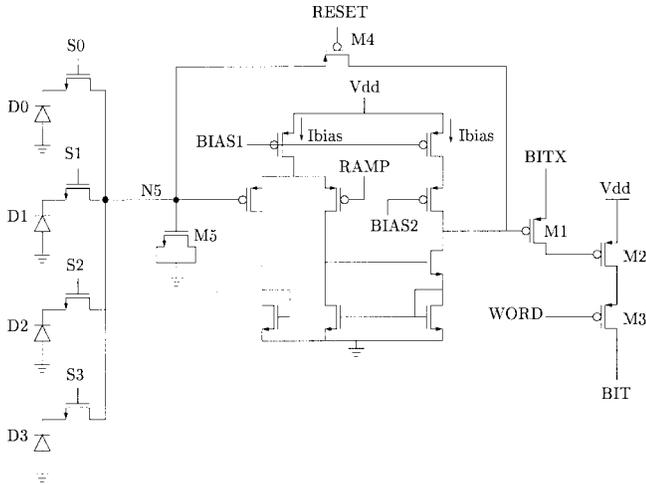


Fig. 8. Four pixels sharing a comparator/latch pair.

- We decided that it must be possible to electrically test the pixel circuit. Relying on light only to test the circuit would be significantly more costly.

To satisfy the criterion of low power consumption, we had two options: to operate the comparator above threshold and switch it off when it is not in use or to operate it in subthreshold. We chose the latter, since an MOS transistor achieves its maximum gain in subthreshold, where the current is very low. Recall that the gain of a single stage MOS amplifier in subthreshold is $\kappa q V_{\text{early}}/KT$ [20], where V_{early} , the early voltage of the transistor, depends on the process and varies inversely with the transistor length; κ (≈ 0.6) is the gate efficiency of the transistor; and KT/q is the thermal voltage. Since our comparator must have gain $G \geq 1690$, we must have V_{early} of at least 69 V. This requires using an impractically long transistor. Hence, we decided to use a two-stage amplifier with $V_{\text{early}} \approx 1.6$ V per stage. To find the amplifier bias current i required to achieve the desired gain-bandwidth product, we use the rough formula $GBW \approx g_m/C$, where $g_m = \kappa i q/KT$ and C is the load capacitance. Since capacitances within a pixel are on the order of few tens of femtofarads, the required i is only a few nanoamperes, which is well within the range of current in subthreshold.

There are two topologies from which to choose in two-stage amplifier design: classical two-stage and cascode. Since we decided to implement CDS at the pixel, feedback must be incorporated in the comparator, i.e., the comparator must operate both as a comparator and as an op-amp. In the classical two-stage topology, a Miller compensation capacitor is typically required to stabilize the comparator operating in the feedback mode. It is, however, difficult to implement the floating Miller compensation capacitor in a single poly digital CMOS process. As a result, we chose to use the cascode topology whose compensation capacitor is its output load.

A circuit schematic of four pixels sharing an MCBS channel is shown in Fig. 8. The circuit uses 18 transistors. The comparator consists of a transconductance amplifier followed by a Wilson current mirror and a cascode output load. It is biased to operate in subthreshold to maximize gain and minimize power. The latch operates as a 2T DRAM cell, where M1 is

the write-port pass transistor and M2 is the read-port buffer. Pixel nonuniformity is reduced by sharing the circuits that generate the global signals, which constitute the most complex ADC circuits. We use PMOS transistors as much as possible to reduce the potential for impact ionization noise that can adversely affect the photodetectors and to minimize $1/f$ noise.

Each conversion begins by sampling a photodiode voltage through the analog multiplexer, using **S0**, **S1**, **S2**, or **S3**, to the gate capacitance of M5. The resulting voltage on the gate of M5, v_5 , is

$$v_5 = V_{\text{reset}} - V_{\text{photo}} \frac{C_d}{C_d + C_{gs5}}$$

where V_{reset} is the photodiode reset voltage, V_{photo} is the photon- (and dark current)-induced photodiode voltage, C_d is the effective photodiode junction capacitance, and C_{gs5} is the gate capacitance of M5. This, of course, assumes that v_5 is greater than the threshold voltage of M5. The RAMP signal is applied to the positive input of the comparator. The BITX signal is used as the input to the latch. When the comparator changes state, the last value of BITX is stored in the latch. After each RAMP sequence, one bit is read out of the latch. At the end of conversion, the pixel is reset by turning on M4 and the appropriate photodiode select device. This allows the comparator to operate as an op-amp with unity-gain feedback, so that the reset voltage plus the comparator offset is stored on the selected photodiode. This reset feature also allows complete electrical testability of the ADC. To test the ADC, the photodetectors are disconnected by turning off all select transistors. The comparator/latch pair input (node N5 in Fig. 8) is then set to the desired RAMP value by turning on M4, and its output is read out.

Assuming subthreshold operation and that the early voltage and gate efficiency of all the transistors are the same, it can be shown that the gain of the comparator is approximately

$$A_0 = \frac{1}{6} \left(\frac{V_{\text{early}} \kappa}{\frac{KT}{q}} \right)^2$$

It can also be shown that the gain-bandwidth product of the comparator is approximately

$$GBW = \frac{\kappa I_{\text{bias}}}{4\pi \frac{KT}{q} C}$$

where I_{bias} is the tail current of the differential pair and C is the load capacitance. Substituting for $I_{\text{bias}} = 190$ nA, $C = 7$ fF, and $V_{\text{early}} = 10$ V, we get $A_0 = 8900$ and $GBW = 50$ MHz at room temperature. Clearly, GBW can be increased by increasing I_{bias} . The comparator has a simulated gain of $A_0 = 4000$. The simulated gain is significantly lower than the calculated value because of the simplifying assumptions used in deriving the equation.

Gain FPN due to the ADC circuit is minimized by sharing the circuits that generate the global signals RAMP and BITX. Offset FPN arises from two sources: comparator offset and variation in analog switching feedthrough. The FPN due to

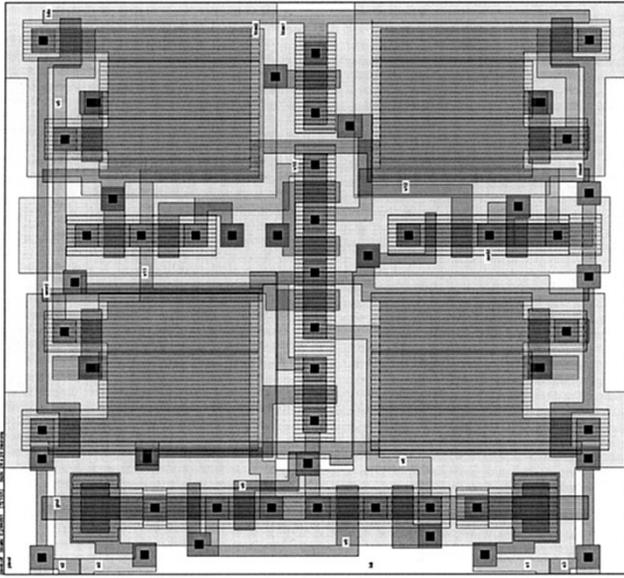


Fig. 9. Layout of a 2×2 pixel block. The photodiodes are the large square gray areas. The select transistors are placed next to the photodiodes. The PMOS transistors are located in the cross area between the photodiodes, whereas the NMOS transistors are placed at the bottom of the block. The hold capacitor M5 is made out of the two large NMOS transistors in the bottom area.

comparator offset is reduced using autozeroing, which is accomplished by storing the offset value on the photodiode capacitor during reset. Offset FPN due to switching feedthrough of M4 is reduced using M5. The residual photodiode referred offset error charge is given by

$$q_{\text{error}} = \left(-\frac{V_{\text{offset}} + V_{\text{reset}}}{1 + A_0} + \frac{V_{\text{dd}}C_{\text{ov4}}}{C_d + C_{\text{gs5}} + C_{\text{ov4}}} + \frac{\alpha C_{\text{ox4}}W_4L_4(V_{\text{reset}} - V_{\text{tp4}})}{C_d + C_{\text{gs5}}} \right) (C_d + C_{\text{gs5}})$$

where V_{offset} is the offset voltage of the comparator, A_0 is the open loop gain of the comparator, α is the proportion of M4's channel charge that is transferred to the gate of M5, C_{ov4} is the overlap capacitance of M4, W_4 is the width of M4, L_4 is the length of M4, and V_{tp4} is the threshold voltage of M4. The formula confirms the intuition that reducing the capacitance C_{gs5} of the sense node N5 reduces the error charge. The capacitance C_{gs5} , however, cannot be made too small. To ensure the reliable operation of the MCBS ADC, the input signal must remain constant throughout conversion, and thus drooping at N5 must be minimized. More specifically, the worst case drooping must be less than half an LSB, which sets a lower bound on the size of C_{gs5} .

The layout of a 2×2 pixel block is shown in Fig. 9. The layout is symmetrically organized to reduce fixed pattern noise among the four pixels and to ensure uniform spatial sampling. This includes using identical geometry photodiodes with equal spacings among them, implementing capacitor M5 using four symmetrically placed MOS transistors, and ensuring that the photodiodes have very similar wire and transistor surroundings. The effect of pixel circuit-induced

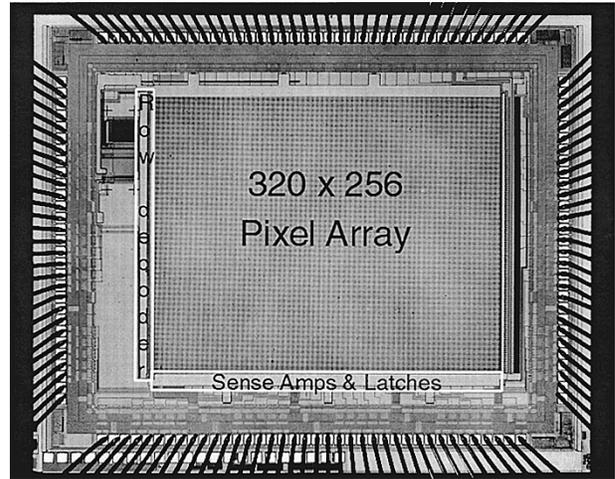


Fig. 10. Photomicrograph of the CMOS image sensor chip.

substrate noise, e.g., impact ionization noise, on the $n^+ - p_{\text{sub}}$ photodiodes is minimized by using PMOS transistors (in an n-well) whenever possible. To prevent light-induced currents from affecting the analog circuitry or causing latchup, we used fourth-level metal as a light shield everywhere except over the photodetectors.

B. Testing and Results

The 320×256 image sensor chip has a total of 144 pins: 32 are used to output the digital image data, 17 are used as analog inputs to drive the ADC signals and to set the biases, and the rest of the pins are digital inputs that provide the addresses and other control signals needed for readout. Most of the input pins can be eliminated by on-chip signal generation, i.e., by integrating the DAC, bias generation, and address generation on the chip. A photomicrograph of the image sensor chip is shown in Fig. 10.

To test the chip, we built two test boards. The first is the device under test (DUT) board, which includes the sensor, a 16-bit DAC for generating the RAMP signal, and RS422 chips for input and output interface. The board also includes level shifters and other analog bias generators to provide the analog input signals to the chip. The output of the DUT board is captured by a peripheral component interconnect digital frame grabber board that resides in a PC. The second board we built is a pattern generation board. It drives the digital inputs to the DUT board. The board is controlled by a PC via its parallel port. To drive the DUT board, we designed a microcontroller, which was implemented using a field-programmable gate array. To capture data from the sensor, we download the appropriate program into the microcontroller memory.

To capture an image, we used a motorized lens to provide the needed focus. The microcontroller generates all the needed input patterns to control the image sensor and to read its output into the digital capture board. The image is then reformatted for display. Fig. 11 shows an 8-bit image captured by the image sensor with no digital processing such as offset FPN correction, gamma correction, or histogram equalization performed.



Fig. 11. A 320×256 image.

In addition to capturing images, the setup is used to perform the electrical testing described in Section III. Using the electrical testability feature, an ADC transfer curve was obtained. The ADC measured integral and differential nonlinearities are 2.3 and 1.2 LSB at 8 bits, respectively. The measured standard deviations of the pixel gain and offset FPN due to ADC are 0.24 and 0.2%, respectively. The ADC performance did not meet our design criteria due to unexpectedly high threshold voltage mismatch that significantly reduced our comparator gain. This problem can be easily overcome by slightly altering the comparator transistor sizes.

The setup is also used to measure sensor characteristics such as its spectral response, noise, fixed pattern noise, and modulation transfer function. For these measurements, we use a more sophisticated optical set up consisting of a dc regulated tungsten halogen light source, a monochromator, focusing lenses, and an integrating sphere. The output of the integrating sphere is used to provide the needed illumination to the sensor. All of the electrical equipment and the monochromator are IEEE488 (GPIB) programmable. We used very tightly regulated power supplies to reduce noise.

IV. CONCLUSION

We have introduced the first viable Nyquist-rate pixel-level ADC technique. The ADC uses very simple and robust circuits, which can be implemented in a standard CMOS process. The ADC results in very low FPN and can be fully tested electrically. We presented a 320×256 CMOS image sensor with pixel-level MCBS ADC implemented in $0.35\text{-}\mu\text{m}$ technology. The results demonstrate that the ADC achieves a high enough level of performance for image sensor applica-

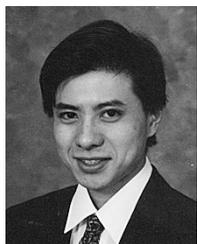
tions. The DAC and the control logic needed to generate the ADC signals can be readily integrated with the image sensor. Since the DAC is relatively low speed (120 kSamples/s), integrating it on-chip should not be a major challenge.

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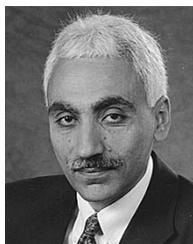
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