6.1 A 10kframe/s 0.18µm CMOS Digital Pixel Sensor with Pixel-Level Memory

Stuart Kleinfelder, SukHwan Lim, Xinqiao Liu, Abbas El Gamal

Stanford University, Stanford CA

In a digital pixel sensor (DPS), each pixel has an ADC, all ADCs operate in parallel, and digital data is directly read out of the image sensor array as in a conventional digital memory [1]. The DPS architecture offers several advantages over analog image sensors including better scaling with CMOS technology due to reduced analog circuit performance demands and elimination of column fixed-pattern noise and column readout noise. With an ADC per pixel, massively-parallel conversion and high-speed digital readout become possible, completely eliminating analog readout bottlenecks. This benefits traditional high-speed imaging applications and enables imaging enhancement capabilities such as multiple sampling for increasing sensor dynamic range [2]. Achieving acceptable pixel sizes using DPS, however, requires the use of a 0.18µm or below CMOS process, which is challenging due to reduced supply voltages and increased leakage currents [3].

This 352x288 CMOS DPS with pixel-level digital memory is fabricated in a standard digital 0.18µm CMOS technology. The objectives of our design are: (i) to explore image sensor design in a 0.18µm technology and demonstrate the scalability potential of DPS, (ii) to demonstrate the high frame rate potential of DPS by breaking both the 1G-pixels/s and the 10kframe/s (fps) continuous full frame parallel ("snap-shot") image acquisition speed milestones, and (iii) to explore the benefits of pixel-level digital memory, e.g., pipelining for faster readout and focal-plane processing.

A block diagram of the DPS chip is shown in Figure 6.1.1. The core is a 352x288 array of pixels, each containing an nMOS photogate circuit, a comparator, and an 8b memory. The input-related periphery consists of an 8b Gray code counter, column drivers and multiplexers. Control periphery includes row-select pointer for addressing the pixel-level memory, comparator power down circuits, and timing control and clock generation circuits. Output periphery includes column sense-amps for reading the pixel-level memory, and an output multiplexing shift register.

Sensor operation can be divided into four main phases: reset, integration, ADC, and readout (Figure 6.1.2). At low to moderate frame rates (<5kframe/s) much flexibility can be exercised regarding chip timing. For example, all phases can be kept separate to prevent noise due to analog to digital conversion and readout from corrupting the analog signals during charge integration and reset. Digital CDS can also be performed externally with an additional A/D conversion and readout immediately after reset. When operating at the highest speeds (>5kframe/s), it may be important to maximize integration time to collect as much light as possible. In this case, the reset and integration phases of each frame can be overlapped with the readout of the previous frame.

Pixel-level single-slope A/D conversion is performed simultaneously for all pixels after standard photogate integration and charge transfer. The analog ramp signal is generated off-chip and globally distributed to the pixel-level comparators. The 8b Gray-coded digital ramp sequence is generated by the on-chip counter and distributed via the memory bit lines. Each comparator fires as the ramp exceeds its signal value and the corresponding digital code is latched into the pixel-level memory. Alternatively, a digital ramp sequence that is generated off-chip can be used, allowing other conversion strategies such as logarithmic compression and expansion.

The pixel values are read out of the memory one row at a time using the read row-pointer and column sense-amps. Each row is then shifted out, while the next row is read out of the memory. To reach over 1Gpixels/s sustained throughput a 64-bit-wide readout bus operating at 167MHz is used. The readout operation is coordinated by on-chip control logic operating off of a frame reset strobe and a single clock. Since full-frame conversion and readout can be accomplished in under 100µs, average power consumption may be significantly reduced at low frame rates by powering down the comparators using on-chip digitally controlled power-down circuitry.

Each pixel includes an nMOS photogate, transfer and reset gates, a storage capacitor, a three-stage comparator, and 8b 3T dynamic memory cells (Figure 6.1.3). The photogate is used to achieve acceptable conversion gain. Thick oxide 3.3V transistors are used for the photogate, transfer gate, storage capacitor, and reset transistors to combat the high gate and sub-threshold leakage currents and the low supply voltage problems of the thin oxide 1.8V transistors. The comparator consists of a differential amplifier stage followed by two single-ended gain stages. It provides 10b resolution at an input swing of 1V and worst case settling time of 80ns. This provides the flexibility to perform 8b A/D conversion down to 0.25V range in ~25µs, which is needed for high-speed, low light, operation. The 3T DRAM is designed for 10ms maximum data hold time. This requires the use of large gate length access transistors and holding the bit lines around Vdd/2 to combat the high transistor off-currents. Single-ended charge-redistribution column sense-amps are used for robustness against voltage coupling between the closely spaced bit lines. The comparator and pixel-level memory circuits can be electrically tested by applying analog signals to the sense node through the "Reset Voltage" signal, performing A/D conversion and reading out the digitized values.

Figure 6.1.4 summarizes the main chip and sensor characteristics and performance. Figure 6.1.5 shows a typical image taken using ~1ms integration time (1kframe/s), while Figure 6.1.6 shows a sample image sequence taken at 10kframe/s, or >1G-pixels/s continuous rate. It depicts a propeller rotating at ~2200 rpm in front of a motionless resolution chart, where every tenth frame is shown. A die micrograph is shown in Figure 6.1.7.

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References:
[1] A. El Gamal, D. Yang, and B. Fowler: "Pixel level Processing - Why?, What?, and How?" Proceedings of SPIE vol. 3650, pp. 2-13, Jan. 1999.
[2] D. Yang et al., "A 640x512 CMOS Image Sensor with Ultra Wide Dynamic Range Floating Point Pixel-Level ADC, " Journal of Solid State Circuits, vol. 34, no. 12, pp. 1821-1834, Dec. 1999.
[3] H.-S. Wong, "Technology and Device Scaling Considerations for CMOS Imagers," IEEE Transactions on Electron Devices, vol. 43, no. 12, pp. 2131-2141, 1996.

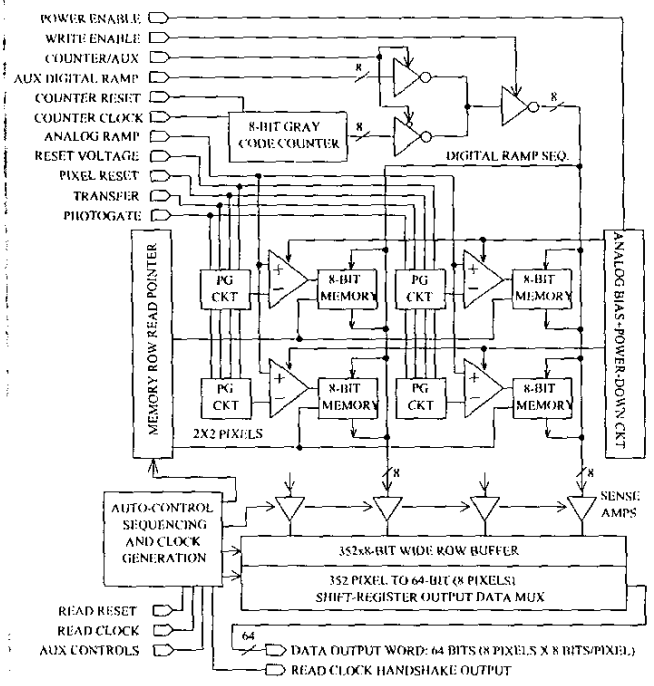

Figure 6.1.1: DPS block diagram.

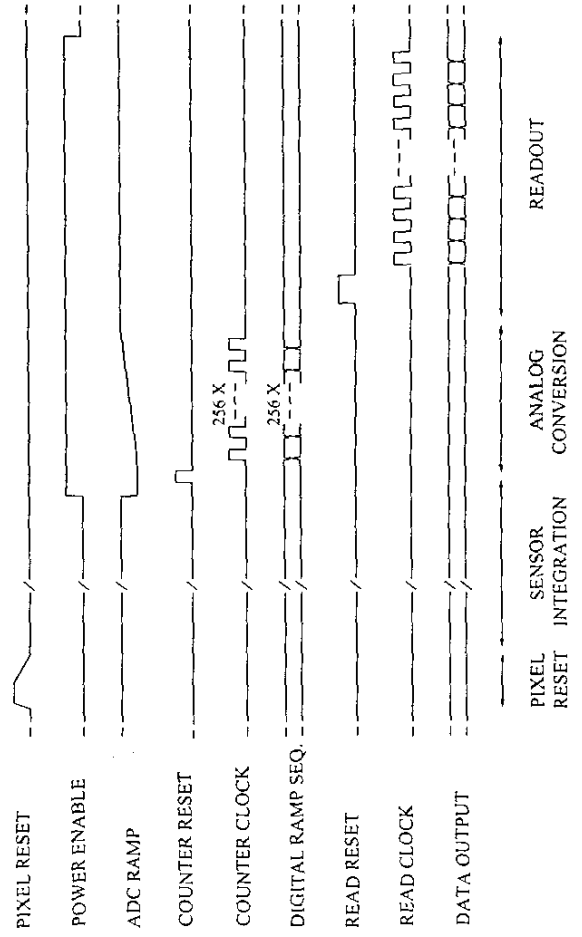

Figure 6.1.2: Simplified timing diagram (photodiode mode).

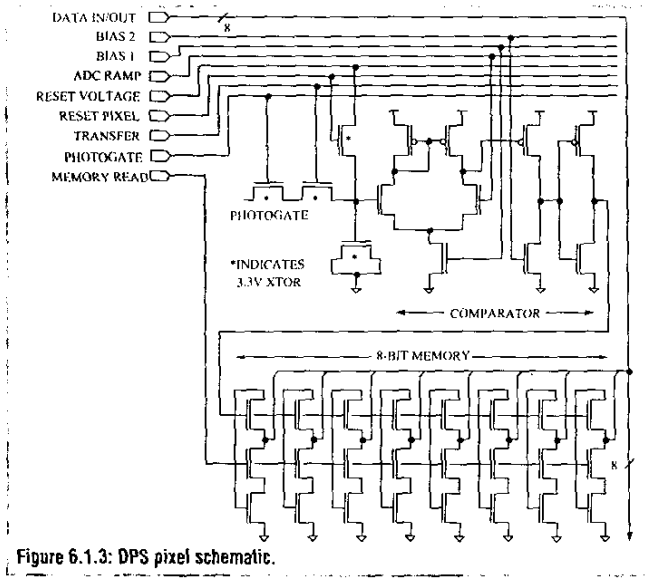

Figure 6.1.3: DPS pixel schematic.

Technology:	0.18 µm 5-metal CMOS
Die size:	5 mm by 5 mm
Array size:	352 by 288 (CIF)
Number of Transistors:	~3.8 million
Output readout architecture:	64-bit bus @ 167MHz
Maximum sustained output rates:	>1 Gpixel/s, >10,000 fps
Power dissipation, max @ 10K fps:	~50 mW
Pixel size:	9.4 µm by 9.4 µm
Photodetector type:	nMOS Photogate
Sensor fill factor:	15 %
Transistors per pixel:	37 incl. photogate and cap.
ADC architecture:	Pixel-level 8-bit single-slope
ADC typical range and conversion time:	1 V, ~25 µs
ADC integral non-linearity:	0.22% (0.56 LSB)
Dark current:	130 mV/s; 10 nA/cm^2
Conversion gain:	13.1 µV/e-
Sensitivity:	0.107 V/lux.s
FPN, rms in dark with CDS, 1K fps:	0.027% (0.069 LSB)
Temporal noise, rms, dark, CDS, 1K fps:	0.15% (0.38 LSB)

Figure 6.1.4: DPS specifications and performance.

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Die Size	5.5mm × 5.5mm
Technology	0.25-µm SiGe BiCMOS (f_T = 52GHz, f_{max} = 70GHz)
Supply Voltage	3.3V
Power Dissipation	1.3W (output clock disabled) 1.6W (data + clock)
Output Data Rate	9.953-10.664Gb/s
Jitter Generation	$0.048UI_{P-P}$
Max. Jitter Peaking	0.04dB (PLL BW = 6MHz)
Input Data Phase Drift Tolerance	±1.5UI (±2.4ns @ 622Mb/s)
Input Flip-Flop t_{su}+t_h	<200ps

Figure 5.4.7: Chip characteristics.

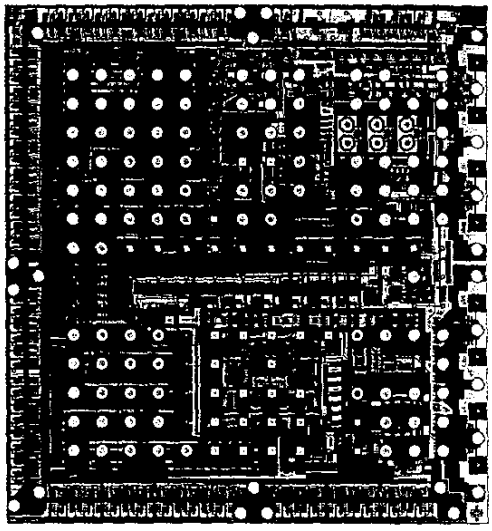
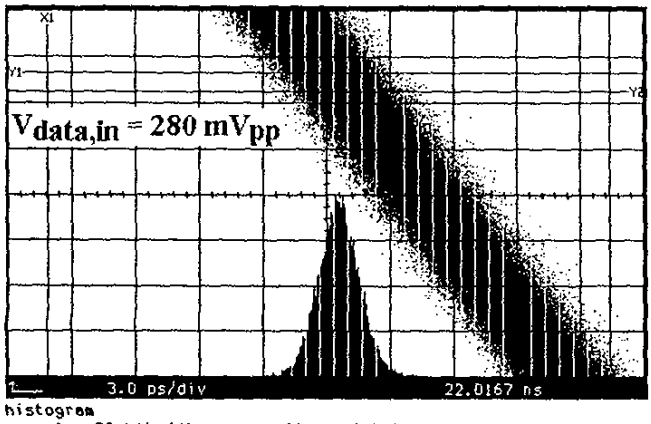


Figure 5.5.7: Chip micrograph.



histogram

scale	88 hits/div	offset	0 hits		
mean	22.03230 ns	median	22.03233 ns	µ±1σ	71.9%
std dev	981.39 fs	hits	10.69 khits	µ±2σ	95.7%
p-p	8.13 ps	peak	352 hits	µ±3σ	99.5%

Figure 5.6.6: Jitter histogram of recovered clock.

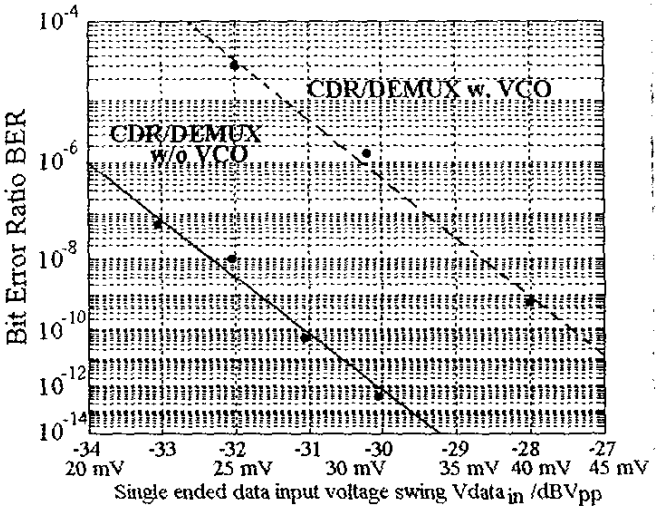


Figure 5.6.7: BER measurement.

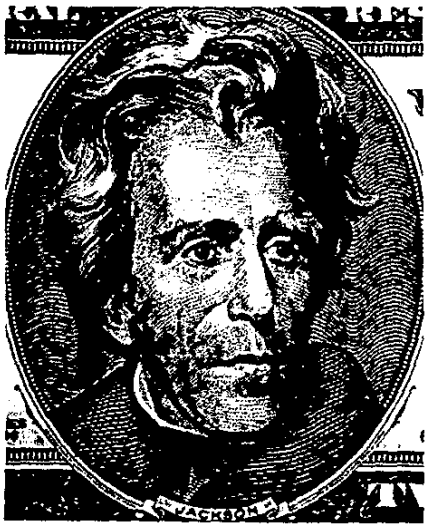


Figure 6.1.5: Sample image at 1kframe/s.

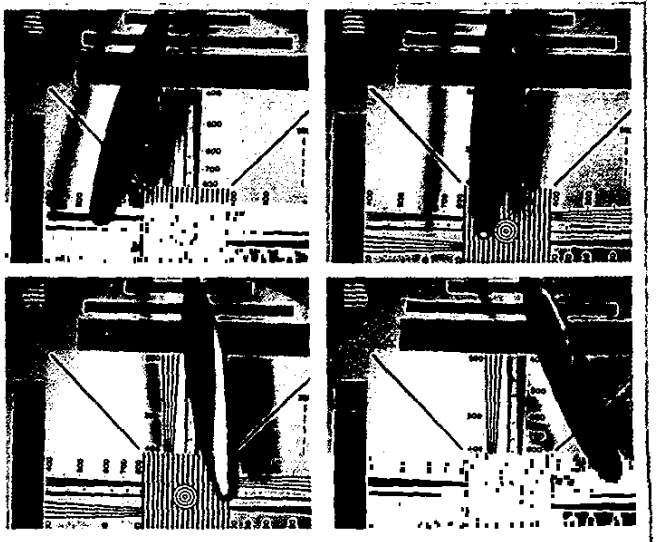


Figure 6.1.6: Video sequence at 10kframe/s, every 10th frame.

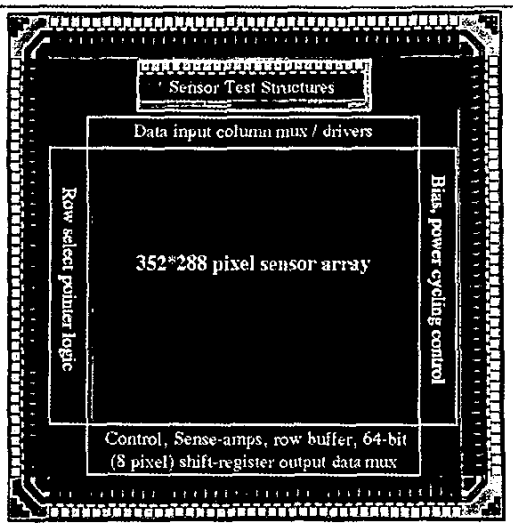


Figure 6.1.7: DPS die micrograph.

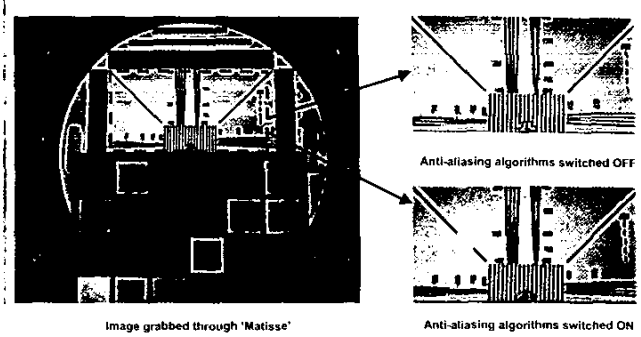


Figure 6.2.5: Reproduced picture effect of anti-aliasing.

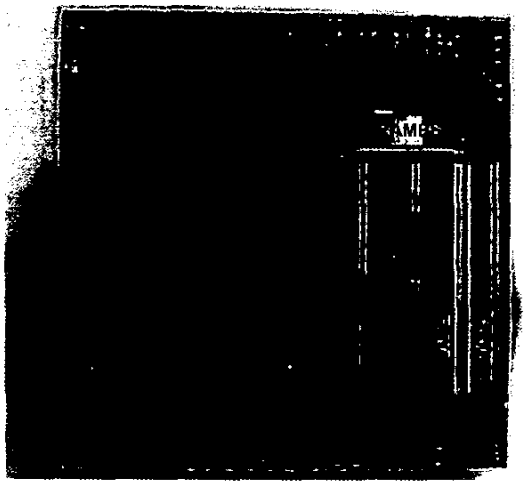


Figure 6.2.6: Sensor die micrograph.

Total module size	10mm x 10mm x 7mm
Lens field of view (horizontal)	54°
Lens aperture (f#)	2.8
Lens effective focal length	2.7mm
Lens focus	30cm - Infinity
Lens optical track	4.9mm
Lens storage range	-40°C - +85°C
Sensor die size	5.5mm x 5.49mm
Sensor technology	0.5µm 2P3M
Pixel size	7.5µm x 7.5µm
Fill factor	70%
Sensitivity (green channel)	2.1V1ux $^{-1}$s $^{-1}$
Quantum efficiency @ 550 nm	60%
Dark current	250pAcm $^{-2}$
Conversion gain	40µV/e
Dynamic range	57dB
Photon shot noise SNR	42dB
Random noise	42e
Column FPN	43e
Dark current FPN	21e
Programmable gain	18dB
ADC resolution	10Bit
Sensor power consumption (@ 2.8V)	32mW
Coprocessor die size	2.435mm x 2.281mm
Coprocessor technology	0.18µm 1P6M
Coprocessor gate count	100k
Coprocessor RAM bit count	64000
Coprocessor clock speed	4.5MHz
Coprocessor power consumption (@ 1.8V)	15mW
Module power consumption (@ 2.8V)	50mW

Table 6.2.1: Module performance.

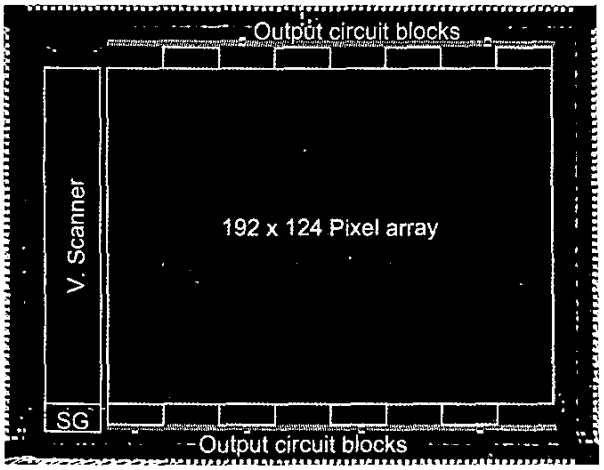


Figure 6.4.7: Chip micrograph.

Clock	**20MHz**
Power Supply	**3.3V**
Technology	**0.6um 3-Metal CMOS**
Chip Size	**5.8 x 12.6 mm^2**
Pixel Array	
Number of Pixels	**128 x 128**
Pixel Size	**18 x 18µm^2**
Processor	
Number of PE	**4x128**
PE Size	**18 x 1200 µm^2**

Table 6.5.1: Chip overview.

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