Active Pixel Sensors Fabricated in a Standard 0.18 um CMOS Technology

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ABSTRACT

CMOS image sensors have benefited from technology scaling down to 0.35μm with only minor process modifications. Several studies have predicted that below 0.25μm, it will become difficult, if not impossible to implement CMOS image sensors with acceptable performance without more significant process modifications. To explore the imaging performance of CMOS image sensors fabricated in standard 0.18μm technology, we designed a set of single pixel photodiode and photogate APS test structures. The test structures include pixels with different size n+/pwell and nwell/psub photodiodes and nMOS photogates. To reduce the leakages due to the in-pixel transistors, the follower, photogate, and transfer devices all use 3.3V thick oxide transistors. To achieve higher voltage swing, the reset devices also use thick oxide transistors. The paper reports on the key imaging parameters measured from these test structures including conversion gain, dark current and spectral response. We find that dark current density decreases super-linearly in reverse bias voltage, which suggests that it is desirable to run the photodetectors at low bias voltages. We find that QE is quite low due to high pwell doping concentration. Finally we find that the photogate circuit suffered from high transfer gate off current. QE is not significantly affected by this problem, however.

Keywords: CMOS APS, image sensor, dark current, quantum efficiency, photodiode, photogate

1. INTRODUCTION

CMOS image sensors have benefited from technology scaling down to 0.35μm. Scaling has made it possible to reduce pixel size, increase fill factor, and integrate more analog and digital circuitry with the sensor on the same chip. These benefits have been achieved with only minor modifications to standard CMOS processes aimed mainly at reducing their photodiode dark currents. Several studies[1] have predicted that below 0.25μm, it will become difficult, if not impossible to implement CMOS image sensors with acceptable performance without more significant process modifications. At 0.18μm technology, shallow trench isolation (STI) is widely used, retrograde wells with high doping concentrations are standard, and gate oxide thickness drops to around 3nm. These process features result in dramatic increase in leakage currents and decrease in quantum efficiency (QE) and voltage swing.

To explore the imaging performance of CMOS image sensors fabricated in standard 0.18μm technology, we designed and prototyped a set of single pixel photodiode and photogate APS test structures. The test structures include pixels with different size n+/pwell and nwell/psub photodiodes and nMOS photogates. To reduce the leakages due to the in-pixel transistors, the follower, photogate, and transfer devices all use 3.3V thick oxide transistors. To achieve higher voltage swing, the reset devices also use thick oxide transistors.

The paper will report on the key imaging parameters measured from these test structures including conversion gain, dark current and spectral response. The results confirm the poor imaging performance predicted by the earlier studies.

- As predicted, we find that all photodetectors, especially the nwell photodiode, have unacceptably high dark currents. However, we find that dark current decreases super-linearly in bias voltage, which suggests that it is desirable to run the photodetectors at low bias voltages.

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- The n+/pwell photodiode and nMOS photogate quantum efficiencies are lower than expected, possibly due to the high pwell doping concentration.
- In spite of implementing the transfer device of the photogate APS using thick oxide transistor, we were not able to turn it completely off during integration without applying negative voltage to its gate. However, this problem did not have a significant effect on the photogate imaging parameters.

In the following Section 2 we describe the design of our test structures. The experimental setup and measured results are reported in Section 3.

2. TEST STRUCTURE DESIGN

The main challenge in the design of CMOS image sensors has been the high junction leakage currents of standard CMOS processes. As technology scaled down to 0.18μm, transistor off-current and low supply voltage have begun to present new challenges requiring further modifications to standard CMOS processes. At 0.18μm technology, the transistor gate oxide thickness begins to reach direct tunneling.[2] At gate oxide thicknesses around 3nm gate current density i_{gate} (see Figure 1) can be five orders of magnitude higher than acceptable photodiode dark current densities. Gate current density, however, is a strong function of v_{gb}. As shown in Figure 1, when v_{gb} drops from 1.8V to 1.0V, the gate current density drops by two orders of magnitude.

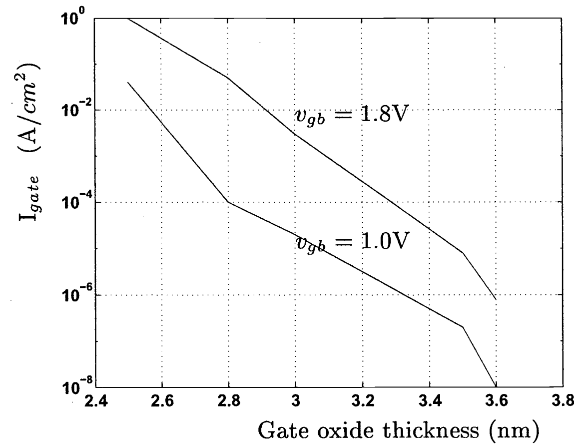

Figure 1. Transistor gate tunneling current i_{gate} as a function of gate oxide thickness at $v_{gb} = 1.8\text{V}$ and $v_{gb} = 1.0\text{V}$.[2]

This high gate leakage current presents a new challenge to image sensor design in 0.18μm technologies and below. In the standard APS pixel circuit, the photodiode is directly connected to the gate of the source follower transistor. The gate leakage current during integration can be higher than photodetector dark current – even comparable to photocurrents under normal lighting conditions. For a photogate APS the effect of gate current can be even more pronounced, since the photogate area is quite large.

One way to mitigate the transistor gate leakage problem is to design all image sensor circuits using the 3.3V thick oxide transistors used in the design of chip I/O buffers. This does not, however, take full advantage of technology scaling. Thick oxide transistors occupy larger area and have higher threshold voltage than thin oxide transistors. Instead, in the design of our test structures we used the thin oxide transistors as much as possible to achieve small area and use the thick gate oxide transistors to ensure low leakage and achieve high voltage swing.

The test structures include pixels with different size n+/pwell and nwell/pwell photodiodes and nMOS photogates. Circuit schematics of the photodiode and photogate test structures are shown in Figures 2. Note that the drain of the reset transistor is not tied to v_{dd} but is connected to the signal v_{set}. This makes it

possible to accurately test the readout circuit response and to achieve wider voltage swings. The operation of the circuits is otherwise standard and will not be described here. Figure 3 is a photomicrograph of the test structures portion of our 0.18μm chip.

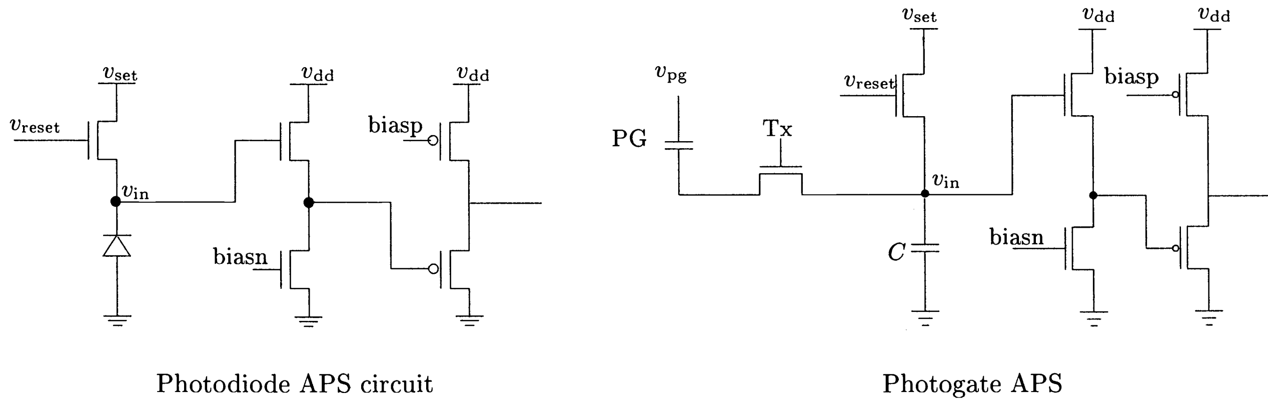

Figure 2. Test Structure Circuits

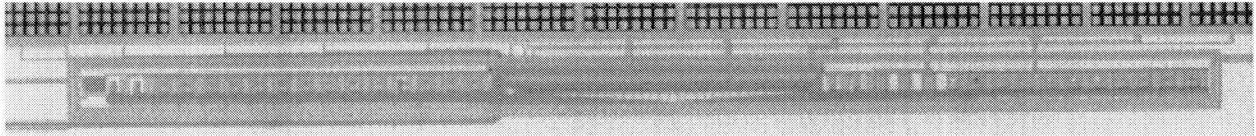

Figure 3. Photomicrograph of the test structures.

To avoid the high gate leakage current of the thin oxide transistors, we implemented the follower transistor, the photogate, and the transfer device using 3.3V thick oxide transistors. To achieve acceptable voltage swings, the reset transistors also use thick oxide transistors. The v_{reset} and v_{set} signals can be set to higher voltages to achieve larger signal swings. For example if we set $v_{reset} = v_{set} = 3.3$V, the signal swing of v_{in} can be increased to 1.5V from 0.6V when only thin oxide transistors are used. The standard supply voltage $v_{dd} = 1.8$V is used in all digital circuits including row address decoders.

3. MEASUREMENT RESULTS

In this section, we present measurement results from our APS test structure fabricated in a standard 0.18μm digital CMOS process.

To determine the dark current and QE we first estimated conversion gain by measuring the readout circuit gain and the sense node capacitance. The response of the readout circuit is shown in Figure 4. It was measured by setting the reset transistor gate to 3.3V and driving its drain with a triangular waveform. As the figure shows, for $1\text{V} \leq v_{set} \leq 2\text{V}$ the response is quite linear and the gain is ≈ 0.6.

We determined the sense node capacitance by measuring the voltage drop due to charge injection when the reset transistor is turned off and comparing this drop to that of a reference pixel with the photodiode replaced by a metal capacitor of known value.

The sources of charge injection, as depicted in Figure 5, are the feed-through due to the gate to source overlap capacitance and the diminishing channel of the reset transistor.

The sense node voltage drop due to charge injection is thus given by

$$\begin{aligned} v_{drop} &= v_{ch} + v_{fd} \\ &= \frac{\alpha Q_{ch}}{C_s} + \frac{v_{rst} C_{gs}}{C_s + C_{gs}} \end{aligned}$$

$$\approx \frac{\alpha Q_{ch} + C_{gs} v_{rst}}{C_s}$$
$$= \frac{Q_{eff}}{C_s}.$$

Here

v_{fd} is voltage drop due to overlap capacitance

v_{ch} is the voltage drop due to channel charge injection,

v_{rst} is the voltage drop at the gate,

C_s is the sense node capacitance,

C_{gs} is the gate source overlap capacitance,

Q_{ch} is the channel charge,

α is the percentage of the charge that injected to the sense node,

Q_{eff} is the total effective charge injected into the sense node, and

$C_s \gg C_{gs}$, which is the case in the design of the test structures.

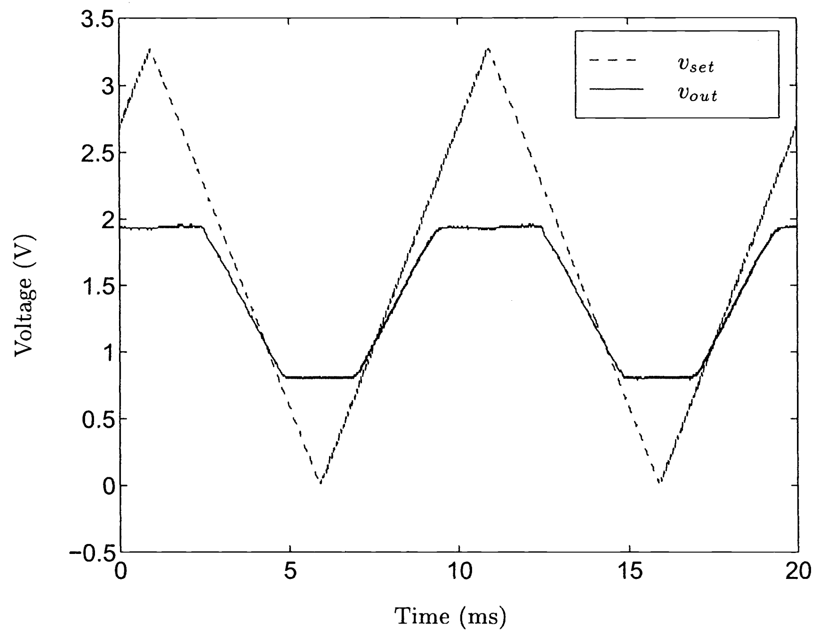

Figure 4. Measured readout circuit response.

It follows from our derivation that the voltage drop is inversely proportional to the sense node capacitance. We used this fact to compute C_s. To determine the total effective injected charge, we measured the voltage drop of the reference pixel. We then used this value and the measured voltage drop of each pixel to compute C_s. The results are reported in Table 1.

The measured quantum efficiency curves are plotted in Figure 6. The major reason for the low QE is the high recombination rate of the highly doped substrate. Also note that the photogate has uniformly lower

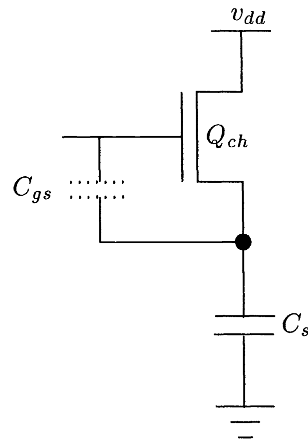

Figure 5. Charge injection when the reset transistor is turned off.

Symbol	Name	Capacitance
PD_3	3×3 μm^2 photodiode	8.64fF
PD_4	4×4 μm^2 photodiode	12.42fF
PG_S	3.85×3.25 μm^2 photogate sense node	12.26fF

Table 1. Measured capacitances

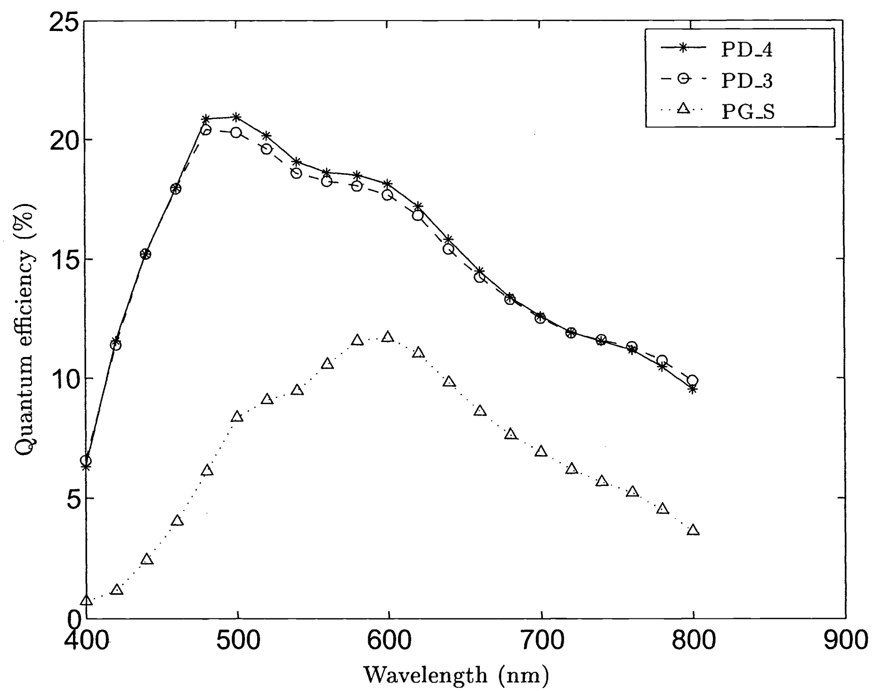

Figure 6. Measured quantum efficiency.

QE than the n+/psub photodiode due to the absorption in the poly gate, which does not scale as fast with technology as planar dimensions.

We also investigated the photon loss due to the oxide and passivation layers above the photodetector. To do so we dry etched holes through these layers and measured QE. We found the loss to be approximately 20% primarily due to reflection from the surface of the passivation layer.

To determine dark current we measured the output voltage under dark condition as a function of integration time as shown in Figure 7. Note the pronounced nonlinearity of these plots. By comparison, the output voltage under moderate illumination is quite linear in integration time as shown in Figure 8. The nonlinearity of the voltage under dark condition, therefore, should be attributed to the decrease in dark current density with decreasing reverse bias voltage. This is confirmed in Figure 9, where the dark current density is shown to increase super-linearly with reverse bias voltage. The rate of increase in dark current density, however, is too fast to be explained by the widening of the depletion region. It may, instead, be due to the Poole-Frenkel effect,[3,4] where the carrier emission rate from the traps is significantly increased by the electric field in the highly doped substrate of the 0.18μm technology. In Figure 10 we, again, observe the super-linear relationship between gate voltage and dark current density for the photogate APS.

As we have seen, dark current density decreases substantially with reverse bias voltage for photodiode and with gate voltage for photogate. It is, therefore, desirable to operate the photodetectors at low voltages. Figures 8 and 11 show that such decrease in bias voltages has little effect on QE.

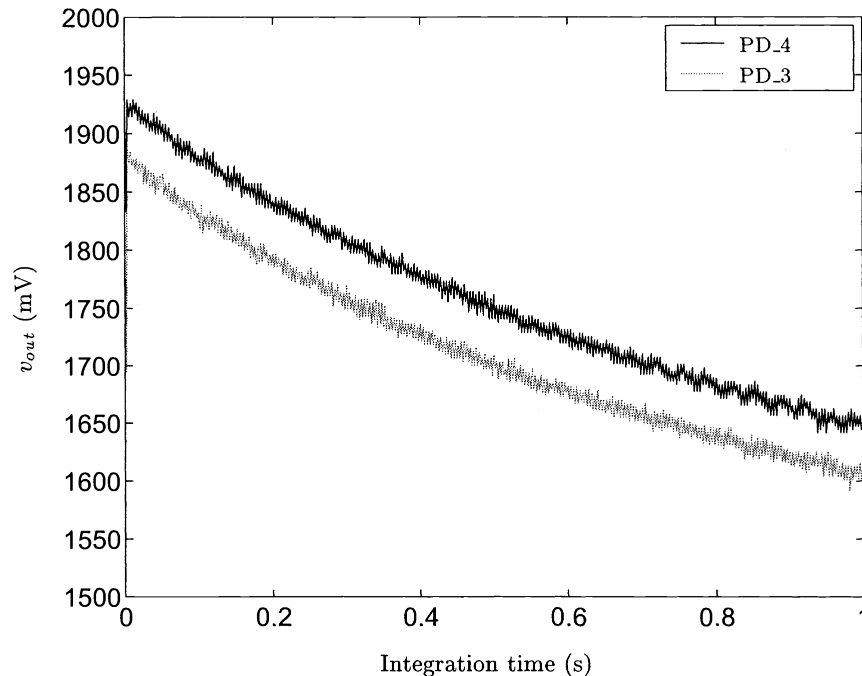

Figure 7. Measured v_{out} versus integration time under dark condition.

Finally, we found that the transfer transistor of the photogate circuit suffered from high off-current (in spite of using thick oxide transistor). We performed an experiment to find out the transfer gate voltage needed to turn it off. Figure 12 plots the normalized quantum efficiency of the photogate device for Tx voltage from 1V down to −0.6V. During the experiment, $v_{set} = 1.15$V and v_{pg} is pulsed between 0 and 2.1V. It is clear that the transfer gate cannot be turned off unless the gate voltage is negative.

Since Tx cannot be turned off using nonnegative gate voltage, we operated the photogate as a photodiode by setting both v_{pg} and Tx voltages to 0V. We found that QE in this mode is only a few percent lower than when operating in the normal photogate mode pulsing v_{pg} and Tx from 2.1V and −0.3V during integration to 0V and 1V during transfer, respectively.

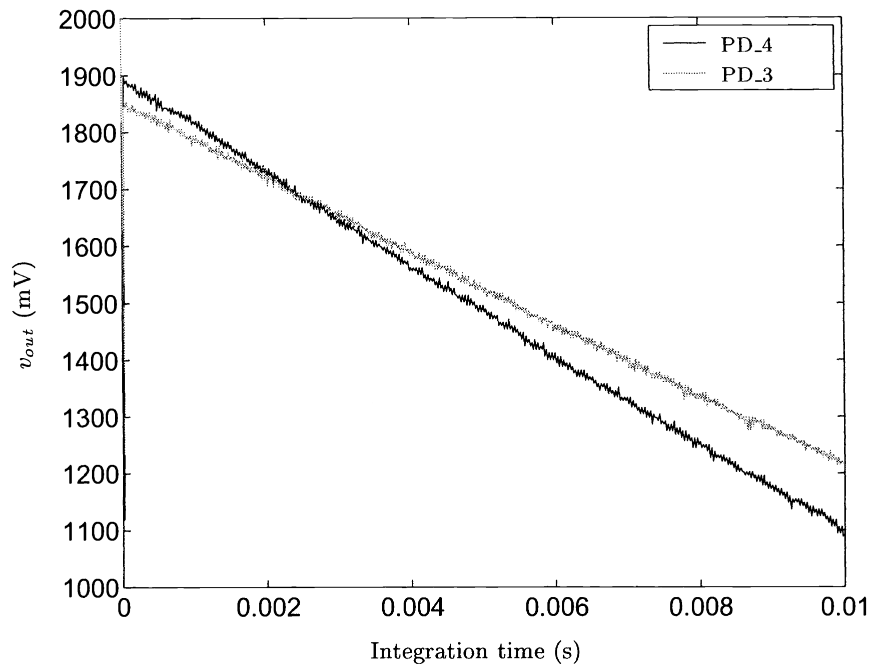

Figure 8. Measured v_{out} versus integration time under moderate illumination.

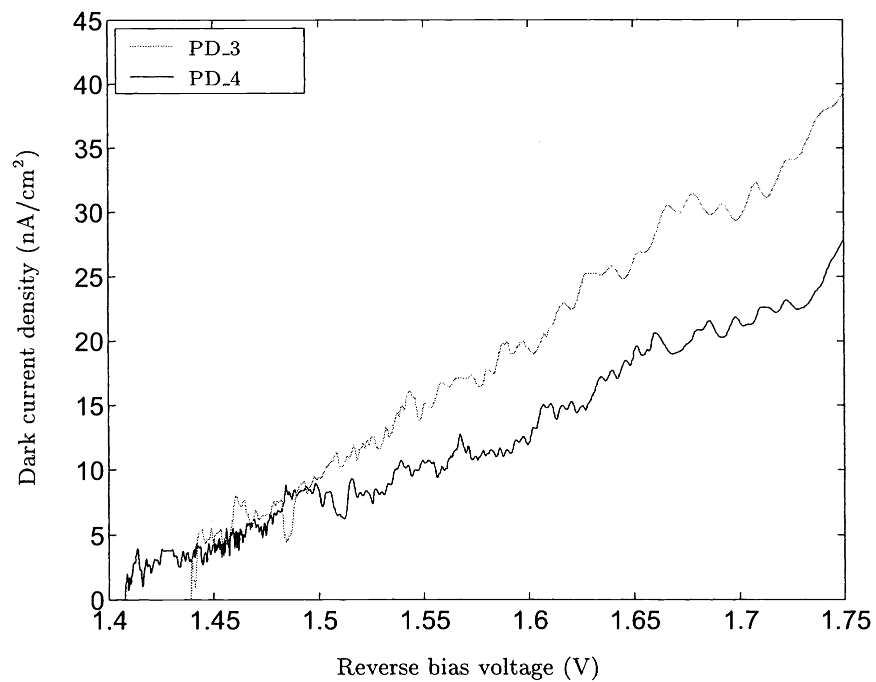

Figure 9. Measured photodiode leakage current as function of the reverse bias voltage.

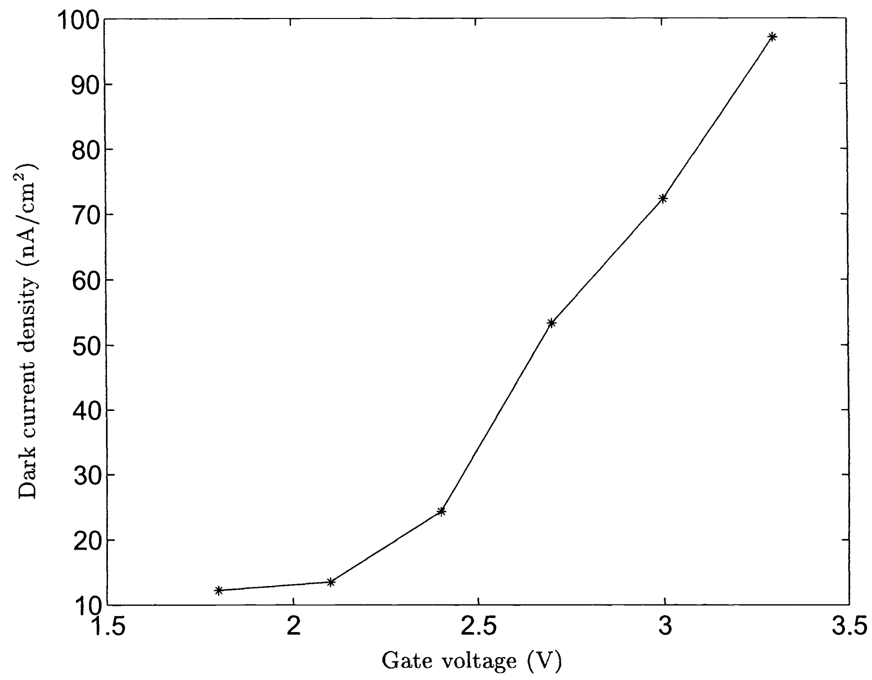

Figure 10. Measured photogate PG_S leakage current as a function of gate voltage.

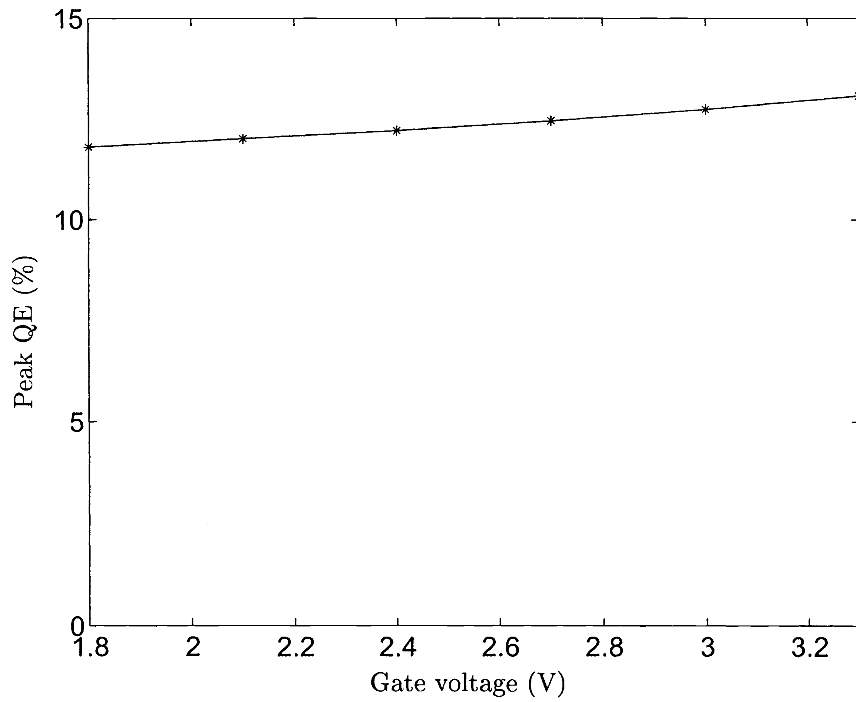

Figure 11. Measured peak QE of PG_S versus gate voltage.

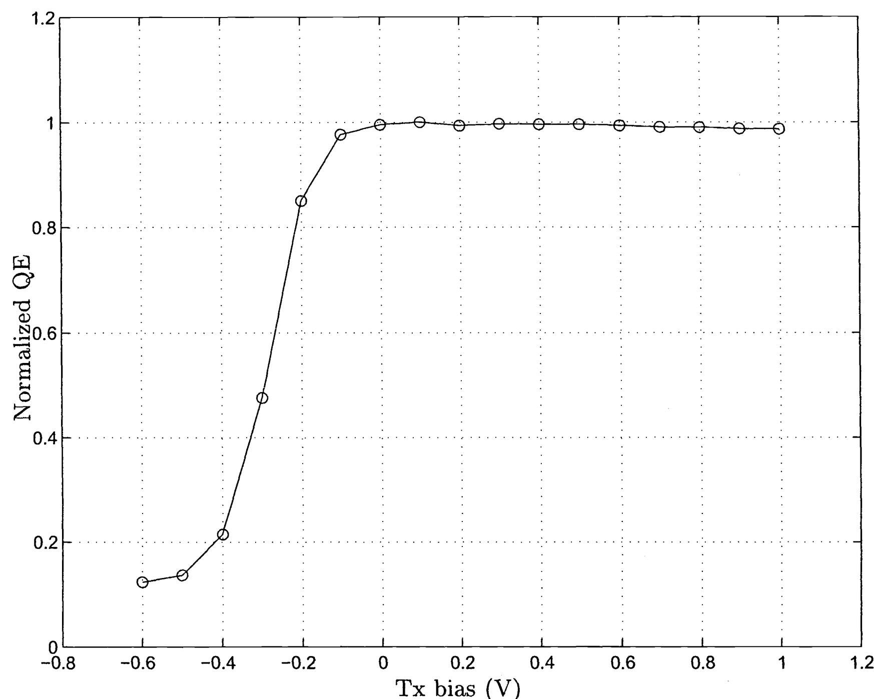

Figure 12. Measured quantum efficiency versus Tx bias voltage.

4. CONCLUSION

We described APS test structures fabricated in standard 0.18μm CMOS process. The test structures include pixels with different size n+/psub and nwell/psub photodiodes and nMOS photogates. To reduce leakage current and increase voltage swing, we used a mixture of thin and thick oxide transistors in the pixel designs. We reported measured dark current and QE results that confirm the poor imaging performance predicted by earlier studies. We found that dark current density decreases super-linearly with reverse bias voltage, which suggests that bias voltage should be scaled down with technology faster than supply voltage. We found that QE is quite low due to high pwell doping concentration. Finally we found that the photogate circuit cannot be operated in the standard way due to high transfer gate off-current. QE did not seem to be significantly reduced by this problem, however.

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