WA 17.5 A 640x512 CMOS Image Sensor with Ultra Wide Dynamic Range Floating-Point Pixel-Level ADC

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The dynamic range of an image sensor is often not wide enough to capture scenes with both high lights and dark shadows. In Reference 1, dynamic range is enhanced by increasing well capacity one or more times during exposure time. Another approach, which achieves consistently higher SNR is multiple sampling [2] A 640x512 image sensor with Nyquist rate pixel level ADC implemented in a 0.35μm CMOS technology shows how a pixel level ADC enables flexible efficient implementation of multiple sampling. Since pixel values are available to the ADCs at all times, the number and timing of the samples as well as the number of bits obtained from each sample can be freely selected without the long readout time of APS. Typically, hundreds of nanoseconds of settling time per row are required for APS readout. In contrast, using pixel level ADC, digital data is read out at fast SRAM speeds. This demonstrates another fundamental advantage of pixel level ADC - the ability to programmably widen dynamic range with no loss in SNR.

The 640x512 sensor employs the MCBS ADC technique described in Reference 3. Each 2x2 block of pixels share a 1b comparator/latch pair. The signals required to operate the ADCs are globally generated by off chip DAC and digital control circuitry. The ADC is bit serial and each bit is generated by peforming a set of comparisons between the pixel values and a RAMP signal. The bits are generated independently and in any order, and the data is read out as bit planes [3].

Consider the implementation of multiple sampling for exponentially increasing exposure times T, $2T$, $4T$, ... 2^kT. Each sample is digitized into m bits. The digitized samples for each pixel are combined into an $m+k$ bit binary number with floating point resolution. The number can be converted to floating point with exponent ranging from 0 to k and an m bit mantissa, in the usual way. This increases sensor dynamic range by a factor of 2^k, while providing m bits resolution for each exponent range of illumination. An important advantage of this scheme, over other dynamic-range enhancement schemes, is that the combined digital output is linear in illumination [1]. This not only provides more information about the scene, but also performs color processing in the standard way.

To illustrate implementation of this scheme, consider an example with k=2 and m=2. Figure 17.5.1 plots output pixel voltage versus time for constant illuminations I_1, I_2, and I_3, assuming linear photon-to-voltage response, and saturation voltage V_{max}. The voltage is sampled after exposure times T, $2T$, and $4T$. Each sample is digitized into 2 bits using binary code as shown in the figure. The first sample is digitized into x_1x_2, e.g. 11 for I_1. The second is also digitized to 2b. Since the second sample is twice the value of the first, the 2b are x_2x_3 if the sample is not saturated, i.e. $< Vmax$, and 11 if it is. In either case, the ADC needs to generate only the least significant bit x_3. Similarly, for the third sample at 4T only the least significant bit x_4 needs to be generated. Table 17.5.1 lists the bit values for each illumination and the corresponding binary floating-point representation. This is easily extended to any exponent k and mantissa m. The first sample is digitized to m bits, then only the least significant bit is generated from each consecutive sample. Thus as long as the sensor photon-to-voltage response is linear only $m+k$ bits need be read out, which is the minimum required. This further reduces readout time. Often, more bits need to be read out from the samples to correct for sensor nonlinearity, offset, and noise.

A schematic of four pixels sharing a 1b comparator/latch pair, and the column sense amplifier is shown in Figure 17.5.2(a). The comparator/latch circuit is described in Reference 3. An anti-blooming transistor is connected to each photodetector to avoid blooming during multiple sampling. The sense amp is high-speed, low-noise and low-power. A charge amplifier minimizes bitline voltage swing. To sense the bitline, capacitor Mc is first reset, and current from the pixel and transistor M7 is integrated. The sensed bit is latched using a flip flop. The tristate inverter is part of a 10:1 mux.

A scene is imaged one quarter frame at a time as illustrated in Figure 17.5.2 b. Before capturing a quarter frame the sensor is reset. Sample and hold ensures that the signal does not change during ADC. Each quarter sample image is read out one bit plane at a time [3]. The quarter images are then combined to form a quarter frame, and the quarter frames merged into a high-dynamic-range frame.

Figure 17.5.6 is a micrograph of the sensor. Table 17.5.2 summarizes the main sensor chip characteristics. Figure 17.5.3 plots the pixel output voltage vs. time under constant illumination. Note that it is quite linear. A scene with measured dynamic range $\geq 10^4$ is illustrated in Figures 17.5.4 and 17.5.5. The scene is sampled 9 times, at T=3.3 ms, 2T, ..., and 256T, and a 16b image is reconstructed. Since we cannot print gray scale images of more than 8 bits, in Figure 17.5.4 we display four 8b slices of the image. The first is a plot of the 8 most significant bits of the 16b image, where only the roof and the front of the dollhouse is seen. The 2nd is obtained by brightening the image by 8x. Several objects inside the house are revealed. These objects become more visible in the 3rd image, after the original image is brightened by 32x. The 4th image is obtained by brightening the image by 256x. A table and a man hiding in the dark area next to the house appear. Figure 17.5.5 is an 8b plot of the log of the 16b image.

Acknowledgments:
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References:
[1] S. Decker et al., "A 256x256 CMOS Imaging Array with Wide Dynamic Range Pixels and Column-parallel Digital Output," ISSCC Digest of Technical Papers, Feb. 1998, pp. 176–177.
[2] D. Yang et al., "Comparative Analysis of SNR for Image Sensors with Enhanced Dynamic Range," SPIE, vol. 3650, 1999.
[3] D. Yang et al., "A Nyquist Rate Pixel Level ADC for CMOS Image Sensors," Proc. IEEE CICC, May 1998, pp. 237-240.

Technology	0.35 μm, 4-layer metal, 1-layer poly, nwell CMOS
Sensor size	640 × 512 pixels
Pixel size	10.5 μm × 10.5 μm
Photodetector	n-well to p-sub diode
Sensor area	6720 μm × 5376 μm
Fill Factor	29%
Transistors per pixel	5.5 (22 per four pixels)
Package	180 pin PGA
Supply Voltage	3.3V
Signal swing	0.5–2.5V
Sensitivity	4.1 $\mu V/e^-$
Maximum frame rate	250 frames/s (@ 8-bit resolution)
Fixed pattern noise	< 0.2% (dark) at 25°C
Dark current	1.3 mV/sec (160 pA/cm^2) at 25°C
Digital dynamic range:	65536:1 measured

Table 17.5.2: Characteristics of 640x512 Area Image Sensor.

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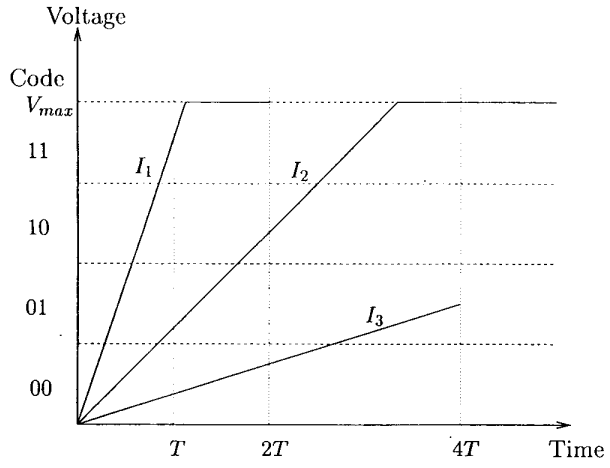

Figure 17.5.1: Pixel output voltage and its digitized value vs time.

Illumination	$x_1x_2x_3x_4$	Exponent	Mantissa
I_1	1 1 1 1	2	11
I_2	0 1 0 1	1	10
I_3	0 0 0 1	0	01

Table 17.5.1: Digitized values for 3 illumination levels.

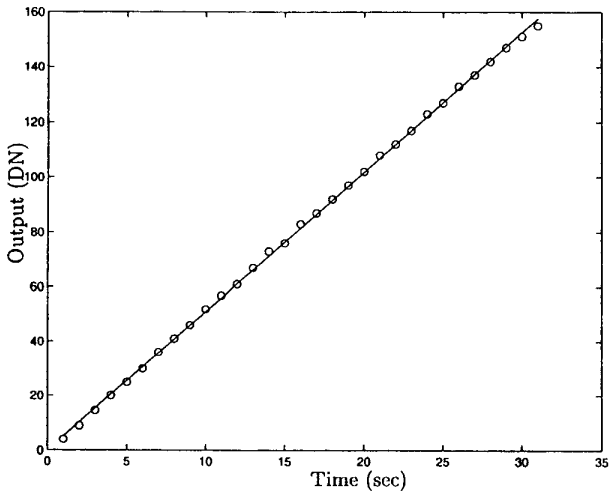

Figure 17.5.3: ADC output vs. time at constant illumination.

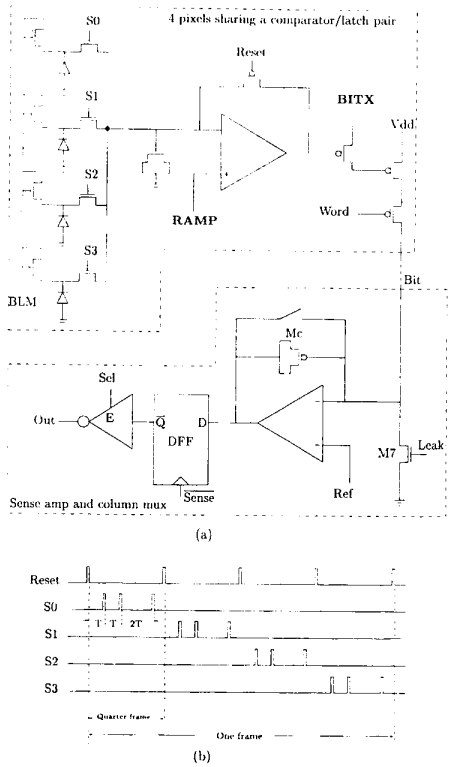

Figure 17.5.2: (a) Pixel block and column sense amplifier. (b) Timing diagram for multiplexed multiple sampling.

Figure 17.5.4: **See page 472.**

Figure 17.5.5: **See page 472.**

Figure 17.5.6: **See page 471.**

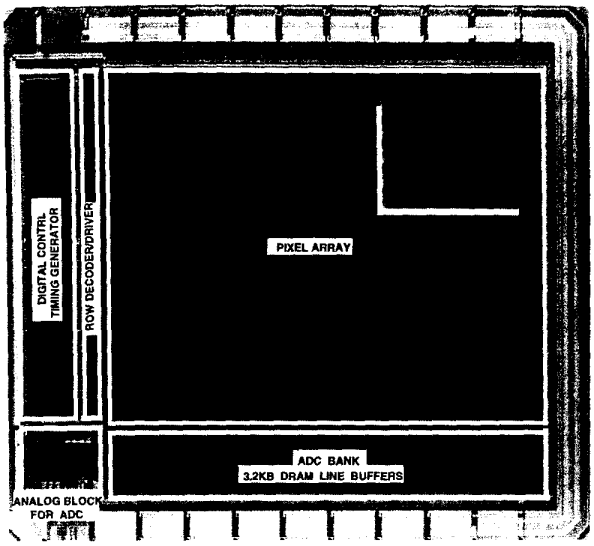

Figure 17.3.1: Micrograph of the 7.6x6.8μm² CMOS imaging system with 800x600 pixel array, integrated digital control, 8b ADC bank and 3.2kB line buffer.

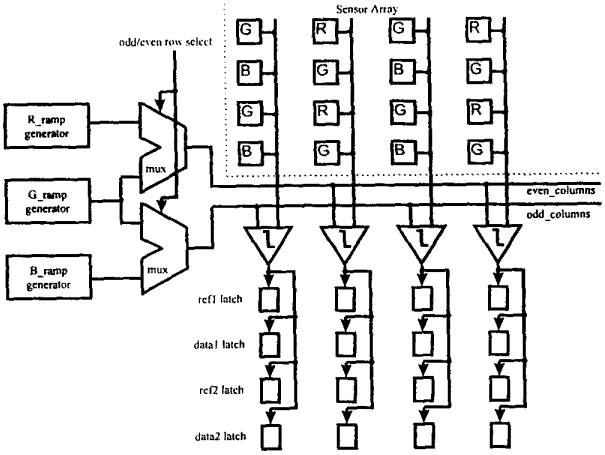

Figure 17.3.6: Three analog ramp generators with programmable step sizes multiplexed into odd and even subbanks of comparators for individual ADC gain control for red, green and blue pixels arranged in Bayer pattern.

Figure 17.3.7: Typical raw image data from digital 800x600 CMOS imager.

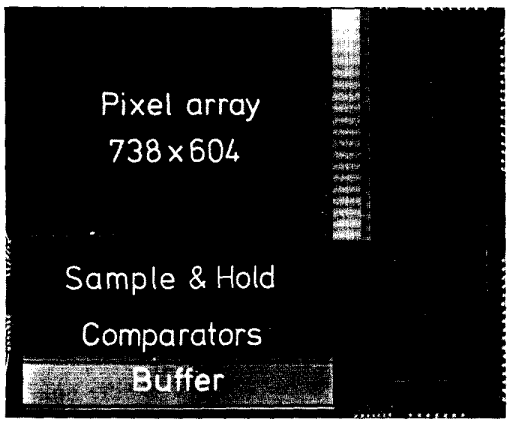

Figure 17.4.5: Die micrograph.

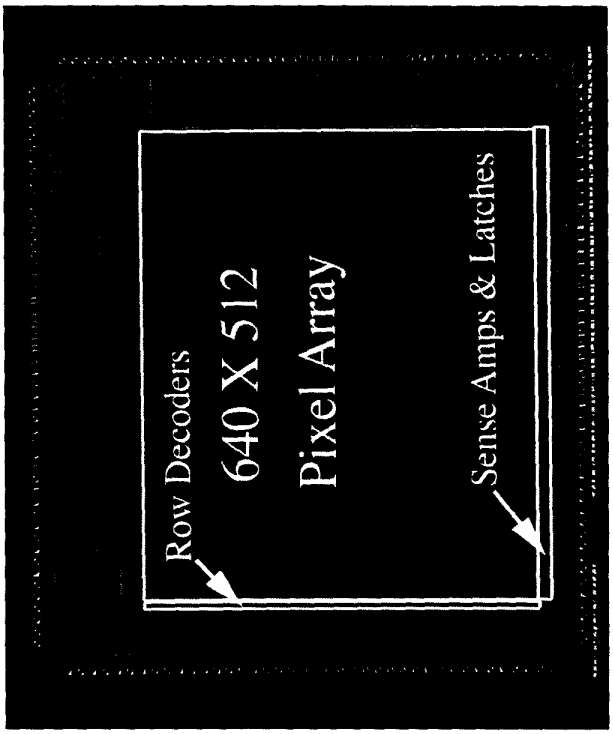

Figure 17.5.6: 640x512 image sensor micrograph.

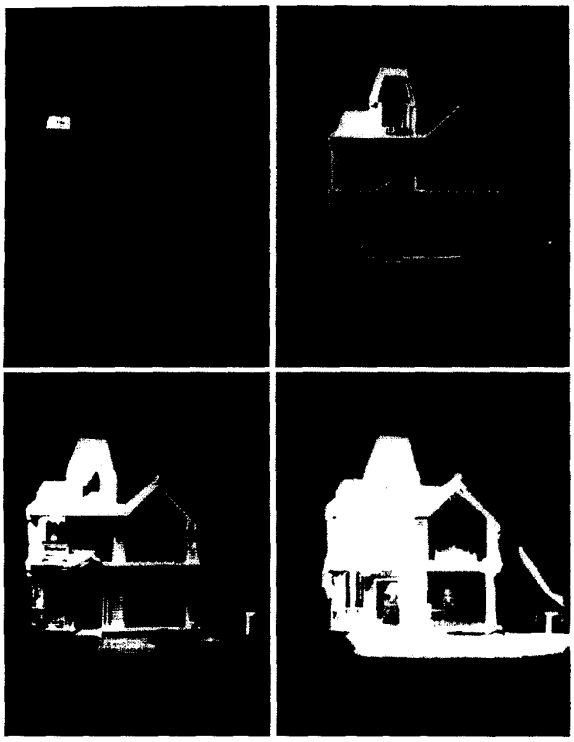

Figure 17.5.4: Four slices of 16-bit image.
(Upper left) Most significant 8b.
(Upper right) Image brightened 8x.
(Lower left) Image brightened 32x.
(Lower right) Image brightened 256x.

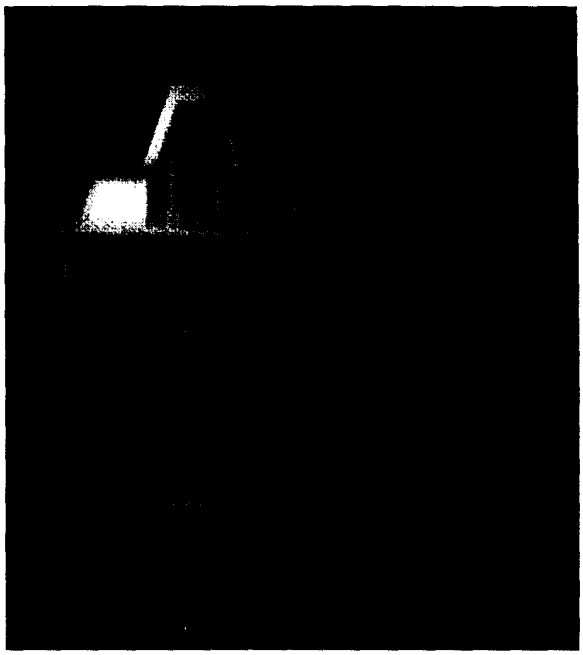

Figure 17.5.5: Log of 16b image.

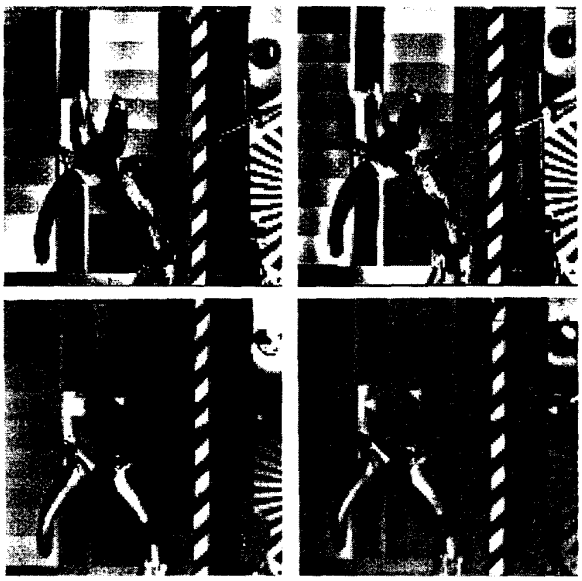

Figure 17.6.6: Upper scene: 16x16 kernel.
Lower scene: 32x32 kernel.

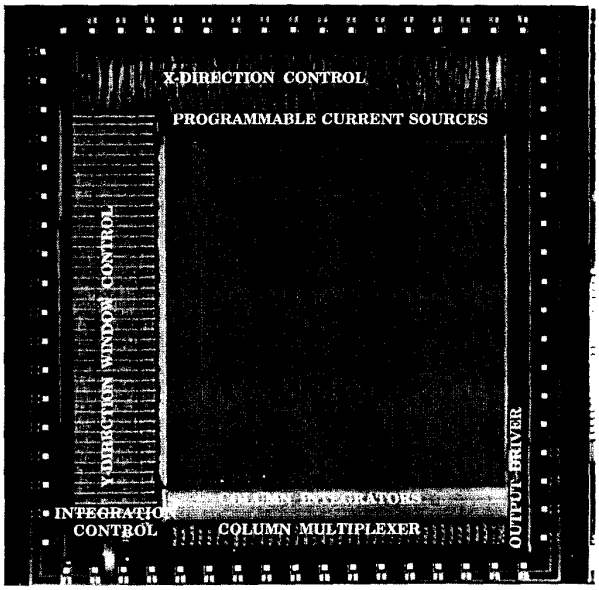

Figure 17.6.7: Chip micrograph.

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