Test Structures for Characterization and Comparative Analysis of CMOS Image Sensors

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1. ABSTRACT

A set of test structures designed to characterize and compare the performance of CMOS passive and active pixel image sensors is presented. The test structures are designed so that they can be rapidly ported from one process to another. They are also designed so that individual photodetectors and pixel circuits as well as entire image sensor arrays can be characterized and compared based on: quantum efficiency, spectral response, fixed pattern noise, sensitivity, blooming, input referred read noise, reduction of quantum efficiency caused by silicide/salicide, lag, digital switching noise sensitivity, impact ionization noise sensitivity, dynamic range, and temperature dependency of all measured parameters. Four test chips that include a variety of these structures have been built in two different 0.35μm CMOS processes. The test chips include nineteen types of individual photodetectors and thirty eight types of 64×64 pixel arrays. The test methodology and preliminary test results from these chips will be presented.

keywords: CMOS imaging, APS, quantum efficiency, dark current, spectral response

2. INTRODUCTION

CMOS image sensors are being actively researched as an alternative to CCDs for digital imaging applications. The main advantage of using CMOS is the ability to integrate most or all of a digital imaging system on a single chip, thus reducing cost and power dissipation. Remarkable results have been published showing that certain CMOS sensors compare favorably to CCDs in dynamic range, and fixed pattern noise.[7,1] In spite of these reported results we believe that the know-how required to build such integrated CMOS sensors especially in advanced (0.35μm and below) processes is still lacking. Issues such as image sensor noise , quantum efficiency and dark current are not well understood for advanced CMOS processes. Most published work is concerned with the implementation of a specific sensor architecture in a specific process. For example Denyer[8] reports on passive pixel sensor built in a 1.5μm process, Forchheimer[2] reports on passive pixel sensor built in a 1.6μm process, Fossum[4] reports on an active pixel sensor built in a 2.0μm process, Dickinson[1] reports on an active pixel sensor built in a 0.9μm process, and Fowler[3] and Yang[11] report on sensors with pixel level A/D conversion built in 1.2μm and 0.8μm processes respectively. As a result it is difficult to objectively compare the characteristics of different sensor designs. Additionally, the reported results do not provide designers the predictive knowledge necessary to select the best image sensor architecture for the given process or to optimize the design of the selected architecture.

In this paper we describe a set of test structures that can be used to characterize a CMOS process for image sensor applications. The goal of designing the test structures is to be able to characterize and compare the performance of different photodetectors, pixel circuits, and sensor architectures built in the same process and across different processes. The results obtained from the characterization of these test structures should provide image sensor designers the predictive knowledge needed to design new image sensors. To achieve this goal we

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designed the test structures to be modular and process portable so that it is easy to include all or a subset of the structures in a test chip and it is easy to add new photodetectors or change array sizes without major redesign. We designed the test structures to be comprehensive so that they can be used to compare most known photodetectors and passive as well as active sensor architectures. The test structures include many flavors of photodetectors such as native photodiodes, photodiodes in a well, well photodiodes (reverse biased well-substrate junction), native photogates, well photogates, and phototransistors. They also include many arrays of passive and active pixel architectures employing these different flavors of photodetectors. The test structures can be used to measure image sensor parameters such as quantum efficiency, spectral response, sensitivity, dark current, fixed pattern noise, blooming, lag, dynamic range, and input referred read noise. They can also be used to measure the effects of various noise sources including impact ionization, capacitively coupled substrate noise, and charge injection noise. Much thought has been given to how each structure may be characterized while keeping the need for expensive specialized test equipment to a minimum.

The remainder of this paper is organized as follows. In section 3. we discuss the image sensor parameters that we plan to extract from the test structures. In section 4. we describe each type of test structure used, what parameters it is used to measure and how we plan to test it. Four test chips that include a variety of these test structures have been designed in two 0.35μm CMOS processes. The test chips have been taped out and should be available in time to present preliminary results at the conference.

3. IMAGE SENSOR PARAMETERS

Before describing our test structures, we discuss the image sensor parameters we wish to measure. For the purpose of organizing the discussion we group these parameters into two sets. The first set measures the characteristics of single pixel circuits and include, quantum efficiency, spectral response, sensitivity, dark current, dynamic range, and the effect of silicide and salicide on quantum efficiency. The second measures the parameters particular to an array of pixels and include fixed pattern noise, blooming, lag, and input referred read noise. In addition we designed the test structures so that we can better understand the noise sources resulting from integrating analog and digital circuitry with an image sensor, especially at the pixel level.[3] These noise sources include: impact ionization noise,[9] capacitively coupled switching noise,[10] and charge injection noise.[10] Although each of these noise sources is caused by different effects they all generate excess electron/holes in the substrate/well which, if diffused to a photodetector, would cause noise in the output signal.

For completeness we briefly define each of these parameters.

Quantum Efficiency is the ratio of the number of collected electron/hole pairs to the number of incident photons at a given light wavelength. The quoted quantum efficiency is typically the maximum achieved over the visible spectrum.

Spectral Response is quantum efficiency as a function of the wavelength measured within the desired wavelength range. For example, the spectral response of a silicon photodetector is usually measured for wavelengths between 0.3μm and 1.1μm.

Sensitivity is the gain of the read circuitry measured in volts per electrons. It is measured by irradiating the photodetector with a thermal radiation source at 2856 Kelvin.

Dark Current is the current generated by the detector in the absence of any incident radiation. It is measured in nA/cm^2. Note that dark current in a silicon photodetector is a strong function of temperature,[5] and therefore the photodetector junction or gate temperature at which dark current is quoted must be specified.

Dynamic Range is the ratio of the maximum non-saturating signal to the dark signal measured over the desired image capture time period. For example, if a photodetector is reset to 1v and requires 500,000 electrons

to discharge it to 0v, then its maximum non-saturating signal is 500,000 electrons. If its dark signal is 10 electrons at 77 Kelvin then the dynamic range is 94dB.

Silicide/Salicide Effect is the reduction in quantum efficiency due to the use of silicide/salicide. Silicide and salicide are metal silicon molecules that are grown on the gate and source/drain regions of a MOS transistor respectively. They are used to lower sheet resistance, and in turn increase digital switching speed. Unfortunately, silicide and salicide are opaque to visible light and as a result greatly reduce quantum efficiency.

Fixed pattern noise is the variation in pixel currents at uniform illumination, measured at the output of the sensor array. For example at no illumination, fixed pattern noise measures the variation in dark current.

Blooming is the number of electron/holes dumped into the substrate/well and collected by adjacent photodetectors when a photodetector saturates.

Lag is the fraction of charge left over after the pixel is reset. For example, a photodetector that collects 10000 electrons during a frame but still contains 1000 electrons after reset has a lag of 10%. Note that lag is a function of illumination.

Input referred read noise is the photodetector input referred noise measured at no illumination. The result is measured in electrons.

4. TEST STRUCTURES

To measure the parameters discussed in the previous section we use two basic structures: single pixel test structures and 64×64 pixel arrays. The single pixel test structures are used to measure quantum efficiency, spectral response, dynamic range, sensitivity and dark current. Each single pixel consists of one photodetector followed by several stages of amplification. The 64×64 pixel arrays are used to measure fixed pattern noise, blooming, input referred read noise, and lag. All of the structures can be used to measure the effects of digital switching noise (capacitively coupled and charge injection), impact ionization noise and the quantum efficiency reduction caused by silicide/salicide. In the next two subsections we describe each structure, what parameters it is used to measure, and how we intend to perform the measurements.

4.1. Single Pixel Test Structures

A single pixel test structure consists of a photodetector, a calibration circuit, noise generation circuitry and several stages of amplification. The calibration circuit is used to determine the relationship of the output voltage to the input charge. The single pixel test structures include many flavors of photodetectors such as: native photodiodes, photodiodes in a well, well-photodiodes (reverse biased well-substrate junction), native photogates, photogates in a well, and phototransistors, as shown in Figure 1. Most CMOS processes below 0.8μm use silicide/salicides over their gate and source/drain regions. Since silicides are opaque, quantum efficiency is greatly reduced. This problem is eliminated if a silicide blocking mask is available. If not, the effect can be reduced by cutting holes through the photodetector area. The test structures include both passive and active pixels, the main difference being the design of the first stage of amplification. The passive pixel has a charge integrator whereas the active pixel has a source follower buffer. We designed a total of nineteen single pixel test structures.

The circuit schematic for a passive single pixel test structure is shown in Figure 2. It consists of calibration circuits which are not shown and a charge integrating amplifier followed by a voltage amplifier and a follower buffer. It also includes noise generating circuits near the photodetectors that are not shown. Offset compensation and correlated double sampling are performed by autozeroing. The timing of the readout sequence is shown in Figure 3. First S0 and S01 are turned on. This resets the photodiode and stores the opamp offset values on

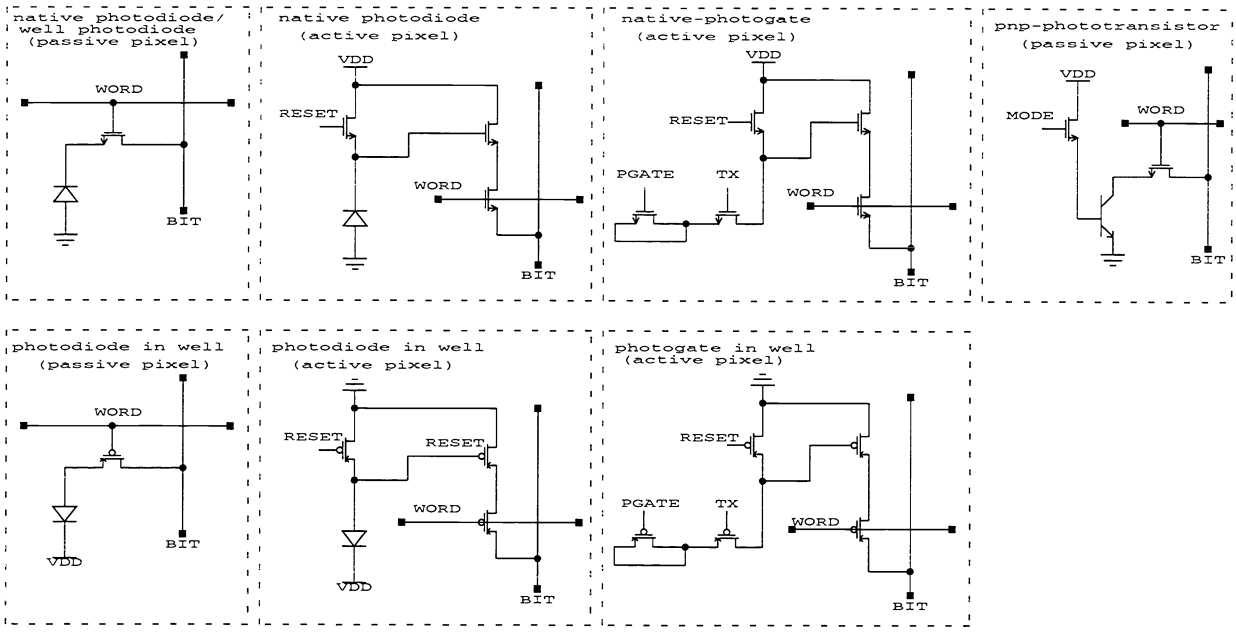

Figure 1: Pixel Circuits

capacitors C1, C2, C4 and C5. S01 is then turned off so that the switch charge injection offset of the integrating amplifier is stored on C3. Thus the opamp offset voltages and the switch charge injection are all cancelled. S0 is then turned off and S1 is turned on. The amplification circuitry can now be operated either in a sampled mode which is similar to the readout operation of an image sensor, or in continuous tracking mode. To operate the circuit in continuous tracking mode the shutter is closed. The amplifier integrates the charge collected by the photodetector. To operate in the sampled mode the shutter is left open and the photodetector collects charge. The shutter is then closed and the total amount of charge collected is transferred to C1 or C1 + C2 depending on the state of the two switches controlled by the signal mc. If mc is high, i.e. the switches are closed, then C1 and C2 in parallel constitute the integrating capacitor of the amplifier. This is the setting for normal to strong light intensities. If mc is low only C1 is selected. This increases amplification for dark current measurements. Continuous tracking mode has less kT/C noise and is therefore preferred for low noise measurement even though it is not used in normal image sensing operation.

The calibration circuit is used to calibrate the charge to voltage transfer function of the amplifier. It comprises a current source with a very wide dynamic range. Calibration time is controlled by the signal CAL.

To minimize noise and maximize voltage swing, we choose a two stage configuration for the opamp. The opamps are biased in the subthreshold region to maximize their gain. The final follower buffer stage is biased above threshold in order to drive a chip output pad. If a process does not support linear capacitors, MOS capacitors biased by at least one threshold drop are used. Note that the only linear capacitors needed are C1, C2, C3, and C4. Here C1 or C1 + C2 is the integration capacitor, and C3 and C4 are used for voltage amplification. All other capacitors such as the pole splitting Miller compensation capacitors and the offset-compensation capacitor used in the final follower stage can be well-MOS capacitors at any bias. The capacitors must be large enough to ensure stability and achieve low kT/C noise.

The schematic for an active single pixel test structure is shown in Figure 4. The first amplification stage is

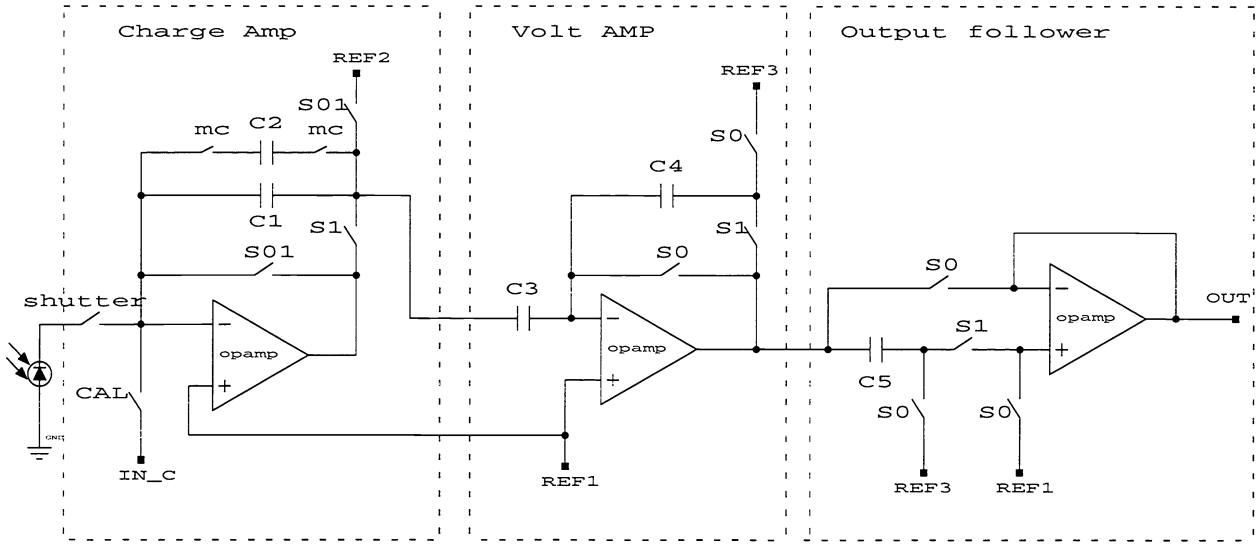

Figure 2: Passive Single Pixel Test Structure Circuit

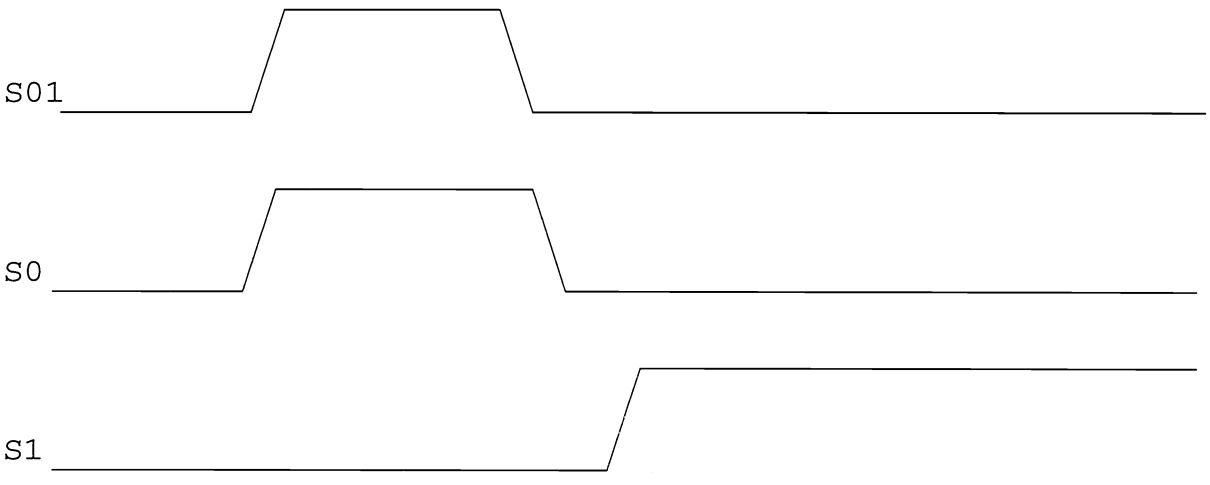

Figure 3: Timing Diagram for setup and readout

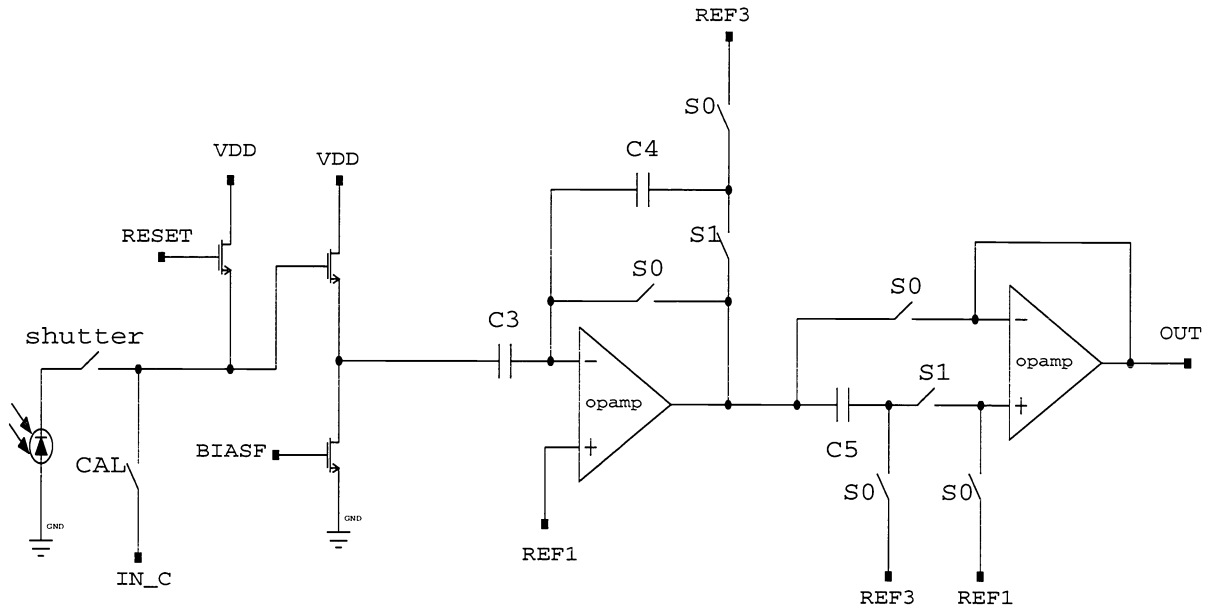

Figure 4: Active Single Pixel Test Structure Circuit

identical to an APS pixel where a source follower buffer is used. The second and third amplification stages are identical to those used in the passive pixel test structure described earlier.

We now briefly discuss how the photodetector parameters listed in the previous section will be extracted from the single pixel test structures. The quantum efficiency of a single pixel is measured as follows: First, we calibrate the single pixel, i.e, we establish a relationship between its input charge and output voltage. When calibration is completed, we measure the quantum efficiency of the photodetector by illuminating it with a uniform monochromatic source of known intensity. The output voltage of the amplifier is then used to determine the number of collected photons. The uniform monochromatic source is generated using a thermal source of uniform illumination, a monochromator and an integrating sphere. The intensity of the source is determined using a calibrated photodiode. To measure the spectral response of a photodetector, the same measurement is performed using a set of different monochromatic radiances that span the visible spectrum. Sensitivity is similarly measured except that the thermal source is not filtered through a monochromator. Dark current is measured by first covering the chip with a standard ceramic lid and then measuring the output voltage of the single pixel circuit. Dynamic range can be simply calculated as the ratio of the maximum output current of the photodetector to the dark current. The effect of silicide/salicide is calculated by measuring the spectral responses of one single pixel without field oxide cut holes and one with field oxide cut holes, see Figure 5.

To measure digital switching an inverter near the photodetector is selected and switched at a constant frequency. The output of the single pixel indicates how much noise is collected by the photodetector. By selecting inverters placed at different distances from the photodetectors we hope to better understand the substrate noise effects.

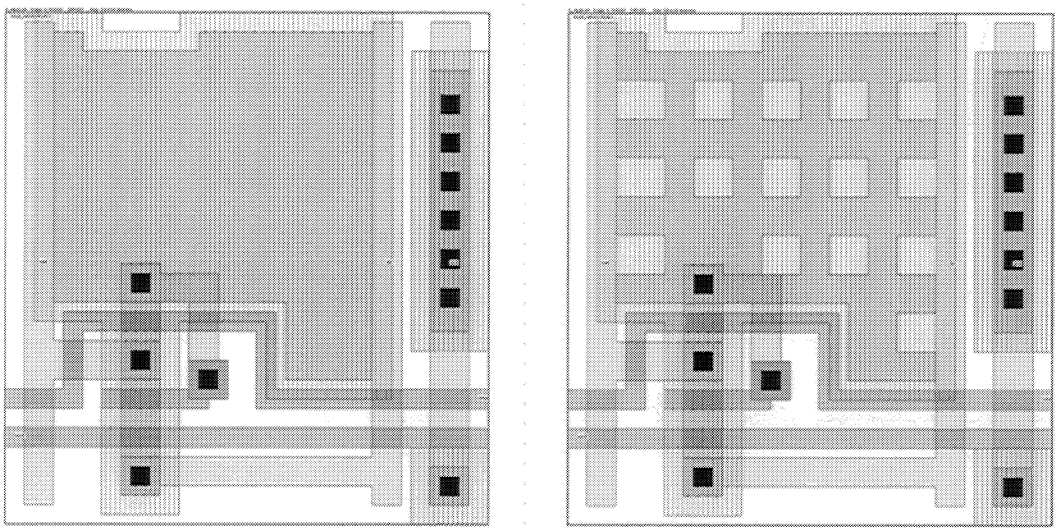

Figure 5: Left - Active n-type photodiode pixel, Right - Active n-type photodiode pixel with field oxide cuts

4.2. 64×64 Pixel Arrays

Each 64×64 pixel array test structure consists of a sensor array, a row decoder, column amplifiers, and a column decoder. As is the case for the single pixel test structures many flavors of photodetector can be used in designing the arrays. Additionally, many variations of passive and active pixel designs can be used resulting in a very large number of possible array test structures. For example all the array designs used by Denyer,[8] Forchheimer[2] and Fossum[4] can be generated. By placing a set of these different types of arrays on the same chip, we can quantitatively compare their performance in any given CMOS process. Also, all of the 64×64 pixel arrays can be tested at the same time, forming a 'giant' array of image sensors. The performance of the sensors may be qualitatively compared by simply looking at the 'giant' image.

We now discuss the circuit implementation of a 64×64 array test structure. Figure 6 shows the architecture of a 64×64 array. The array is read one row at a time using the row decoder. The signals from each row are then amplified using the column amplifiers and serially shifted off the chip through S_OUT and R_OUT. To control switching noise, the slew rate of the row decoder outputs can be adjusted. All timing and control signals needed for the operation of the array are generated off chip. Two types of pixel designs can be used in an array: passive pixel design[8] and active pixel design.[4] The active pixel design is almost identical to the APS[4,6] design with column level fixed pattern noise suppression circuits, and is shown in Figure 7 for completeness. Correlated double sampling is achieved by storing reset and signal on two output branches. Capacitors CS, CR, CCS and CCR are made large enough for tolerable kT/C noise. Since we are targeting standard CMOS processes with no available linear capacitors, MOS capacitors are used. The nonlinearity of the MOS capacitors is not an issue since they are only used to hold voltages.

In the passive pixel design each pixel contains a photodetector and an access transistor for readout as shown in Figure 8. The column amplifier employs a charge integrator implemented using a two stage opamp circuit and is otherwise similar to the column amplifier used in the active pixel design.

We now briefly describe how we plan to measure the array parameters listed in the previous section. Fixed pattern noise is determined by computing the mean and standard deviation of the measured dark currents, or pixel currents at any other desired uniform illumination. Blooming is measured by using either a metal shield

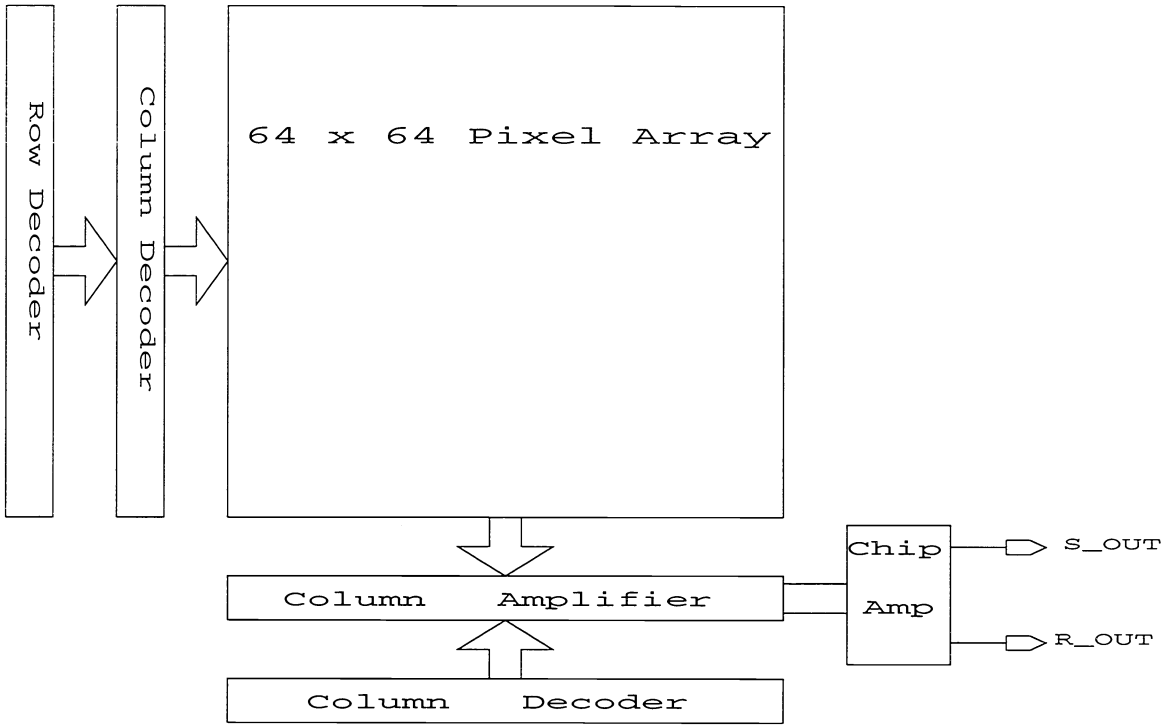

Figure 6: Pixel Array Block Diagram

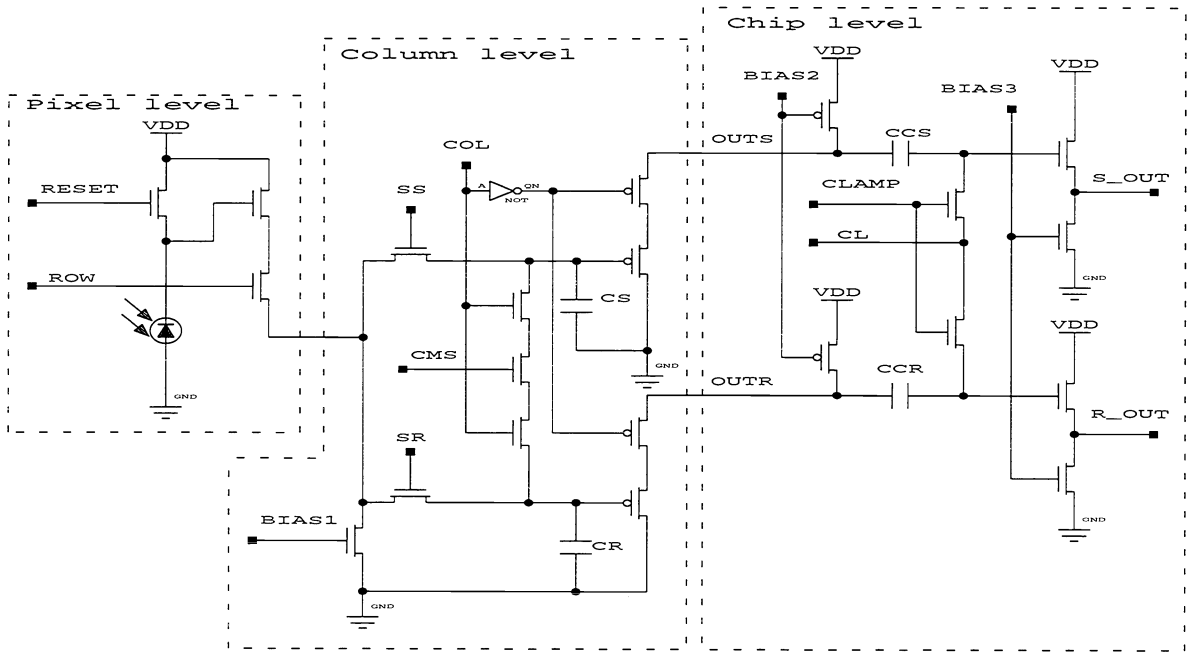

Figure 7: Pixel and readout circuitry of an Active Pixel Array

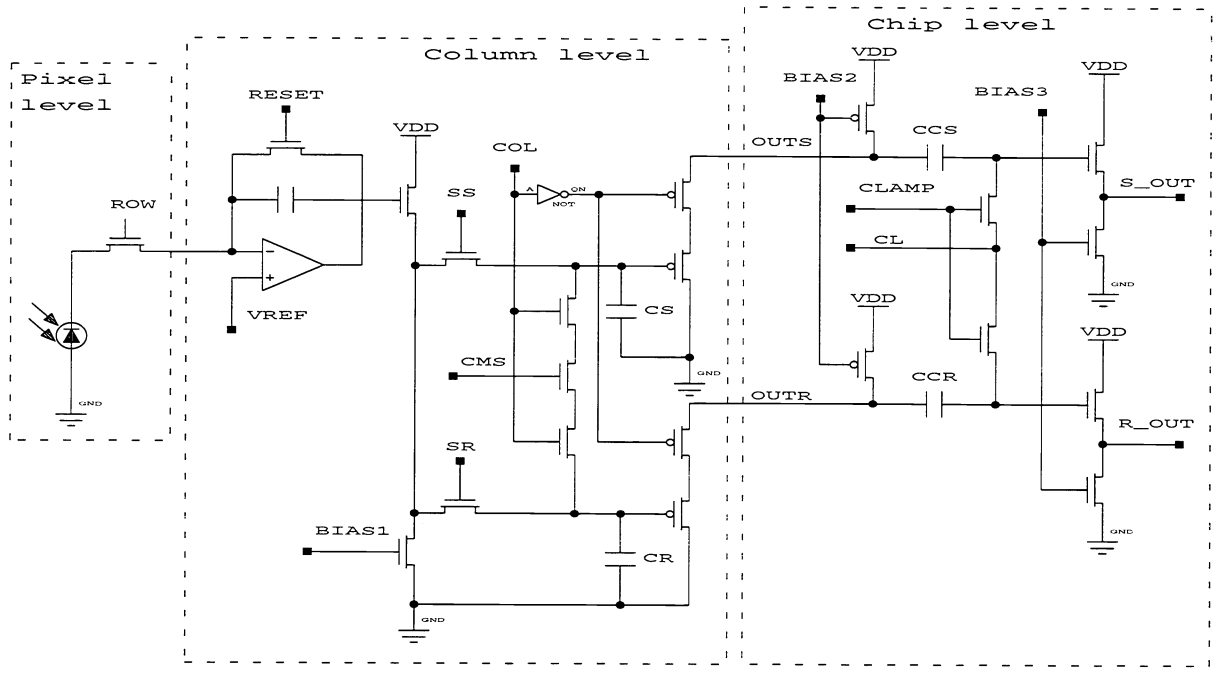

Figure 8: Pixel and readout circuitry of a Passive Pixel Array

over the entire array with a 4×4 pixel block cut out at the center, or by using a He-Ne laser. When the sensor is illuminated by a high intensity source the unshielded pixels saturate and dump charge into the substrate and their surrounding pixels. The outputs of the surrounding pixels are then measured in order to determine blooming.

Input referred read noise is found by computing the standard deviation of the output voltage at no illumination and back calculating the number of electrons at the photodetector necessary to produce the measured output.

Lag is measured by comparing consecutive frames. The array is uniformly illuminated using a thermal source. A shutter is opened and the first frame is captured. The shutter is then closed and subsequent frames are captured.

In addition to measuring the array specific parameters the 64×64 arrays may also be used to measure quantum efficiency and sensitivity. The values of these parameters may be different from those obtained from the single pixel test structures but are of greater practical significance.

5. TEST CHIPS

Four test chips have been designed and taped out in two different 0.35μm CMOS processes. The test chips contain a total of nineteen different single pixel structures and thirty eight 64×64 pixel arrays. The test chips are expected to be back from fabrication in time to present preliminary results at the conference.

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