TA 6.7: Regenerative Feedback Repeaters for Programmable Interconnections

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FPGA performance is limited mainly by the delay of the programmable interconnection network [1]. This delay increases quadratically with the number of series switches, and is a problem especially when the programmable switches are implemented using MOS transistors, since these have an appreciable resistance and capacitance. The delay can be reduced, at the cost of routability, by limiting the number of series switches per interconnection, or at the cost of area by inserting repeaters, as shown in Figure 1. Conventional bidirectional repeaters consist of sets of unidirectional tristate buffers and memory cells. Their benefit is limited due to high area and delay penalty.

Area and delay penalty can be alleviated by using a regenerative feedback that senses the beginning of a transition and subsequently enforces it. This requires one buffer and no memory cells. Figure 2 conceptually shows a network with such repeaters for direction-independent buffering. The concept is similar to the signal propagation in myelinated nerve axons [2].

The simple implementation using cross-coupled inverters does not function due to hard-latching, but this is avoided by using dynamic logic. Precharged regenerative feedback circuits have been used in memories and carry-chains [3, 4]. Implementations in Domino and NORA logic are shown in Figure 3. When the precharged node N is pulled below the threshold voltage of a sensing stage, the low level is enforced locally. When added to a chain of switches as in Figure 2, these circuits rapidly propagate a falling transition. The propagation delay decreases as the threshold voltage of the sense gate, measured with respect to the initial node voltage, is reduced, as shown in Reference 5. The NORA implementation is fastest, due to its small threshold voltage, but suffers from a limited noise margin and poor noise performance. Feedback repeaters allow faster signal propagation than conventional repeaters since the buffers are not directly in the signal path. Additionally, precharged regenerative feedback repeaters offer a reduction in area compared to the repeater of Figure 1 due to the elimination of a buffer, memory cells, and the pMOS pull-up transistor. However, the precharged circuit is not compatible with most FPGAs since it requires clocked monotonic signaling.

The self-timed, complementary regenerative feedback (CRF) circuit of Figure 4 addresses FPGAs. This is the complementary version of the circuit in Figure 3b, where the clock is replaced by the delayed inverse of the signal on node N. In steady state, both drivers are off, so N is not actively driven. In the case of a falling transition on node N, both inputs to the NOR gate are temporarily low, and the nMOS driver is turned on for approximately the imposed delay t_d. In the case of a rising transition, the complement occurs and the pMOS driver temporarily turns on. Thus, this circuit can be used to propagate rising and falling transitions. The propagation speed through a chain of switches with CRF repeaters depends on the delay and threshold voltage of the NOR and NAND gates, and the size of the driver transistors. The delay t_d of each repeater must be long enough such that the repeater can activate the next repeater before the local current path is turned off. Otherwise, stored charge may initiate the reverse transition, resulting in oscillations. This constraint on t_d can be relieved by using a Schmitt-trigger instead of an inverter (Figure 4). The delay t_d must also be shorter than the pulse width of the propagated signal.

A test chip in MOSIS 1.2μm-well CMOS is used to evaluate regenerative feedback repeaters. Figure 5 shows a micrograph of the chip. Several chains are implemented, each consisting of 64 MOS switches in series. Each intermediate node is loaded by 14 switches in the off state, representing unused switches in a typical programmable interconnection of an FPGA. Each chain employs a different combination of feedback circuits and switch types. The switches are either nMOS transistors with an external gate voltage V_{GG} (Figure 6a) or CMOS transfer gates (Figure 6b). The voltage V_{GG} can be set above V_{DD} for lower resistance and to avoid voltage drop. To evaluate many repeater placements, NOR and NAND gates are added at the clock input or in the delay loop such that the feedback can be enabled externally. The delay t_d of the CRF repeaters is controlled by an external supply V_{delay}. At certain nodes, the signal is observed by a measurement circuit consisting of nMOS and pMOS differential pairs and an inverter, with outputs connected to a balanced network of multiplexers for measurement of relative delays and transition times. All reported results are for chain length 64, with 14 extra switches per node, V_{DD}=5V, and nMOS switches with V_{GG}=6.5V. Figure 7 shows the measured propagation delay versus repeater interval k, for NORA feedback and CRF repeaters. The delay monotonically increases with the repeater interval k. Due to added loading by the disabled repeaters, the delay is overestimated for k>1.

Figure 8 compares delays per stage, expressed in units of RC per stage, for simulations of the falling transition in four chains with variable repeater interval k, and for which disabled repeaters are removed. The first chain uses NORA feedback repeaters, with 0.9V threshold. The second chain, CRF(2.5V), uses CRF feedback repeaters, with 2.5V threshold. A third chain, CRF(0.9V), uses CRF feedback repeaters that have a NORA-like sensing stage with 0.9V threshold. The fourth chain is derived from an equally routable network using conventional repeaters of equal driver strength. The CRF(0.9V) chain is slower than the NORA chain due to higher loading by repeaters. This is more prominent as repeaters are placed more frequently. The CRF curves show the influence of sense gate threshold on overall delay. While the noise margin of a NORA implementation is probably too small to be used on an FPGA, the ideal gate is one with skewed thresholds in the sense gates. In this experiment, the NORA chain is 2.1x faster than the conventional approach. The CRF(0.9V) chain is 1.8x faster, and the CRF(2.5V) chain is 1.5x faster. Sparser placement of smaller CRF repeaters still yields smaller delay than the conventional approach.

Acknowledgments

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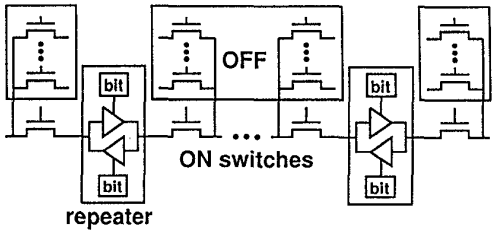

Figure 1: Interconnection network using pairs of unidirectional tristate buffers to limit delay.

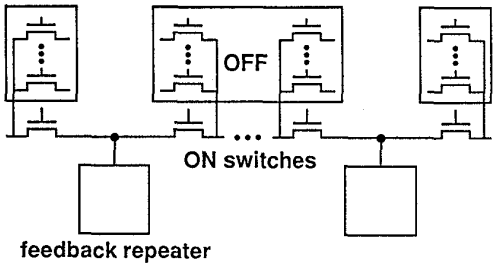

Figure 2: Interconnection network using regenerative feedback repeaters.

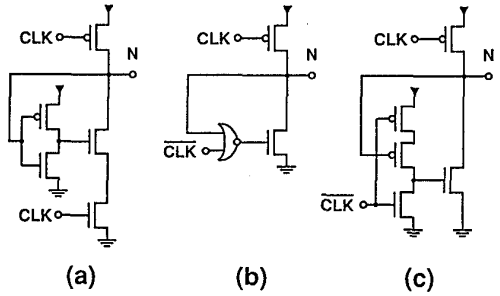

Figure 3: Precharged regenerative feedback circuits: (a) Domino, (b) Improved Domino, (c) NORA.

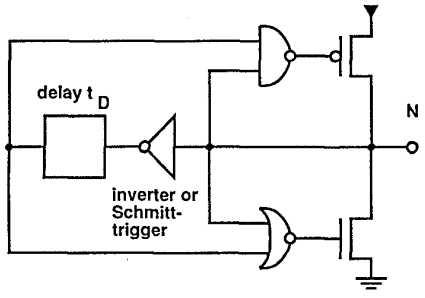

Figure 4: Self-timed complementary regenerative feedback (CRF) repeater.

Figure 5: See page 348.

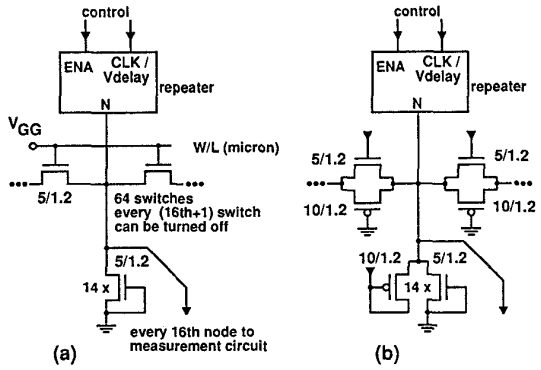

Figure 6: Switches: (a) nMOS transistors with externally supplied V_{GG}, (b) CMOS transfer gates.

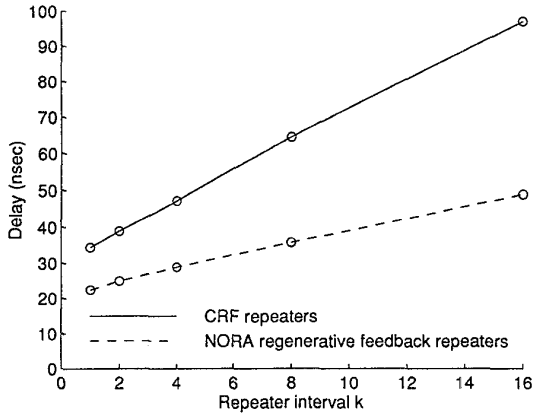

Figure 7: Measured delays through 64 switches for NORA feedback and CRF repeater chains.

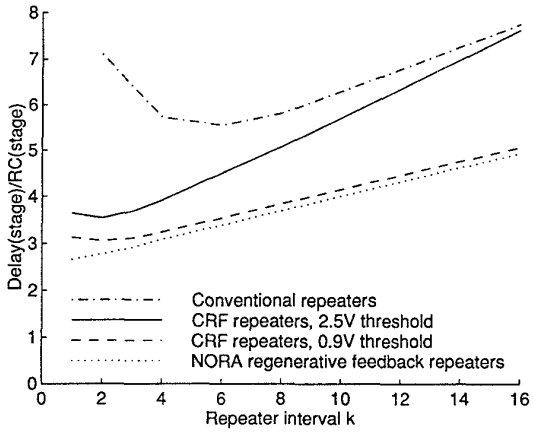

Figure 8: Simulated chain propagation delay of (a) NORA, CRF(0.9V), CRF(2.5V), & conventional repeaters.

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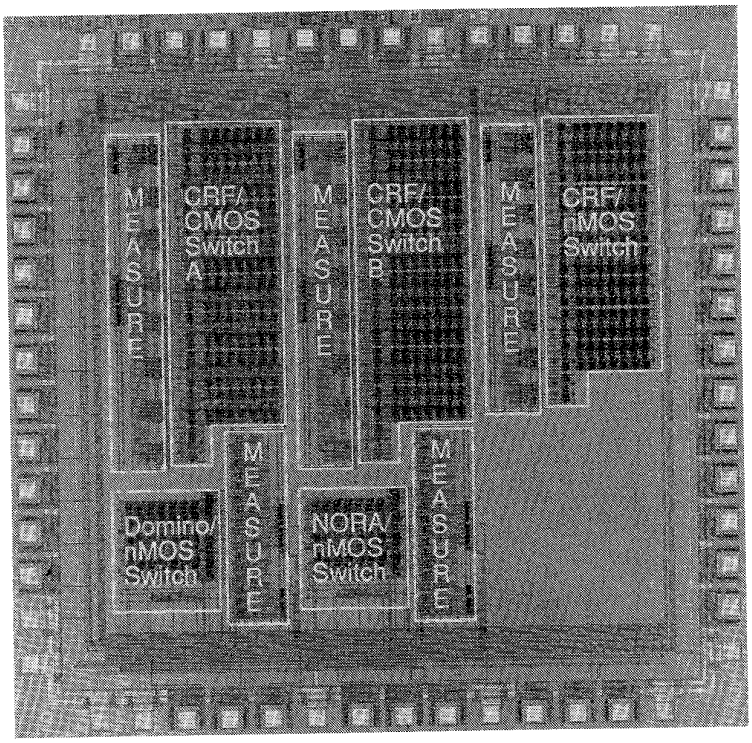

Figure 5: Regenerative feedback repeater test chip micrograph.

TA 7.1: A 3.3V 50MHz Synchronous 16Mb Flash Memory

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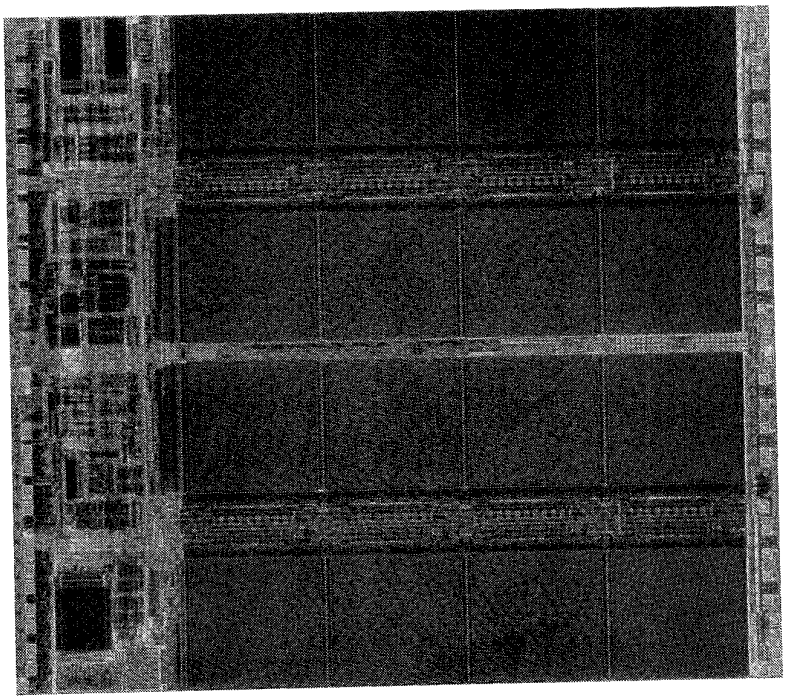

Figure 7: 16Mb flash memory chip micrograph.