TP 13.5: A CMOS Area Image Sensor with Pixel-Level A/D Conversion

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Charge-coupled devices (CCD) are at present the most widely used technology for implementing area image sensors. However, they suffer from low yields, consume too much power, and are plagued with SNR limitations due to the shifting and detection of analog charge packets, and the fact that data is communicated off chip in analog form [1].

Several alternatives to CCD area image sensors use standard CMOS technology. Self scanned photodiode arrays are used to produce both binary and gray-scale image sensors [1, 2]. Bipolar junction phototransistor arrays, and charge injection arrays are used [3, 4]. However, these alternatives can suffer from low resolution due to limited pixel observation time, limited SNR due to analog sensing, and, as with CCDs, data is communicated off chip in analog form.

This paper describes an area image sensor that can potentially circumvent the limitations of CCDs and their alternatives.It uses a standard CMOS process and can therefore be manufactured with high yield. Digital circuitry for control and signal processing can be integrated with the sensor. Moreover, CMOS technology advances such as scaling and extra layers of metal can be used to improve pixel density and sensor performance. The analog image data is immediately converted to digital at each pixel using a one-bit sigma-delta modulator [5]. The use of sigma-delta modulation allows the data-conversion circuitry to be simple and insensitive to process variations [5]. A global "shutter" provides variable light input attenuation to achieve wide dynamic range [2]. Data is communicated off chip in a digital form, eliminating the SNR degradation of analog data communication. (Figure 1)

To demonstrate the viability of the approach, an area image sensor chip is fabricated in a 1.2μm CMOS technology. A functional block diagram of the chip is given in Figure 2. It consists of an array of 64x64 pixel blocks, a clock driver, a 6:64 row address decoder, 64 latched sense amplifiers, and 16 4:1 column multiplexers. The chip also contains data compression circuitry not described in this paper. A die micrograph is given in Figure 3 and a summary of the main characteristics of the chip are listed in Table 1.

A circuit schematic of the function implemented at each pixel is given in Figure 1. The phototransistor is a vertical bipolar pnp transistor. The emitter is formed using source-drain p^+ diffusion, the base is the n-well surrounding the emitter and the collector is the p^- substrate. The n-well is exposed to light, while the rest of the circuitry is covered with the second level of metal to reduce the chance of photon-induced latch-up. Physical construction and operation of bipolar phototransistors are described in References 7 and 6. Control of the input photocurrent is by setting the duty cycle (the ratio between the on and off times) of the shutter input SHUTTER - the higher the duty cycle, the larger the input photocurrent. Current from the phototransistor is integrated on C1 and quantized using a regenerative latch clocked via PHI2. The quantized value is converted into a current using a 1b D/A converter and fed back to the input capacitor C1. The duty cycle of PHI1 and the voltage VBIAS1 control the magnitude of the feedback signal Delta. PHI1 and PHI2 constitute a two-phase nonoverlapping clock. At the completion of each two-phase clock cycle a single bit is produced. The bit is read by enabling the word line WORD. If the bit is high the precharged bit line BIT is pulled down and sensed by a simple single-ended sense amplifier.

The operation of the area image sensor chip is as follows: after an image is focused on the chip the sigma-delta modulators are reset via the global RESET signal. SHUTTER is then globally set to maximize image SNR without saturating the data conversion circuitry. Next the sigma-delta modulators are globally clocked at a rate F_s above the image frame rate $2F_d$. This is necessary since a sigma-delta modulator reduces quantization error at the cost of extra data. At the end of each clock cycle the outputs of the sigma-delta modulators form a 64x64 array of bits referred to as a "bit plane." Each bit plane is read out row by row. The image is fully captured using a number of bit planes determined by the target SNR. Using the theoretical analysis in Reference 5, the number of bit planes L needed versus SNR is given by

$$SNR = 9\log_2 L - 5.2dB.$$

The maximum achievable SNR is measured at 61dB. SNR degradation due to charge injection of digital circuitry close to analog sensors is negligible since the frequency of operation is very low (1kHz) and the circuitry consumes less than 20nA per pixel.

Figure 4 shows the output from a single-pixel sigma-delta modulator.

The digitized pixel values are reconstructed using a decimation filter [5]. Depending on the application, this reconstruction may be implemented in software, using special-purpose hardware external to the sensor, or integrated with the sensor. In a low-resolution application where no local reconstruction is needed, e.g. video phone or surveillance camera, the sensor digital output is compressed and immediately transmitted. Reconstruction is at the receiving end using general- or special-purpose hardware. If the image is to be displayed or processed locally one or more decimation filters are integrated with the sensor and an external RAM is used. Pixel values stored in RAM are recursively updated by reading into the sensor, updating their values using the decimation filters and the new bits from the corresponding sigma-delta modulators, and storing the new values back into the RAM. This scheme appears feasible even for a sensor with as many as 1M pixels operating at 30 frames per second at 8b-per-pixel resolution.

The sensor can achieve a dynamic range (ratio of maximum non-saturating photocurrent to dark current) potentially greater than 93dB. This is because the magnitude of the photocurrent can be varied by a factor of 1000, or 60dB, and the maximum measured SNR is approximately 33dB with the SHUTTER duty cycle set at 100%, the frame sampling rate set at 30Hz, and the oversampling ratio set at 64.

Figure 5 shows a scan from a 35mm print, and the image obtained by the sensor when contact exposed to the 35mm negative. The sensor estimated total power of less than 1mW is significantly lower than that of other types of image sensors.

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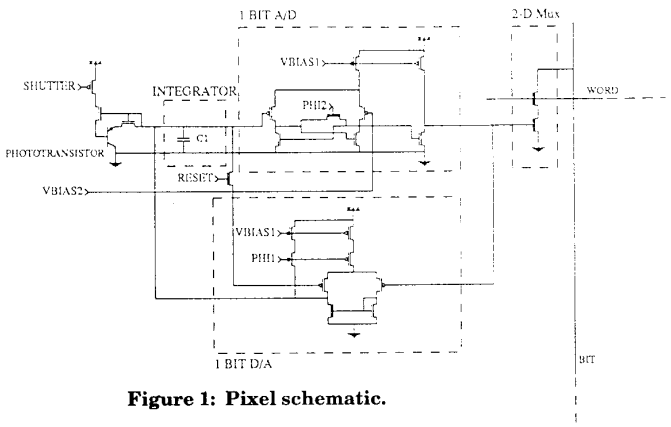


Figure 1: Pixel schematic.

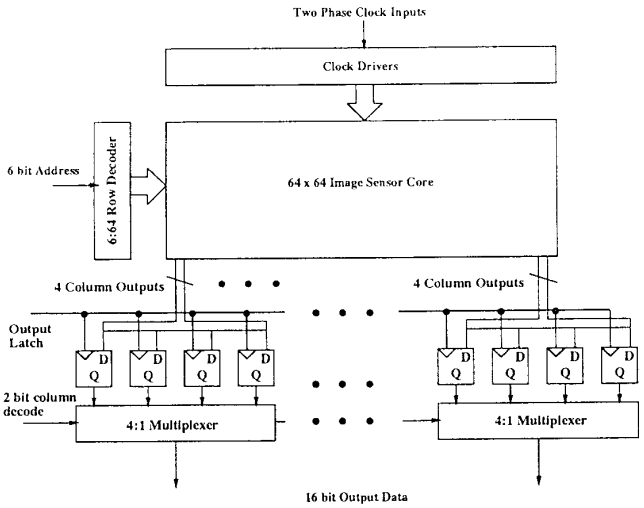


Figure 2: Image sensor chip functional block diagram.
Figure 3: See page 344.

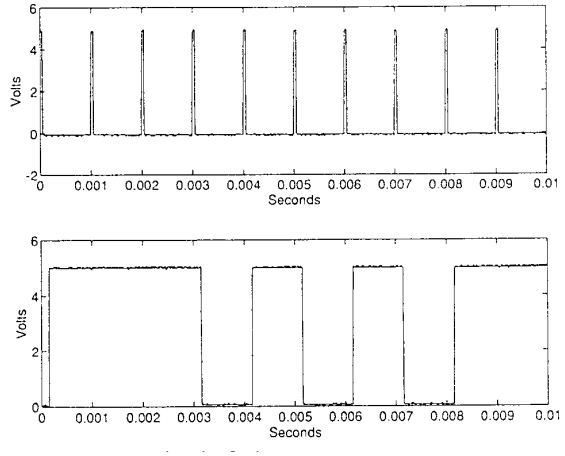
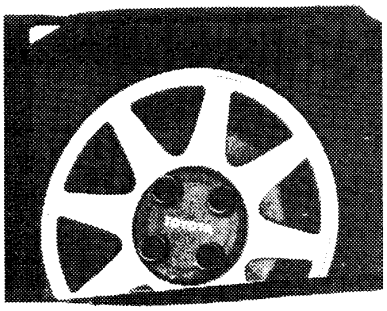


Figure 4: Single-pixel sigma-delta modulator output from HP54601A. PHI2 (top), pixel output (bottom).



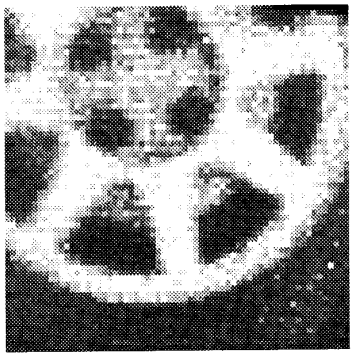


Figure 5: 300dpi scan of print from negative (top). 64x64 image by sensor using 35mm negative contact exposure (bot.).

CMOS technology	1.2μm 2-metal, 1-poly, n-well
Die area	6.5x5.0mm²
Pixel area	60x60μm²
Transistors/pixel	22
Phototransistor area	105μm²
Package	84-pin PGA
Supply	5V
Maximum SNR	61dB
Dynamic range	93dB
Dissipation w/o pads	<1mW
Measurement T	23°C

Table 1: 64x64 area image sensor characteristics.

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