[See page 309 for Figure 1]

SESSION VII: GATE ARRAYS

WPM 7.5: A CMOS Electrically Configurable Gate Array

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PRESENT PLD PROGRAMMING technologies and architectures have not allowed efficient integration of a wide variety of applications exceeding a few hundred gates[1,2]. Mask programmable gate arrays, on the other hand, offer the architectural flexibility and efficiency to integrate thousands of gates, but at the expense of long development time and high engineering development cost.

The architecture of the CMOS electrically-configurable gate array to be described, combines flexibility of mask programmable gate arrays and convenience of user-programmable PLDs; Figure 1. The inplementation is facilitated by a configurable interconnect tachnology based on a one-time, two-terminal programmable, low-impedance circuit element[3]. The electrical characteristics of this element are more suitable for one chip integration than preciously published anti-fuses[4]; Table 1. The device has been fabricated using 2μm N-well CMOS technology with two-layer metallization. Four transistor types were used to optimize logic-speed path and programming path operating voltages.

The architecture of the device[5] is similar to that of gate arrays; Figure 1. It consists of configurable logic modules organized in rows and columns and separated by wiring channels. Unlike gate arrays, however, the channels contain segmented *horizontal* metal tracks. The inputs of the logic modules are connected to dedicated *vertical* metal wire segments. Other vertical wire segments not dedicated to any module input or output are also provided for vertical interconnection. Anti-fuse elements are located at the intersection of the horizontal and vertical wire segments, and between adjacent horizontal and vertical wire segments. To program an element, 18V is applied across its terminals, while all other elements are subjected to no more than half that voltage. This is accomplished by a procedure that utilizes the wiring segments, pass transistors between adjacent segments with shared control lines, and serial addressing circuitry at the periphery of the array. A programmed anti-fuse element at the intersection of, or between, two wire segments provides a low resistance bi-directional connection between the two segments.

Choice of the lengths of the horizontal and vertical wire segments, as well as the number of tracks in each channel, provides routing flexibility comparable to that of gate arrays. The similarity of this architecture to that of gate arrays can be best understood by drawing a parallel between the programmable anti-fuse elements and the vias introduced during the fabrication of gate arrays. The small size of the via allows the gate arrays to contain an extremely large number of potential via sites, of which a very small fraction is needed to implement an application. Similarly, the size of the anit-fuse elements permits packing them as close as the metal pitch of the CMOS technology. Thus, a large number of these elements can be included in the device. Again, only a very small fraction of these anti-fuse elements need to be programmed to implement any application. This allows gate array-like extension of the device architecture by adding more logic modules and imcrementally increasing the number of wiring tracks in each channel.

The configurable logic module has 8 inputs and one output. This module was chosen for its efficiency in implementing both combinatorial and sequential circuits and for its optimum utilization of routing resources. This module implements all two- and three-variable functions and some four-variable functions. It may also be connected to form latches and flip flops. No predetermined hardwired latches or flop flops are implemented or needed in this gate array since latches and flip-flops may be implemented anywhere in the array to suit the requirements of the application. The I/O architecture is also quite flexible. Any I/O module may be configured as input, output, or bi-directional I/O by programming the appropriate anti-fuse elements.

An important aspect of the device is that its design is testable. Since the programmable element is an anti-fuse, the array circuits are normally open with no circuit connections established to external I/O buffers. Testability circuits are, therefore, implemented to allow full testing of any module in the array, I/O buffers vertical and horizontal tracks, as well as all programming circuits in the device before configuration. The overhead of these testability circuits is minimized by sharing the periphery circuits and the pass transistors needed for programming. Appropriate test patterns are applied to the testability circuits before configuration to ensure quality devices and programming yield.

The key characteristics of the chip are listed in Table 2; Figure 1. The device is supported by an automated placement and routing software capable of mapping applications utilizing up to 95% of the array modules. The frequency counter circuit uses 283 logic modules, out of the available 295, and 37 I/O modules; Figure 2. The speed of the circuit under normal operating conditions is 25MHz. If implemented with a mask programmable gate array, this example would require over 1,000 gates. The waveform of a counter output is shown in Figure 3. Other examples of applications that have been mapped in the array include a model with a carry-look-ahead circuit and an 8 x 8 parallel multiplier.

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[1] Wong,S., So,H., Hung,C., Ou,J., "CMOS Erasable Programmable Logic with Zero Standby Power", *ISSCC DIGEST OF TECHNICAL PAPERS*, p.242-243, Feb., 1986.

[2] Hsieh,H., Duog,K., Ja,R., Kanazawa,R., Ngo,L., Tinkey, L., Carter,W., Freeman,R., "A Second Generation User-Programmable Gate Array", *Proceedings of the CICC*, p.515-521; May 1987.

[3] Patent pending.

[4] Stopper,H., "A Wafer with Electrically Programmable Interconnections", *ISSCC DIGEST OF TECHNICAL PAPERS*, p.268-269; Feb., 1985.

[5] Patent pending.

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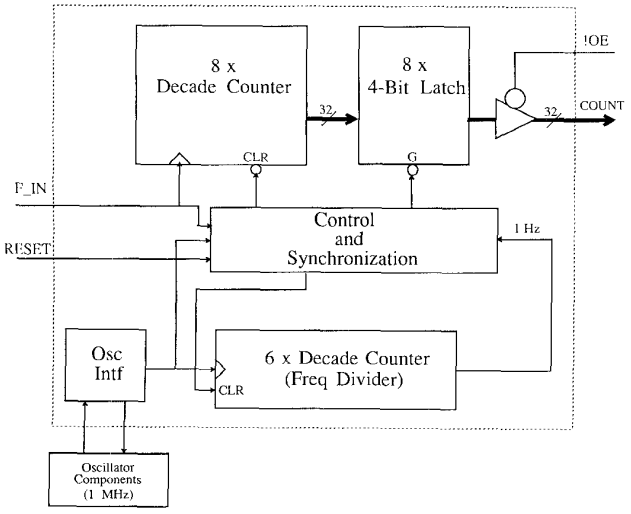

FIGURE 2 – Frequency counter.

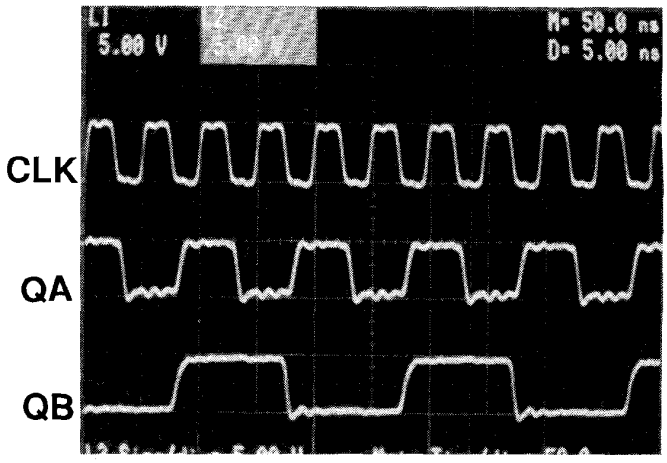

FIGURE 3 – Counter output waveforms.

TABLE 1 – Technology Overview

Process: NWELL, 2 micron, Double layer metal CMOS

TransistorType	Gate Oxide	Leff	Voltage
N Low Volt	250 A	1.1 u	5 V
P Low Volt	250 A	1.2 u	5 V
N High Volt	400 A	1.5u	20 V
P High Volt	400 A1	.8 u	20 V

Anti-fuse Characteristics:

Programming Voltage	18 V
Programming Time	<10 ms
Programming current	<10 mamps
On Resistance	<1K ohms
Off Resistance	>100M ohms

(right)

TABLE 2 – Chip characteristics.

chip size	240x360 mil^2
package	84 LCC
standby current	<5 mA
number of modules	295
no. of programming elements	112,000
number of transistors	60,000
clock network	delay = 6 ns*
	max skew < 3 ns*
module performance	5 ns
latches	
setup	6 ns*
hold	1.5 ns*
clock to out	5ns*
max no. of user defined pins	55
configurable I/O buffers	TTL
input: delay	6 ns*
output: delay	12 ns*
drive	4 mA
	bi-directional
diagnostic features	microprobes

*All delays are measured at 5 V, 25°C temp, and a typical net with fanout of 3. Output delay and drive is measured at 50 pF loading.

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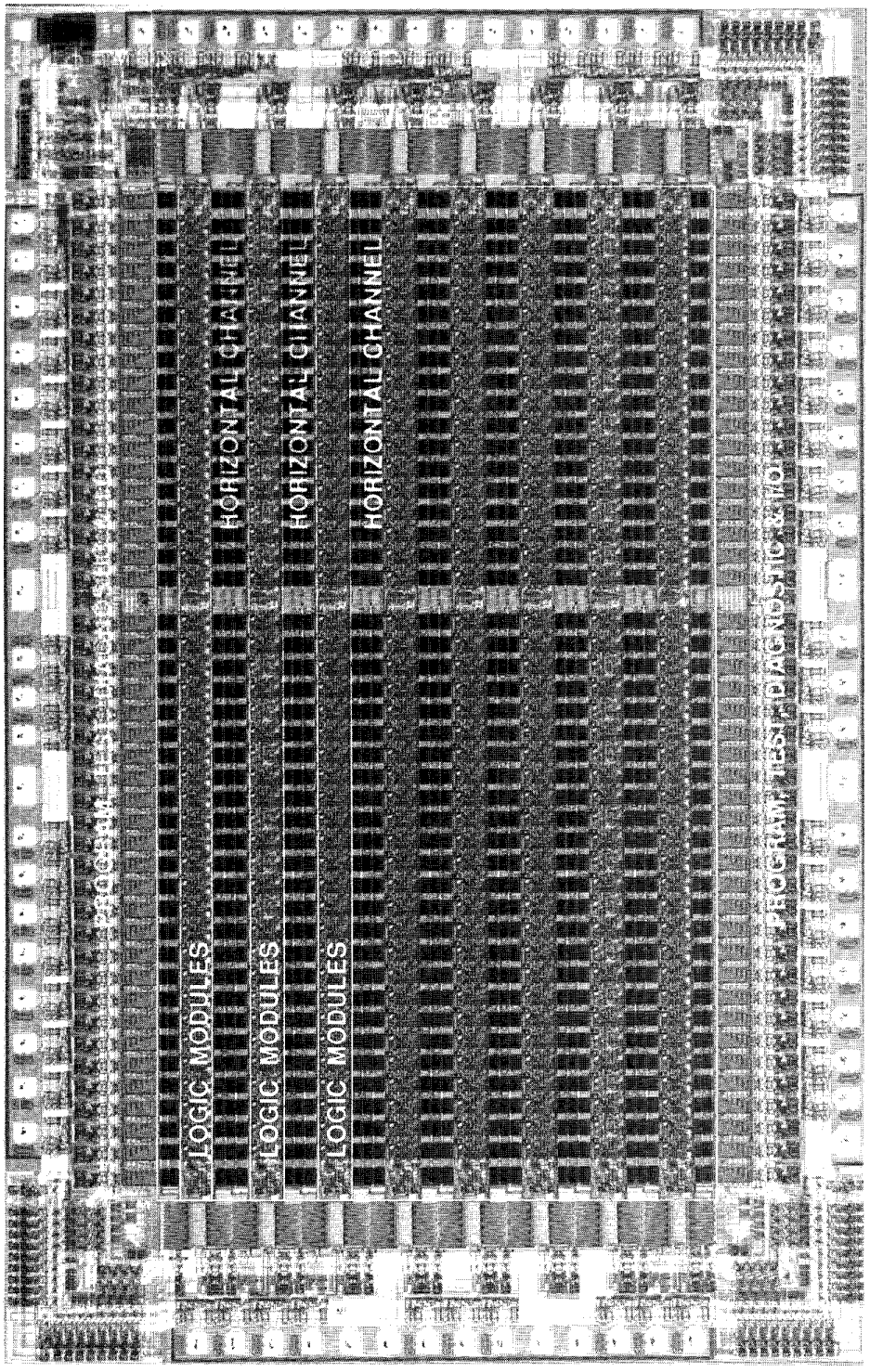

FIGURE 1 – Microphotograph of the chip.