[See page 345 for Figure 2.]

SESSION XV: HIGH-SPEED DIGITAL CIRCUIT TECHNOLOGY

THPM 15.5: A CMOS 32b Wallace Tree Multiplier-Accumulator

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IN SPITE OF THEIR SPEED ADVANTAGE, carry save adder trees (CSA or Wallace trees[1]) are seldom, if ever, used in the design of monolithic multipliers. The main reason is the general belief that they are very difficult to lay out efficiently[2,3]. There is also no published algorithm, other than certain simple rules[4] to interconnect a CSA tree so as to minimize the overall propagation delay. Nor is there a published algorithm for designing the final adder stage of a parallel multiplier to take full advantage of the different arrival times of the signals from the tree (or array).

The design of the 32b multiplier-accumulator to be described in this paper uses algorithms for the layout and delay optimization of CSA trees, and carry select adders: see Tables 1 and 2 for main features, and Figures 1 and 2 for block diagram and plot of layout. The results demonstrate that CSA tree multipliers can in fact be laid out efficiently and that a systematic design of the final addition stage can eliminate the need to use carry lookahead adders or a dynamic carry chain.

The multiplier has been automatically compiled**. The program produces a final layout for a circuit to perform the operation of $A \cdot B + \Sigma A_i$, where A, B, and the A_i's are integers of arbitrary sizes. The program takes as an input a characterized cell library, the sizes of the numbers to be multiplied and accumulated (i.e., A, B, A_i's). The program first produces an interconnection pattern for the optimized CSA tree and an optimal partitioning for the carry select adder stage. An interesting fact to note is that the interconnection of the full adder cells constituting the CSA tree as well as the partitioning of the carry select adder are highly dependent on the input-output delays of the cells in the library. The second phase of the program performs placement, routing, and compaction according to the prespecified floor plan. The rest of the multiplier design (output Mux, . . . etc.) has been designed using standard cells and a channel router. In addition to the 32b multiplier-accumulator, the program has also been used to produce the 16 x 16 multiplier-accumulators used in our structured arrays[5].

This chip has been fabricated in both 2μ and 1.5μ (by shrinking N-channel gate length to 1.5μ CMOS and P-channel to 2μ technologies). The 1.5μ version is 25% faster; i.e., worst case delay of 42ns.

Acknowledgments

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**MACGEN.

[1] Wallace, C.S., "A Suggestion for a Fast Multiplier", *IEEE Trans. Electron Comput.*, p. 14-17; Feb., 1964.

[2] Harata, Y., Nakamura, Y., Nagase, H., Takigawa, M. and Takagi, N., "High Speed Multiplier using a Redundant Binary Adder Tree", *Proceedings of the IEEE ICCD: VLSI in Computers*, p. 165-170; Oct., 1984.

[3] Chu, K. and Sharma, R., "A Technology Independent MOS Multiplier Generator", *ACM IEEE 21st Design Automation Conference Proceedings*, p. 90-97; June, 1984.

[4] Lerouge, C., Girard, P. and Colardelle, J., "A Fast 16-Bit NMOS Parallel Multiplier", *IEEE Journal of Solid-State Circuits*, Vol. SC-19, No. 3, p. 338-342; June, 1984.

[5] Walker, R., Yin, P., Lobo, K., Chang, Y., Tsao, P., Yuen, A. and Hsue, J., "Structured Arrays — A New ASIC Concept Provides the Best of Gate Arrays and Cell Based Custom", *Proceedings of the IEEE Custom Integrated Circuits Conference* p. 252-257; May, 1985.

Process	2μm P-well CMOS*
Total Device Count	Approximately 45K
Chip Size (including pads)	7 mm x 7.8 mm
Multiplier-Accumulator Size	5.3 mm x 5.7 mm
Supply Voltage	5V $\pm$ 10%
Power Dissipation	1W max
Package	132 pin ceramic or plastic pin-grid array
Multiplier-Accumulator Time**	56 ns

**A 1.5μm version will also be fabricated.*

***Worst case $V_{DD} = 5V$, $T = 25°C$*

TABLE 1—Chip features.

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Multiplication Algorithm	Modified Booth encoding
Number Format	Integer or fraction two's complement or unsigned
Accumulation	68 bits positive or negative
Cell Design	Fully static design
Carry Save Adder Stage Design	Optimized tree, automatically placed, routed, and compacted*
Final Adder Stage Design	Optimized carry select adder, automatically placed and routed*

64-bit multiplication can be performed in four clock cycles

Round control for both integer and fraction formats

Separate clocks for X, Y, P and I registers

Full 68-bit or shifted 67-bit output can be read in two cycles

Accumulator can be preloaded (the full 68-bits in four cycles)

Tri-state, TTL level output buffers

Scan test design for all registers

**Using MACGEN*

TABLE 2—Architecture features.

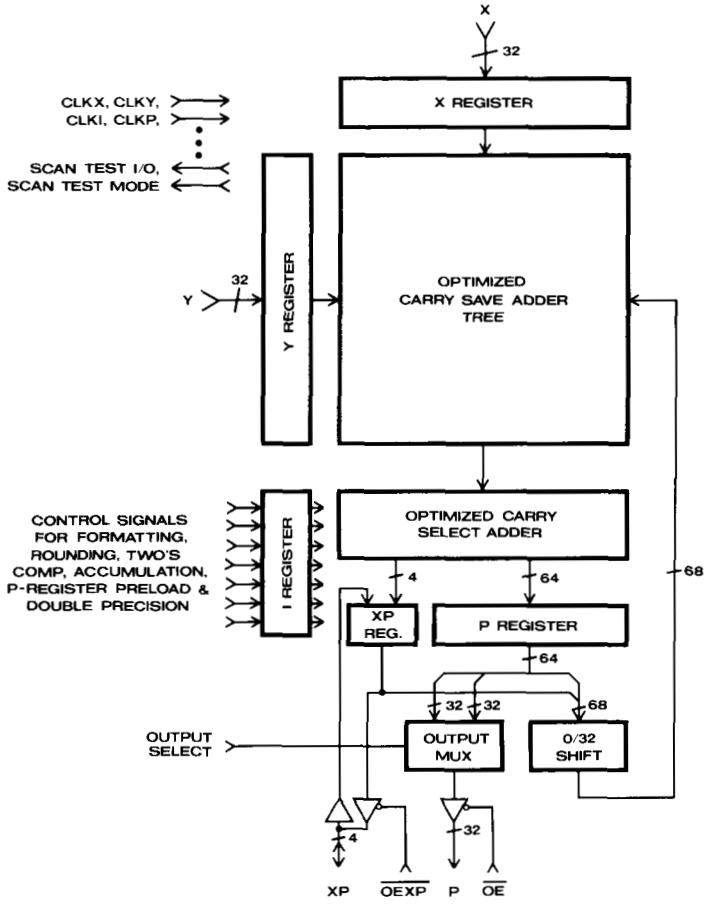

FIGURE 1—Block diagram of 32b multiplier-accumulator.

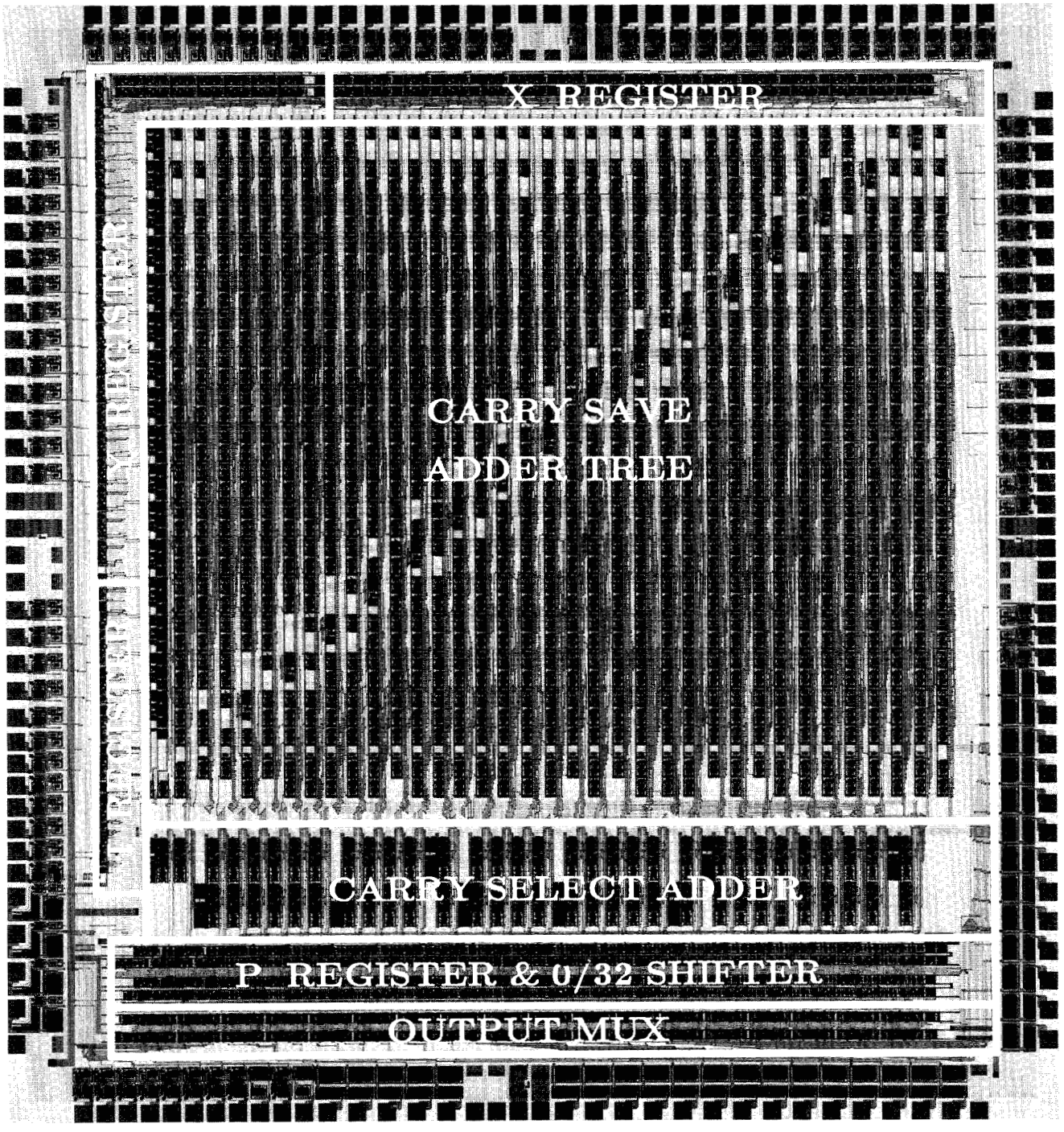

FIGURE 2—Plot of layout of 32b multiplier-accumulator.