A NEW STATISTICAL MODEL FOR GATE ARRAY ROUTING†

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ABSTRACT

A new statistical model for routing of gate arrays is described. The model takes into consideration the effect of gate utilization on wiring area requirement. Model computed wiring area estimates suggest that it is better (in terms of area and wire length) to use higher utilization and a relatively large number of tracks than low utilization and smaller number of tracks. This is shown to be consistent with the results of two experiments.

1. INTRODUCTION

The idea of estimating gate array wiring area via statistical modeling is due to Heller et al. [Hel78]. In [ElG81], El Gamal generalized the model in [Hel78] to two dimensions and provided simple upper bounds to the expected maximum congestion. The model in [ElG81] is not completely satisfying for the following reasons:

(i) The gates are organized in a two dimensional square grid with horizontal and vertical wiring channels. Most gate arrays are organized as rows of gates with horizontal wiring channels and vertical feed through routing areas (see Fig. 1).

(ii) All gates in the model of [ElG81] are assumed to be used. In practice only a fraction u of the gates is used (see Fig. 1).

(iii) In [El81], the wire generation distribution is assumed Poisson, which results in a non zero expected fraction of gates with zero connections; a clearly unrealistic assumption.

In this paper we introduce a wiring model that avoids the above problems. The new model assumes the organization in Fig. 1. The wire generation distribution is chosen by the user. The main new ingredient, however, is the ability to vary gate utilization and observe its effect on wiring area requirement.

In Section 2 the model is described. In Section 3, we investigate the layout of two designs on a commercially available gate array. By varying the model parameters, we predict that the overall area and average wire length can be decreased significantly if the array is allowed to have larger wiring area and smaller number of gates (i.e. larger gate utilization). This is shown to be consistent with the experimental results.

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2. MODEL AND BASIC RESULTS

The gate array organization used in the model is depicted in Fig. 1. There are N identical gates organized in n rows. There are t wiring tracks between every pair of rows. To simplify the analysis we assume as in [ElG81] that the array is part of a doubly infinite array.

Each gate of the array is used with independent probability u and not used with probability $\bar{u} = 1 - u$. The parameter u is referred to as utilization. Each used gate generates a number of wires according to an independent distribution P_λ with average λ. The trajectories of wires are determined independently and randomly as shown in Fig. 2. We assume that each wire travels sideways along the wiring channels in steps (as defined in Fig. 1) and downwards through unused gates.† The horizontal length of a wire is measured by the number of horizontal steps traveled by the wire, and the vertical length by the number of unused gates that the wire passes through. For Example, the wire in Fig. 1 has horizontal length = 4 and vertical length = 2. At any row, if a gate and the gate below it are used (Fig. 2a) then each generated wire terminates with probability γ, takes one step to the right with probability $\frac{1-\gamma}{2}$ or to the left with probability $\frac{1-\gamma}{2}$. If a gate is used and the gate below it is not used (Fig. 2b), each generated wire goes through the unused gate with probability β and takes one step to the right or left with equal probability $\frac{1-\beta}{2}$. A wire passing through an unused gate terminates at the gate below it, if it is used (Fig. 2c), with probability β and takes one step to the right or left with equal probability $\frac{1-\beta}{2}$. If a gate is not used and the gate below it is also not used (Fig. 2d), a wire passing through the top gate passes through the bottom gate with probability α and takes one step to the right or left with equal probability $\frac{1-\alpha}{2}$. Finally, each wire has an independent probability p of terminating or passing through a gate and $(1-p)$ of taking one more step (see Fig. 2e).

We denote by T_i the number of wires crossing the ith gate pair boundary line, the dotted line shown in Fig. 2e. The distribution of the number of wires passing through an unused gate is denoted by $B_{\alpha\lambda}$ with average $\alpha\lambda$. We denote by $\bar{R}_H$ and $\bar{R}_V$, the horizontal and vertical average wire lengths respectively.

If we assume that $\lambda, \alpha, \beta, \gamma, p, u$, and N are known it is easy to derive the following equations for $\bar{R}_H$, $\bar{R}_V$, a and

† The model can be easily generalized to cases where wires can go through used cells.

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the expected value of T_i (ET_i):

$$\bar{R}_V = \frac{\bar{u}(u\bar{\gamma}+\beta+\bar{\beta}\bar{u})}{1-\bar{u}((\alpha+\bar{\alpha}\bar{u})+u\bar{\beta})}$$

$$\bar{R}_H = (1/p)\left[(u\bar{\gamma}+\bar{u}\bar{\beta})+\bar{R}_V(u\bar{\beta}+\bar{u}\bar{\alpha})\right]$$

$$a = \frac{u(u\bar{\gamma}+\beta+\bar{\beta}\bar{u})}{1-\bar{u}(1+u(\alpha-\beta))}$$

$$ET_i = (\lambda/p)\left[u(u\bar{\gamma}+\bar{u}\bar{\beta})+\bar{u}a(\bar{u}\bar{\beta}+u\bar{\alpha})\right]$$

It is also easy to compute $B_{a\lambda}$, the horizontal and vertical wire length distributions, and to numerically compute an upper bound to the expected maximum congestion E max T_i in a manner similar to [ElG81],

3. VERIFICATION AND APPLICATION

In this section we check the validity of the model and we consider the implementation of two circuits on a commercially available gate array. The characteristics of the array and the circuits are as follows.

Array characteristics:

Technology: Two layer CMOS.
Organization: Shown in Fig. 1.
Type of Gates: Two input NAND.
Size:

Gate: 3 (horizontal) by 18 (vertical) grid units
Channel width: 16 grid units
Array: 22 rows by 191 columns.

Circuit characteristics:

Circuit-1:

Number of nets: 1100
Number of connection pins: 3569
Number of gates used: 2015

Circuit-2:

Number of nets: 1131
Number of connection pins: 3556
Number of gates used: 1569

We first check the validity of the model by comparing measured parameters from a layout of circuit-1 on the described array to those computed from the model (layout was obtained using conventional auto placement, auto routing, and interactive completion routines).

Measured parameters:

u = 0.48; λ = 1.465; α = 0.775;

β = 0.39; γ = 0.166;

The average horizontal wire length $\bar{R}_H$ = 13.15 (each k pin net of horizontal length l is considered as k - 1 nets each of horizontal length $\frac{l}{(k-1)}$). The measured horizontal wire length distribution is presented in Fig. 4. The average vertical wire length $\bar{R}_V$ = 1.446 (the multiple pin net breakup is similar to the horizontal dimension). The vertical wire length distribution is presented in Fig. 5. Finally the average channel congestion ET_i = 9.82 and the channel congestion distribution is shown in Fig. 6.

Model computed parameters:

Using the u , λ, α, β, γ, $\bar{R}_H$, $\bar{R}_V$, and the connections per gate distribution P_λ of Fig. 3 as input parameters the following quantities were computed from the model:

p = 0.11; a = 1.4;

ET_i = 9.9 (the measured value was 9.82);

E max $T_i \leq$ 21.8

Model predicted horizontal wire length, vertical wire length, and channel congestion distributions (Fig. 4,5 and 6 respectively) are computed and compared to the measured distributions.

An Application:

By varying the utilization u, while keeping λ,α,β,r,p fixed, we obtain the plot of channel width (for over 95% routability) shown in Fig. 7. The plot predicts that for E max T_i = 25, utilization can be improved to 80% . This means that circuit-1 could be routed, with 95% or more routing completion, on an array, similar to array-1 except having only 2418 gates and with 25 tracks per channel.

This prediction was tested by implementing circuit-1 on an array having 25 tracks/channel and with 15 rows and 175 columns. The percentage of nets automatically routed in the new array increased from 93.7% to 99.8% with a 22.4% reduction in area (over array-1). In addition to the increase in routability and the decrease in area, the average lengths in both dimension are estimated to decrease by 35% (Fig. 8).

Similar experiment was performed for circuit-2. The chosen array had 25 tracks/channel, 13 rows, and 160 columns. The result was a 16.4% increase in routability, 38.89% decrease in area from array-1 and a 42.1% increase in utilization.

These results suggest the following general conclusion:

If a gate array is to be designed to accommodate logic circuits with no more than k gates, then it is better (in terms of overall area and expected wire length) to use $N = k/0.8$ gates and a large number of tracks t (e.g., the corresponding E max T_i) than to use $k/0.5$ gates and a small number of tracks.

REFERENCES

[ElG81] El Gamal, Abbas, "Two-Dimensional Stochastic Model for Interconnections in Master Slice Integrated Circuits," *IEEE Trans. on Circuits and Systems*, Feb. 1981, pp. 127-138.

[Hel78] Heller, W., Mikhail, W., and Donath, W., "Prediction of Wiring Space Requirements for LSI," *Journal of Design Automation and Fault-Tolerant Computing*, pp. 117-144, 1978.

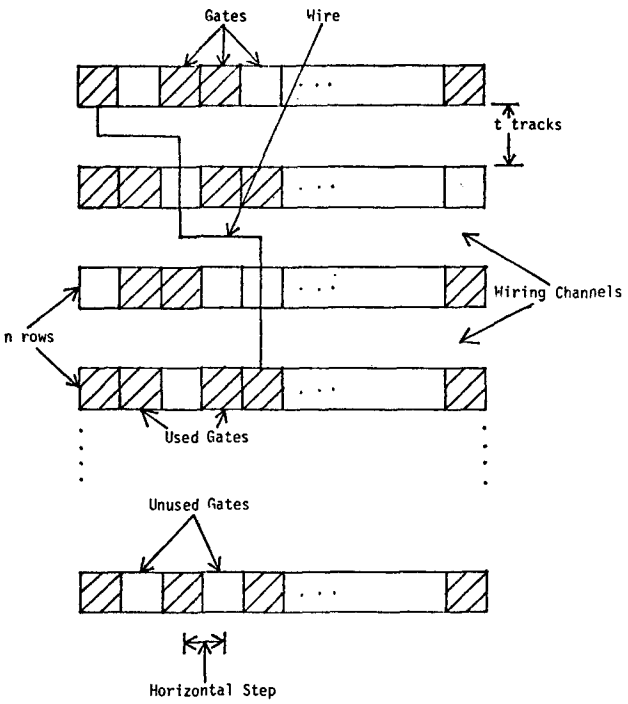

Fig. 1: Gate Array Organizaton

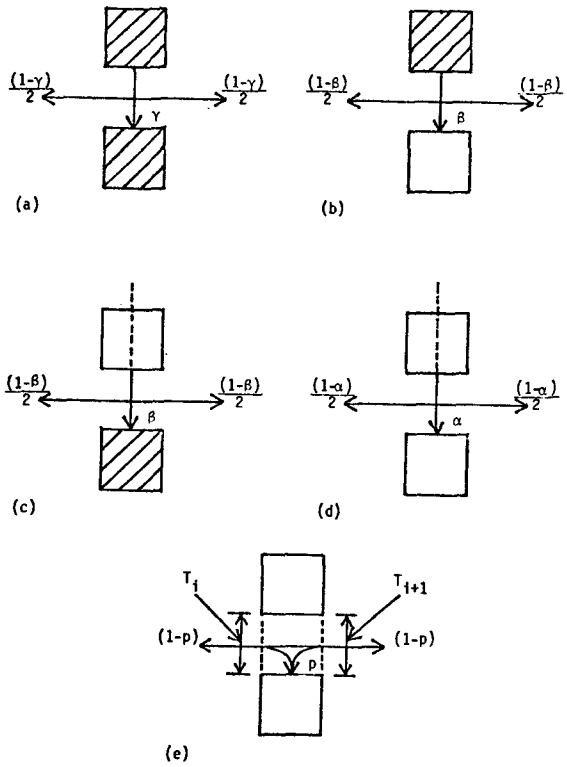

Fig. 2: Probabilities for Wire Trajectories

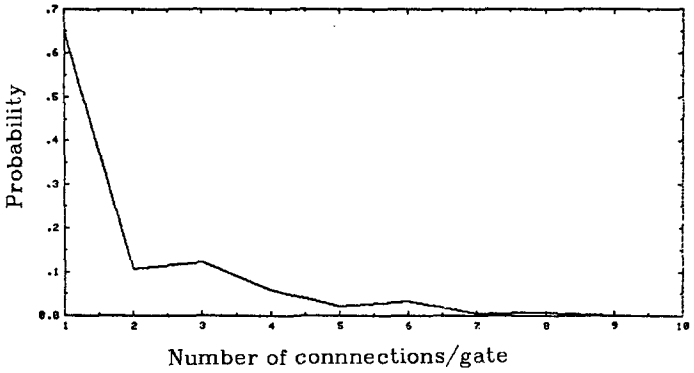

Fig. 3: Distribution of the Number of Connections/Gate

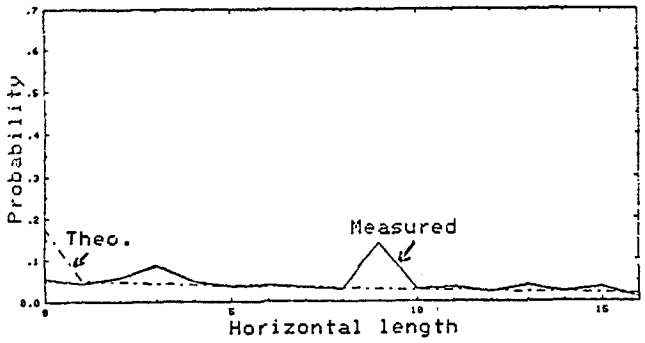

Fig. 4: Horizontal Wire Length Distribution

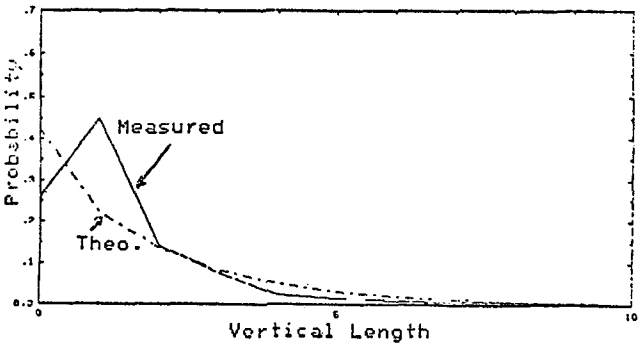

Fig. 5: Vertical Wire Length Distribution

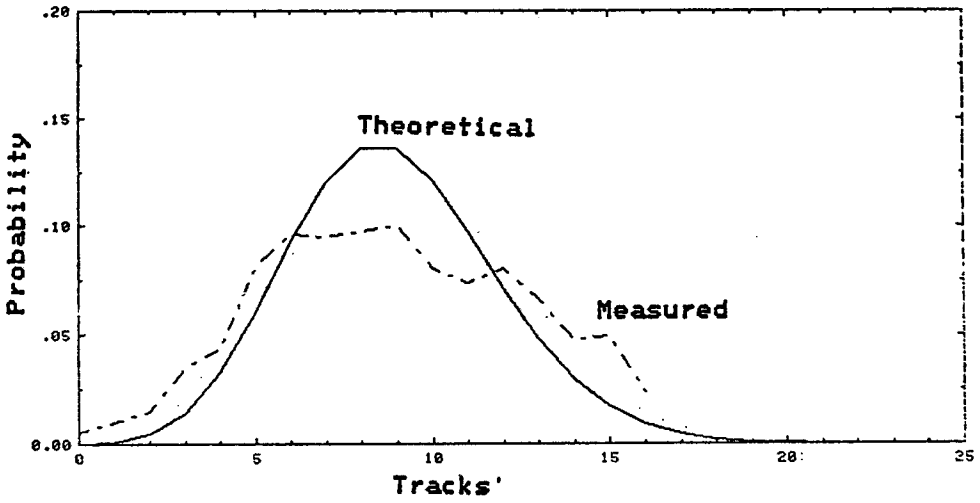

Fig. 6: Channel Congestion Distribution

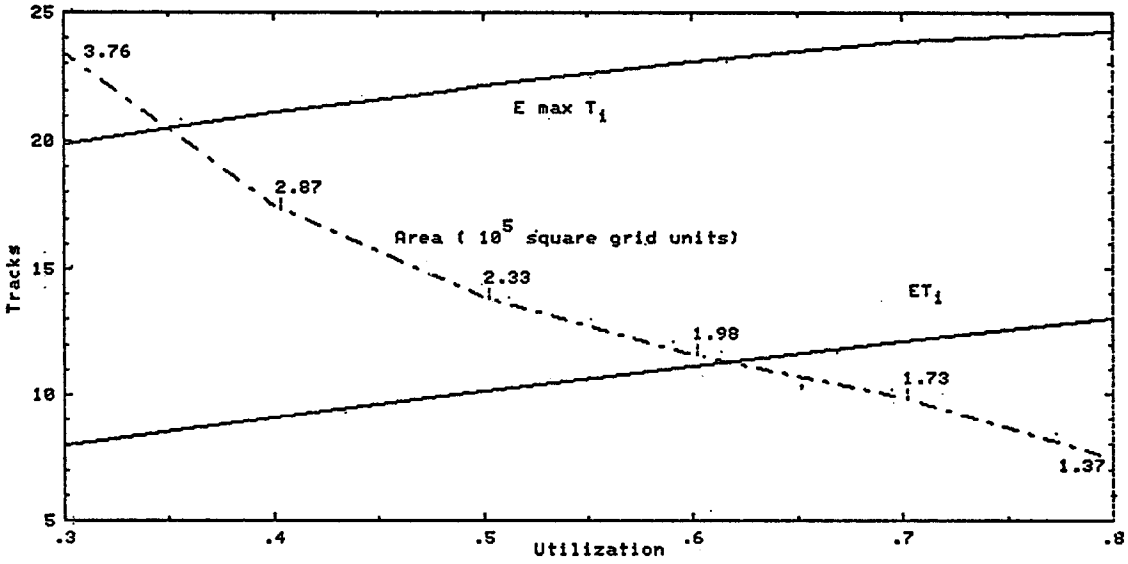

Fig. 7: ET_i , E max T_i , and Gate Array Area Versus Gate Utilization

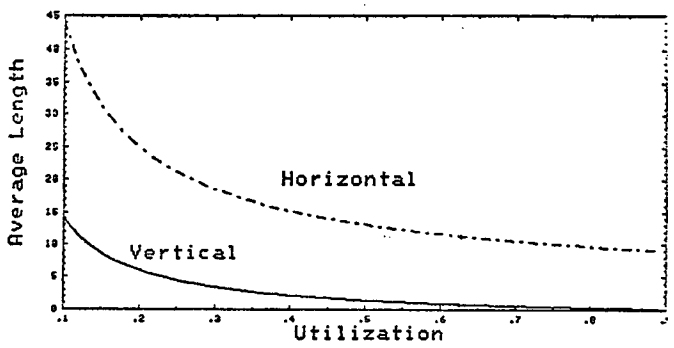

Fig. 8: Average Wire Length Versus Gate Utilization