

ON ROUTING FOR CUSTOM INTEGRATED CIRCUITS

Zahir Syed
Information Systems Laboratory
Stanford University
Stanford, California

Abbas El Gamal
Information Systems Laboratory
Stanford University
Stanford, California

M. A. Breuer
Department of Electrical Engineering - Systems
University of Southern California
Los Angeles, California

ABSTRACT

This paper presents a novel and effective strategy for routing custom integrated circuits as well as solutions to subproblems associated with this strategy. Given an initial placement of rectangular blocks, the routing strategy includes the following major steps: construction of a channel graph, estimation of channel widths (based on a statistical model for signal nets and topological routing of power and ground nets), placement modification to include the estimated channel widths, topological routing for signal nets, and finally track assignment.

Besides presenting an overview of our strategy, the following topics will be discussed in some detail: (1) necessary and sufficient conditions and a simple algorithm for single layer topological routing of power and ground nets, (2) a quadratic programming formulation for the placement modification problem, and (3) a fast algorithm for obtaining topological routes for signal nets.

1. INTRODUCTION

This paper deals with several key issues related to the layout of macro cells, called blocks, in a custom nMOS integrated circuit (IC). We restrict our attention to rectangular blocks of arbitrary size having terminals along their periphery. Normally these blocks represent functional elements, such as ALUs, MUXs and register arrays. We divide the layout process into the following major steps.

1. Initial placement of blocks
2. Construction of a channel graph
3. Final placement estimation:
 - a) estimation of routing space between blocks
 - i) power/ground space estimation
 - ii) net space estimation
 - b) placement modification to include estimated space
4. Determination of net trajectories

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a) topological routing

b) track assignment

5. Minor placement modification.

Steps 4 and 5 may have to be repeated several times before a final layout is obtained.

In this paper we include steps 2-5 of the above layout outline into the routing process. We will only discuss steps 2, 3, 4a and 5. Step 4b employs an extension of dogleg routing techniques [Deu76]. The initial placement (step 1) can be obtained by one of several means, such as automatically [Pre79, Lau80], manually and/or by using the floor plan approach proposed by Mead & Conway [Mea80].

We will now review the major concepts and motivation behind our approach. In the following section we will present our techniques in more detail.

1.1 Assumptions

We assume that the given initial placement is "good" and that all routing must be carried out between the blocks. Signal nets can be routed using two layers of interconnect, while power and ground must both be routed on one and the same layer, e.g., metal. Blocks are assumed to be rectangular, though this restriction is easy to remove by employing fracturing algorithms.

1.2 The Channel Graph

Given a layout consisting of blocks, the spaces between blocks are called channels. It is within these channels that all signal nets, power and ground must be routed. The channels can be modeled (represented) via a channel graph. Figure 1 illustrates a simple block configuration and its corresponding channel graph. An edge in the graph represents a channel, while a vertex in the graph represents the intersection of 2, 3, or 4 channels. A simple algorithm is used for constructing the channel graph. This algorithm is not presented here.

1.3 Final Placement Estimation

In this step, a prediction of the location of each block in the final layout is obtained. An accurate prediction is considered crucial for two reasons:

1. the criterion used for obtaining minimum distance interconnection paths is meaningless unless the predicted placement is close to the final placement.
2. An accurate prediction can drastically reduce

the number of track assignments and minor placement modification iterations.

Placement prediction is done first in the horizontal direction, then in the vertical direction (or vice versa). The main steps for the horizontal phase are described in the following three subsections.

1.3.1 Power and Ground Space Estimation

We have identified a necessary and sufficient condition on the topology of the power and ground terminals for each block to ensure a planar routing of power and ground. If each block satisfies this condition, then power and ground can be routed using the algorithm presented in Sec.2. Actual segment widths of these nets are used for the estimation.

1.3.2 Signal Net Space Estimation

Deterministic procedures to estimate the width of a channel (e.g., [Per77]) require the following information:

- a) list of nets that will partially or wholly exist inside the channel
- b) location of terminals at which some of the nets in the above list will terminate.

Unfortunately to obtain the above information the placement has to be fixed. But it cannot be because the number of wires in each track determine the minimum width of a channel. To solve this dilemma we employ a statistical procedure for estimating the width of each channel. This approach is an extension of the work of Heller et al. [Hel78] and El Gamal [ElG81a]. More details on our technique can be found in [Sye81, ElG81b]. The results of this analysis is the expected value of the maximum track demand for each channel.

Given the width of each power and ground segment in the channel graph and the channel width estimates for nets, the total estimated width of each channel can be determined.

1.3.3 Placement Modification

Given the estimated width of each channel, the blocks, which are normally considered to be adjacent to one another, can be repositioned by spreading them apart so that each channel has a width at least as great as the specified estimated width. This is accomplished (see Sec.3) via a combination of a critical path (a set of blocks and channels with the property that an increase in their dimension increases the overall layout area) technique [Pre77] and a quadratic programming technique [Gil72]. While reorganizing the placement horizontally (vertically), the critical path processing helps in minimizing the horizontal (vertical) dimension whereas the quadratic programming helps in minimizing the increase in the vertical (horizontal) dimension.

Once the placement has been modified it may be necessary to compute a new channel graph before proceeding to the topological routing phase.

1.4 Topological Routing

Once the placement has been modified, distances can be associated with the channel lengths. Using a fast procedure for finding minimal length paths between nodes in a graph, minimal length paths between

nodes in nets can be rapidly determined. These paths define wire segments assigned to the various channels.

1.5 Minor Placement Modification

If the track assignment step fails to complete the routing, e.g., if some channels are not wide enough, the results of the routing are used as new estimates for channel widths and a corresponding reorganization of the blocks is carried out. The placement modification approach of Sec.1.3.3 is again used, but without altering the channel graph.

In order to guarantee routing completion after a few iterations, it may be necessary to make sure that the channel widths are only increased in the modified placement.

In the following sections we will present some of the details of the techniques which we have briefly summarized.

2. SINGLE LAYER TOPOLOGICAL ROUTING OF POWER AND GROUND

For simplicity of presentation we assume that: (1) there is a single power pad at the upper left corner and there is a single ground pad at the lower right corner of the IC, (2) power terminals on each block are on the upper and/or left edge, and ground terminals on the lower and/or right edge, and (3) blocks do not have internally connected power or ground terminals.

For the above assumptions the following steps can be used to obtain the required topological routing:

- a) check for the existence of single layer topological routing for the two nets.
- b) if the routing exists, do the following:
 - i) Connect every power terminal to the power net by propagating segments in the left or up directions. Obey the following rules:
 - 1) in every horizontal channel a power segment must be below a ground segment.
 - 2) in every vertical channel a power segment must be to the right of a ground segment.
 - 3) at any "T" intersection rules shown in Fig.2a must be obeyed.
 - 4) at any "+" intersection the rule shown in Fig.2b must be obeyed.
 - ii) Similarly connect every ground terminal to the ground net by propagating segments in the down or right directions only.
 - iii) Based on the power demands on the terminals compute the widths by binary tree traversal techniques [Hor78].

Existence of topological routing (under the above assumptions) can be easily checked by the condition given in the following theorem.

Theorem: If for every block there exists a cut that separates the power and ground terminals, a single

layer topological routing for the two nets can be obtained. Conversely if there is a block with power and ground terminals not satisfying the above constraint a single layer routing is not possible.

For a proof and generalization of this theorem and a more general algorithm, see [Sye81, Sye82].

3. PLACEMENT MODIFICATION

After estimating channel widths a reorganization of the blocks is needed to make the channels at least as wide as their estimates while minimizing layout area. While reorganizing horizontally, the area minimization is achieved by first finding locations for the critical blocks as dictated by the critical path analysis [Pre79]. This results in minimizing the horizontal dimension. Then the increase in the vertical dimension is minimized by computing locations for the non critical blocks, such that the relative shift between those and the critical blocks is minimal. This is achieved by the quadratic programming technique presented in [Gil72]. We will only present the types of constraints and the objective function used for quadratic programming.

There are two classes of constraints, one user specified, the other based upon the track demand in each channel. We will consider the x-direction only.

For the configuration shown in Fig.3a, we see that $x_j \geq x_i + l_i + W_{3,4}$, where $W_{3,4}$ is the track demand (signal nets, power and ground) for channel (3,4). We have an inequality of this form for each pair of blocks which are horizontally adjacent to each other, except when both blocks are critical. (The definition of horizontally adjacent blocks is similar to the definition of vertically adjacent blocks which is given below.) In case block i or j is critical, x_i or x_j will be a constant.

The situation shown in Fig.3b represents a user specified shear constraint. Here, because of the wiring between blocks i and j, we do not want their relative position to change. This is accomplished by the constraints $x_i = d_{ij} + x_j$.

The objective function is to minimize

$$\sum_{i,j} (d_{ij}^x - D_{ij}^x)^2 \quad (1)$$

where (a) the sum is taken over all vertically adjacent blocks, except when both blocks are critical, (b) block i is said to be vertically adjacent to block j if there is a horizontal channel defined by the lower side of block i and the upper side of block j and (c)

$$d_{ij}^x = x_i - x_j \quad \text{and} \quad D_{ij}^x = X_i - X_j$$

are, respectively, the initial and the final difference between the x coordinates of the left edges of blocks i and j. The d_{ij}^x 's are given while the D_{ij}^x 's are determined by the minimization of (1). In case block i or j is critical, X_i or X_j will be a constant.

Once the x coordinate of each block is fixed, the procedure is reapplied to determine the new y coordinate of each block.

Remark: Mathematical programming methods are computationally inefficient for problems with a large

number of variables. However, since the number of modules in a custom IC placement is usually small (≤ 50), the computation time of the proposed quadratic programming method is not excessive. For example, using a VAX 11/780 computer, a 38 block problem (45 variables, 120 constraints) was solved in 1 minute 37 seconds (CPU time), another 38 block problem (37 variables, 66 constraints) was solved in 19.2 seconds, while a 16 block problem (17 variables, 30 constraints) was solved in 3.3 seconds.

4. TOPOLOGICAL ROUTING

In this section a fast topological routing algorithm is presented. The algorithm determines a least cost trajectory (path) for every net through a set of connected channels and has the following advantages over the methods presented in [Pre79] and [Kan76]:

- i) the nets are naturally grouped by assigning them to channels.
- ii) the channel graph is never modified by adding new vertices.
- iii) the information needed for finding minimum spanning trees for nets is shared among a group of nets, hence leading to a significant reduction in CPU time.

These advantages are achieved by routing the nets, channel by channel, as follows. First, the channel with the largest number of nets connected to it is found. The edges of the channel graph are assigned costs as in [Pre79] and [Kan76]. The channel graph is then labeled starting from the chosen channel, and the trajectories of the nets found. The next channel to be processed is the one with the largest number of unrouted nets. The process of finding a channel, labeling the channel graph and finding net trajectories is repeated until all nets are routed. (Refer to [Sye81] for a more formal presentation of the topological routing algorithm.)

To see how trajectories are constructed, consider the layout depicted in Fig.1. Shown are the placement terminal locations and the channel graph for the layout. Terminals with the same superscript belong to the same net. Assume channel (7,8) is not to be used.

The first channel to be processed (the one with the largest number of nets) is channel (4,5).

To determine least cost paths, the vertices of the channel graph are labeled using Algorithm B of [Joh77]. This labeling is done twice for each processed channel. In Fig.4 the pair of numbers associated with each vertex represent the least cost distance to this vertex from vertex 4 (first labeling) and vertex 5 (second labeling), respectively.

The next step is to find the trajectories for the two terminal nets 1, 2 and 4 using these least cost distances. Consider net 1. First we must decide whether to use the labeling starting from vertex 4 or from vertex 5, and whether net 1 should leave channel (11,12) from 11 or from 12. This is done by finding the minimum of the four numbers (refer to Fig.4).

$$C_1 = 30 + d_4 + d_2$$

$$C_2 = 19 + d_4 + d_1$$

$$C_3 = 51 + d_3 + d_2$$

$$C_4 = 40 + d_3 + d_1$$

In this case C_2 is the minimum and therefore net 1 must leave channel (11,12) from 11 and enter channel (4,5) from 5. The rest of the trajectory is simply decided using the second least cost labels and starting from vertex 11 and ending at vertex 5. Thus net 1 will pass through vertices 5, 7 and 11. Nets 2 and 4 are routed similarly. Since channel (7,8) cannot be used, net 2 will avoid it and go through channel (5,6) instead.

To route a multiple terminal net (e.g., net 3 in Fig.1), we first use the labeling in Fig.4 to find least cost distances and trajectories between terminals p_{32}^3 and p_{21}^3 , p_{32}^3 and p_{22}^3 , and p_{32}^3 and p_{23}^3 .

Next, the channel graph is labeled starting from (2,6) and least cost distances and trajectories between p_{31}^3 and p_{23}^3 , and p_{22}^3 and p_{23}^3 are found. Finally, modification of Prim's [Pri57] minimum spanning tree algorithm is used to select the required trajectories from these distances. Observe that the minimum spanning tree for net 3 is a Steiner tree [Hor78], with a Steiner point at vertex 6. This occurs because we never allow more than one trajectory associated with a net to exist in any given channel.

5. DISCUSSION

The described routing procedure is not completely novel. Similar methods have recently been proposed for custom IC routing (e.g., [Kan76, Pre79, Lau80, San80, Hig80]). The common features among these methods are:

- i) the routing is divided into two phases: topological (or loose) routing followed by channel routing. In [Lau80] an extension of Hightower's algorithm [Hig69] is used instead of a channel router.
- ii) channel graphs are used (except in [Hig80]).
- iii) algorithms are restricted to treating rectangular blocks.
- iv) in the topological routing phase, nets are sequentially processed, using a least cost algorithm (e.g., [Dij59] in conjunction with [Pri57]).
- v) block placement is modified to avoid routing failure (except for [Hig80]).
- vi) the routing areas are estimated by deterministic methods.
- vii) no procedure is given for handling the power and ground nets.

In [Pre79] an approach is given for the automation of both placement and routing. First a placement hierarchy is formed by partitioning the blocks, based on their connectivity, into groups each of which is in turn partitioned into subgroups and so on until small enough groups are formed. Each group of the lowest level of this placement hierarchy is laid out and enclosed in a rectangle. The resulting

rectangles are then considered as blocks and are laid out in groups according to the prespecified placement partition. This process is continued until the complete layout is obtained. The routing of each group of blocks is broken up into five steps:

- i) channel routing order
- ii) topological routing (including channel width estimation)
- iii) channel routing order
- iv) track assignment
- v) absolute coordinate assignment.

In step i) the channel order needed in step iv) is determined. A least cost path for each net is found in step ii). Since the channel routing order is dependent on the outcome of step ii), it is re-computed in step iii). In step iv), an extension of the channel routing algorithm in [Koz74] is used to assign tracks to the net segments.

Although the work in [Pre79] represents the first serious attempt to completely automate the layout of custom integrated circuits, it suffers from the following methodological problems:

- i) The hierarchical decomposition of layout is likely to be inefficient in area utilization for the following reasons:
 - a) the natural shape of the layout of an arbitrary group of modules is not necessarily rectangular. Thus each time a group of modules is enclosed in a rectangle, some area is likely to be wasted.
 - b) at each level of the hierarchy the interconnections are unnecessarily forbidden from passing through the lower level modules. This introduces detours in some of the interconnection paths that may require additional area.
- ii) A close look at the first 3 routing steps reveals the following logical flaw. In order to find a channel routing order a list of critical channels (channels with the property that an increase in their widths will cause an increase in the layout area) is needed. But this list is unavailable until the topological routing is completed. Therefore step i) cannot be correctly performed. But if the result of step i) is not correct, how can the channel width estimates, which depend on the channel order, be correctly computed? A similar problem occurs in the estimation of channel widths. These estimates are determined by topological routing which is in turn dependent on the channel widths.
- iii) The criterion for topological routing does not include interconnection lengths except perhaps indirectly through the attempt to minimize area.

The router described in this paper differs from the methods in [Kan76, Pre79, Lau80, San80, Hig80] in the following regard:

- i) Channel width estimation is done using the statistical method in [EIG81b].

- ii) Two types of placement reorganization are considered: a major reorganization, where the topology of the channel graph is allowed to change, and a minor reorganization, where only the dimensions of the channel graph are allowed to change. Both reorganizations are done using a combination of critical paths and quadratic programming.
- iii) The costs determining the net paths are not changed during topological routing. Thus no ordering of interconnections in topological routing is needed.
- iv) Routing of variable width, single layer power and ground trees is accomplished using the simple algorithm given in Sec.2.

6. ROUTING RESULTS

Figures 5-7 illustrate the final layout achieved by our router using a VAX 11/780 computer. The example of Fig.4 is a Stanford University, student project, having 5 blocks, 50 nets including power and ground, 115 terminals. The routing for this example was obtained in 1 min, 53 seconds (CPU time). The example of Fig.5 was provided by AMI Corporation. This example has 38 blocks, 121 nets, 470 terminals. Total CPU time for the complete layout in this case was 15 minutes, 39 seconds. The final example (Fig. 7) is the IMP (Image Memory Processing) IC designed by Marc Hannah at Stanford University. The IMP IC has 16 blocks, 238 nets, 728 terminals and took our router 12 minutes, 18 seconds to obtain the final layout.

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REFERENCES

- [Deu76] Deutsch, D., "A dogleg channel router," *Proc. 13th Design Automation Conf.*, San Francisco, CA, June 1976, pp. 425-233.
- [Dij59] Dijkstra, E.W., "A note on two problems in connection with graphs," *Numerische Mathematik*, vol. 1, 1959, pp. 269-271.
- [ElG81a] El Gamal, A., "Two-dimensional stochastic model for interconnections in master slice integrated circuits," *IEEE Trans. on Circuits & Systems*, vol. CAS-28, Feb. 1981, pp. 127-138.
- [ElG81b] El Gamal, A. & Syed, Z., "A stochastic model for interconnections in custom integrated circuits," *IEEE Trans. on Circuits & Systems*, Sept. 1981, pp. 888-894.
- [Gil72] Gill, P.E. & Murray, W., "Two Methods for the Solution of Linearly Constrained and Unconstrained Optimization Problem," National Physics Lab. Report NAC-25, Nov. 1972.
- [Hel78] Heller, W., Mikhail, W. & Donath, W., "Prediction of wiring space requirements for LSI," *J. Design Automation and Fault-Tolerant Computing*, 1978, pp. 117-144.
- [Hig69] Hightower, D.W., "A solution to line routing problems in the continuous plane," *Proc. 6th Design Automation Workshop*, June 1969, pp. 1-24.
- [Hig80] Hightower, D.W. & Boyd, R.L., "A generalized router," *Proc. 17th Design Automation Conf.*, June 1980, pp. 12-21.
- [Hor78] Horowitz, E. & Sahni, S., *Fundamentals of Computer Algorithms*, Computer Science Press, Potomac, Maryland, 1978.
- [Joh77] Johnson, D.B., "Efficient algorithms for shortest paths in sparse networks," *JACM*, vol. 24, Jan. 1977, pp. 1-13.
- [Kan76] Kani, K., Kawanishi, H. & Kishimoto, A., "ROBIN: a building block LSI routing problem," *Proc. Int. Symp. on Circuits & Systems*, April 1976, pp. 658-661.
- [Koz74] Kozawa, T., Horino, H., Ishiga, T., Sakemi, J. & Sato, S., "Advanced LILAC: an automated layout generation system for MOS/LSI," *Proc. 11th Design Automation Workshop*, June 1974, pp.26-46.
- [Lau80] Lauther, U., "The SIEMENS CALCOS system for computer aided design of cell based IC layout," *Proc. 1st IEEE Conf. on Circuits & Computers*, Oct. 1980, pp. 768-771.
- [Mea80] Mead, C. & Conway, L., *Introduction to VLSI Systems*, Addison-Wesley, Reading, Mass., 1980.
- [Per77] Persky, G., Deutsch, D. & Schweikert, D., "LTX: a minicomputer based system for automated LSI layout," *J. Design Automation & Fault Tolerant Computing*, vol. 1, May 1977, pp. 217-255.
- [Pre79] Preas, B.T., "Placement and Routing Algorithms for Hierarchical Integrated Circuit Layout," Technical Report No. 180, Computer Systems Laboratory, Stanford University, Aug. 1979.
- [Pri57] Prim, R.C., "Shortest connection networks and some generalization," *BSTJ*, vol. 36, Nov. 1957, pp. 1389-1401.
- [San80] Sanson, W., Belle, H., & Heyn, W., "Design automation software towards MOS VLSI," *Proc. 1st IEEE Conf. on Circuits & Computers*, Oct. 1980, pp. 98-102.
- [Sye81] Syed, Z.A., "On Routing for Custom Integrated Circuits," Ph.D. dissertation, EE. Dept., USC, Los Angeles, CA, July 1981.
- [Sye82] Syed, Z.A. & El Gamal, A., "Single layer routing for power and ground networks in integrated circuits," *J. Digital Systems*, Feb. 1982, pp. 53-63.

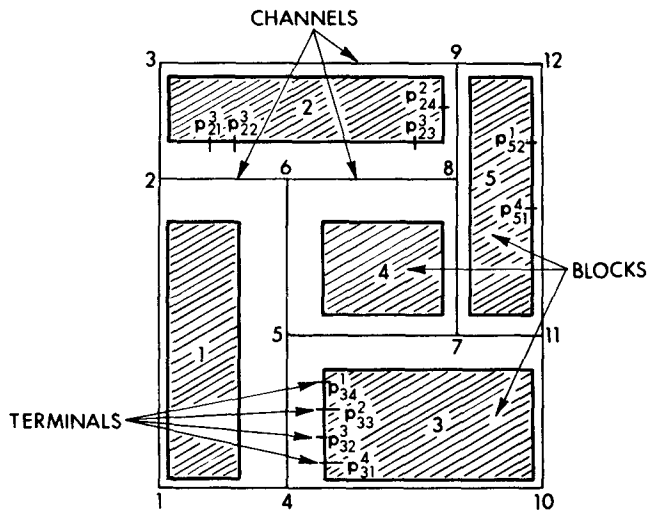


Figure 1. Example of a custom integrated circuit placement

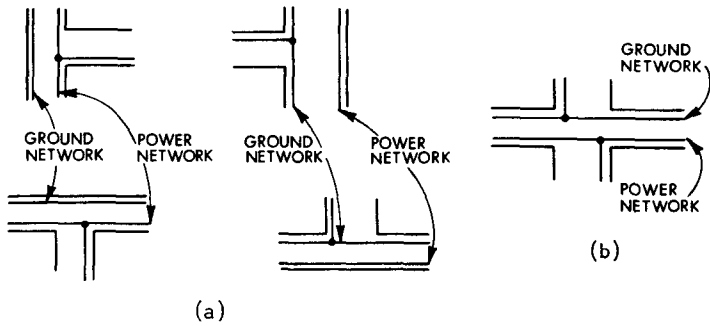


Figure 2. (a) Rules at "T" intersections, (b) Rule at "4" intersections

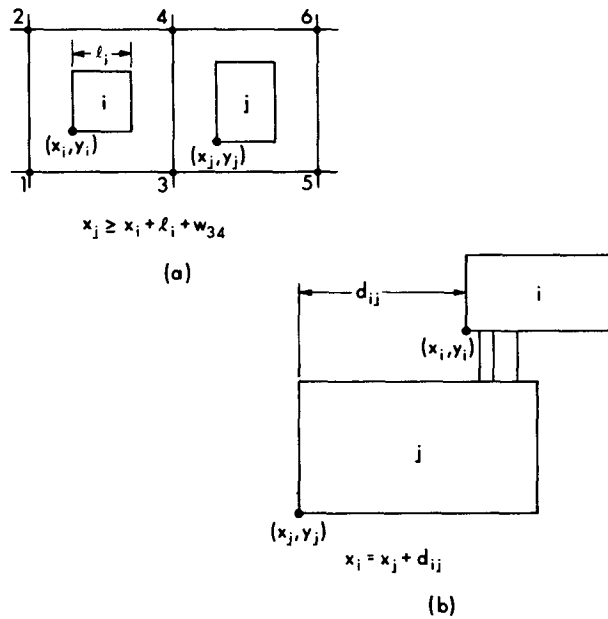


Figure 3. Constraints for placement

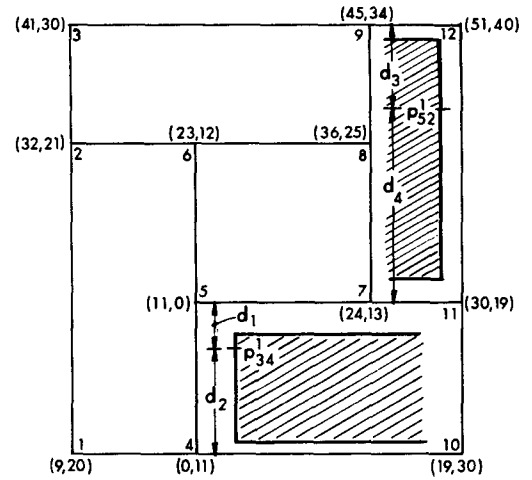


Figure 4. Channel graph for Fig. 1 labeled with respect to (4,5)

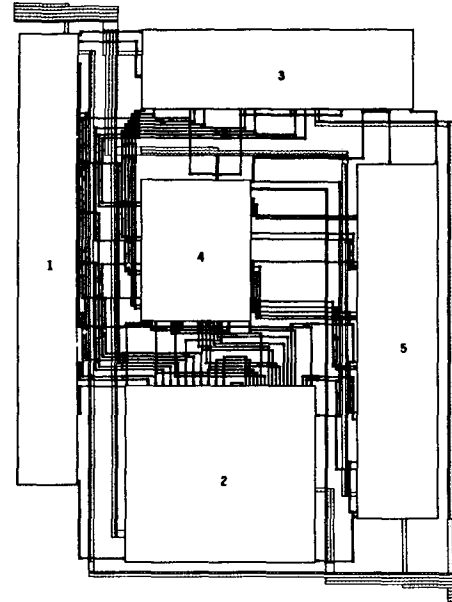


Figure 5. Final routing including power and ground for a student project

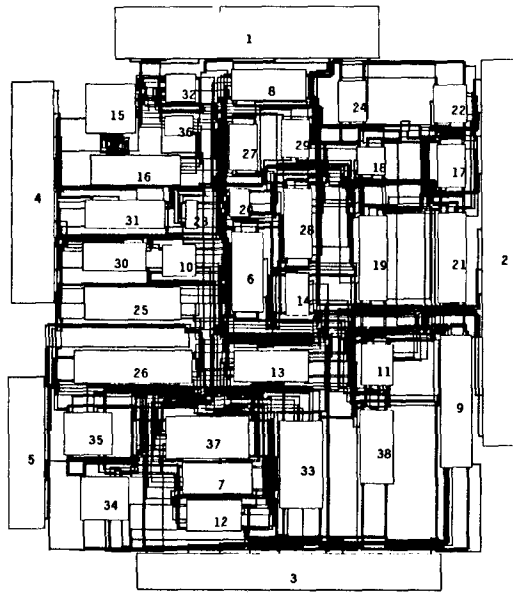


Figure 6. Final routing for the AMI example

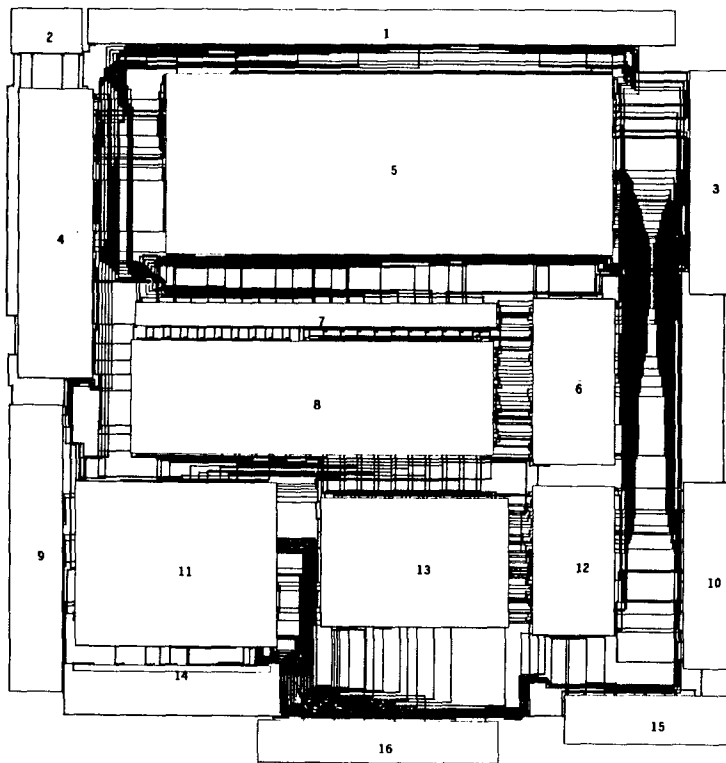


Figure 7. Final routing for IMP IC